Implementation Of Low Power NAND-Based Arithmetic Circuits Using CMOS Technology With SAPON Technique

K.J.Poornima[1], Gogula Chandana[2]
[1] Assistant professor, Dept of ECE
[2]Dept of ECE
[1, 2] VEMU Institute of Technology, P.Kothakota-517112

Abstract- *In the ultra large scale integration (ULSI) field, with widespread growing demand for portable and battery-operated electronic devices, power consumption has become a major concern. Common arithmetic circuits are adders and subtractors which are important components of digital systems and form a significant part of the total power dissipation of the circuit. Traditional CMOS realization of these circuits consumes excessively large number of transistors, leading to high power consumption, long propagation delay and silicon silicon area. To solve these problems, in this paper, low-power NAND-based arithmetic circuits have been developed by 45nm CMOS technology and combined with the idea of SAPON (Self-Adaptive Power Optimization Network). To reduce the complexity of the hardware, half adder, full adder and full subtractor circuits are achieved by using NAND-gate-based architectures as a universal logic gate. The technique called 'SAPON' (sequential active only power optimum) is used to optimize switching activity and thus also the power consumption with correct logical function. The proposed circuits are designed and simulated in Cadence Virtuoso tool, keeping technology 45nm CMOS, and performance analysis is performed based on three metric parameters of the circuits namely, the number of MOS transistors, power dissipation and propagation delay. Through simulation, it has been found that the arithmetic circuits proposed to use SAPON achieves significant power saving with respect to conventional CMOS circuits while maintaining the same delay. Hence, the proposed approach will be suitable for low power VLSI applications, portable electronics and the low power digital system applications.*

Keywords: CMOS Technology, NAND Gate, SAPON Technique, Half Adder, Full Adder, Full Subtractor

I. INTRODUCTION

The development of Very Large Scale Integration (VLSI) technology has allowed the creation of very integrated and powerful digital systems. In recent years, CMOS VLSI design methods have contributed to achieving low size, high reliability and high efficiency integrated circuits for modern applications [1]. In addition, digital integrated circuit design techniques have developed considerably as the demands for increased speed, functionality and power efficiency needed in electronic systems has increased [2]. The domestic manufacturers are dominated by the CMOS Digital integrated circuits that have viable power consumption, high noise immunity and scalable properties [3].

Arithmetic circuits are essential parts of all digital systems and have been widely used in the arithmetic logic unit (ALU) and processors, and digital signal processing applications [4]. In the field of digital circuit design, portability and battery operation have become more popular with requirements to use less power [5]. Because of this, a number of low power CMOS design methodologies has been proposed to reduce dynamic and static power consumption, while retaining system performance [6].Several researchers have suggested that one can perform optimized arithmetic in 5 dimensions.

Designed circuit architectures to enhance circuit efficiency. Zhuang and Wu gave a design of full adder based on CMOS to improve the performance of the arithmetic circuit [7]. Zimmermann and Fichtner examined and compared the different low-power logic styles, and how it performs for VLSI applications [8]. Shams et al. investigated the power-delay performance of low power CMOS full adder cells and the power-delay characteristics were discussed [9]. Chang et al. studied several different architectures of full adder circuits and pointed out the important role of them in optimizing the arithmetic circuit [10].To design and implement efficient VLSI circuits, it is essential to have a solid knowledge of digital circuit architecture and system level [11]. The use of the CMOS (complementary metal-oxide-semiconductor) integrated circuit design techniques offers good means for implementing reliable arithmetic circuits where the quantification of hardware is reduced [12]. With the demand for sustainable and power-efficient electronic systems in recent years, designing cool electronic systems using energy efficient techniques has attracted notable attention [13]. Furthermore, for the efficient digital integrated circuit, detail

analysis and optimization is crucial to achieve better performance and lower power consumption [14]. MOS transistors warrant extensive significance in understanding the overall behaviour and efficiency of the CMOS based circuits, not only during their operation, but also in their properties [15].

II. LITERATURE REVIEW

Weste and Harris [1] presented comprehensive CMOS VLSI design methodologies, covering transistor-level design, logic implementation, and performance optimization techniques. Rabaey et al. [2] discussed digital integrated circuit design principles with emphasis on power, delay, and area trade-offs. The authors explained various design approaches for achieving efficient CMOS circuits and emphasized the growing significance of low-power techniques in deep-submicron technologies. Kang and Leblebici [3] provided detailed analysis and design methodologies for CMOS digital integrated circuits. Their research was on CMOS switching characteristics, structures and power dissipation mechanisms that are imperative to low-power arithmetic circuits.The basic principles of digital design, such as half adder and full adder were described by Mano and Ciletti [4]. They started the theoretical basis to use logical components to perform arithmetic functions.

Chandrakasan and Brodersen [5] presented several low-power CMOS design techniques, including circuit and system level power reduction methods. They showed that reducing the power usage of portable and battery-operated electronic devices was of critical importance in their research. Roy and Prasad [6] have studied some low-power CMOS VLSI circuit design techniques to reduce the dynamic and leakage power consumption. Zhuang and Wu [7] proposed a new design for the CMOS full adder with good performance. They developed their architecture with the objective of minimizing the number of transistors used and increasing the efficiency of the operation, and thus suitable for arithmetic circuit applications.

Zimmermann and Fichtner [8] compared different styles of CMOS logic and compared their effect on power consumption, delay and circuit complexity in a system using pass-transistor logic. Shams et al. in [9] have done a thorough performance study of low power CMOS full adder cells. Chang et. al. [10] examined the comparisons of performance of some of the 0.18-µm full-adder architectures which are used in tree-structured arithmetic circuits. They investigated different designs and determined efficient solutions for performing high performance arithmetic applications.

Uyemura [11] discussed the basics of VLSI circuits and systems, design methodologies of combinational and sequential logic circuits.Razavi [12] introduced modern CMOS integrated circuit design techniques and highlighted optimization of transistors at the level of the circuit in order to enhance the circuit performance. A scalable, energy-quality implementation of integrated circuits and systems was discussed by Alioto [13] with emphasis on energy efficient design methodologies. The research brought up the need of power-aware circuit architectures in modern electronic systems. Hodges, Jackson, and Saleh [14] discussed the analysis and design of digital integrated circuits, the performance optimization technique and power considerations. Tsividis and McAndrew [15] gave a detailed explanation on the operation and modeling of a MOS transistor. The results of their research are used to find the behaviour and power consumption of a transistor in CMOS arithmetic circuits. But it is still a challenge to further reduce power in NAND-based arithmetic circuits. In view of this, the current work is interested in using low-power NAND based arithmetic circuits with CMOS technology and SAPON technique to increase the energy efficiency of the circuits without compromising their performance.

III. EXISTING METHOD

The conventional design of arithmetic circuits primarily relies on CMOS-based logic gate implementations to perform binary operations efficiently. Among the various logic gates used in digital systems, the NAND gate is widely preferred because of its universal functionality and ease of realization in CMOS technology. In the existing method, arithmetic circuits such as half adders and full adders are implemented using standard CMOS NAND gates without employing any additional power-reduction techniques.

The complementary operation of PMOS and NMOS transistors ensures correct logic functionality while maintaining low static power consumption. By combining multiple NAND gates, fundamental arithmetic circuits can be constructed to perform binary addition operations.

In the conventional NAND-based half adder, the SUM output is generated using an Exclusive-OR (XOR) function, while the CARRY output is obtained using an AND function. Since NAND gates are universal gates, both functions can be realized entirely using NAND gate combinations. In the same way, any number of NAND gates will be used to computeSUM and CARRY outputs for three input variables so a full adder is implemented more than one NAND gate. Arithmetic operations are made correctly, but during the operation, the circuit needs several switching

activities. While CMOS dissipates less static power than previous technologies, the dynamic power consumed during logic transitions is still of interest because of the continuous charging/discharging of load capacitances during these transitions. Furthermore, leakage current gains significance when the dimensions of the transistor are shrunk to the smaller technologynodes. All of these are responsible for the higher power consumption of conventional arithmetic circuits based on conventional NAND structures.

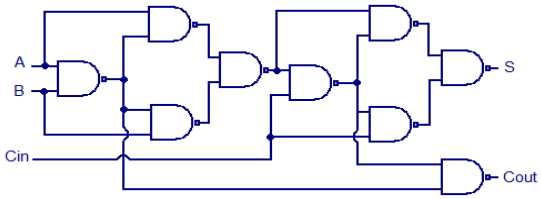

Fig.1. NAND Based Full adder schematic

The existing CMOS NAND-based Fig.1. represents arithmetic circuits offer advantages such as simple design methodology, reliable operation, and ease of implementation. However, they do not incorporate dedicated power-saving mechanisms to reduce switching power and leakage power. As a result, the overall energy efficiency of the circuit is limited, particularly in battery-powered and low-power applications.Therefore, to overcome the limitations of the conventional CMOS NAND-based arithmetic circuit and further reduce power dissipation, the SAPON technique is introduced in the proposed design. The proposed approach aims to improve power efficiency while maintaining correct logic functionality and acceptable circuit performance.

IV. PROPOSED SAPON-BASED LOW-POWER NAND ARITHMETIC CIRCUIT ARCHITECTURE

The proposed design Fig.2. incorporates the SAPON technique into a conventional CMOS NAND gate to achieve reduced power consumption and improved energy efficiency. The output of the gate is represented by Y, while A and B serve as the input signals.

In the proposed architecture, an additional SAPON transistor is inserted in the pull-down path between the NMOS network and ground. This transistor acts as a power-control element that regulates the current flow through the circuit. During active mode, the SAPON transistor remains ON, providing a low-resistance path to ground and allowing the NAND gate to operate normally. Under these conditions, the circuit produces the logic function

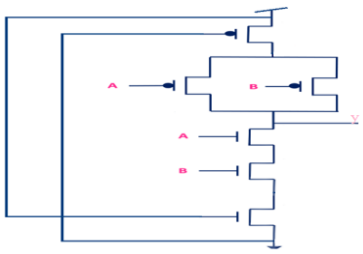

Fig.2. Block Diagram of NAND Gate using SAPON Technique

A. Half Adder using NAND gate

The proposed Half Adder Fig.3. is implemented by using SAPON based CMOS NAND gates for low power operation with correct arithmetic functionality. Since the NAND gate is a universal gate, all the required logic functions are obtained by means of NAND gate structures. The integration of SAPON technique into each NAND gate causes a reduction in leakage current and power dissipation, leading to an improvement in the energy efficiency of the circuit.

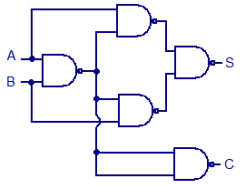

Fig.3. NAND Gate using Half Adder

The half adder has two binary inputs A and B, and produces two binary outputs, SUM and CARRY. The arithmetic operation is performed by NAND gate network and SAPON mechanism minimises unnecessary power consumption during switching. Thus the proposed design consumes less power and is more efficient than the conventional CMOS NAND based half adder which makes it suitable for low power VLSI applications.

B. Full Adder using NAND gate

The proposed Full Adder Fig.4. is implemented using SAPON-based CMOS NAND gates to achieve low-power and energy-efficient operation. The NAND gate is used as the fundamental building block because it can realize all required logic functions using a single gate type. By integrating the SAPON technique into the NAND gate structure, leakage current and overall power dissipation are reduced, resulting in improved circuit efficiency.

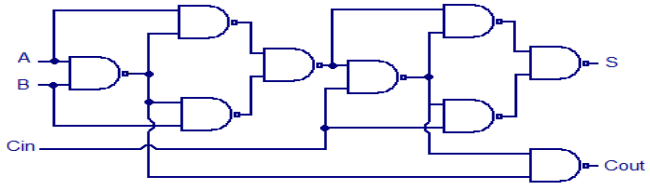

Fig.4. NAND Gate using Full Adder

The full adder performs the addition of three binary inputs, A, B, and Carry-In (Cin), and generates SUM and Carry-Out (Cout) outputs. The interconnected SAPON-based NAND gates perform the required arithmetic operation while minimizing unnecessary power consumption during switching. Consequently, the proposed design exhibits lower power dissipation

C. Full Subtractor using NAND gate

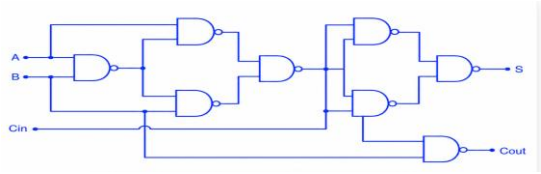

Fig.5. NAND Gate using Full Subtractor

The proposed Full Subtractor is designed with SAPON based CMOS NAND gates to achieve low power operation with correct subtraction operation. The universal property of the NAND gate allows for the implementation of all the necessary logic functions using only one type of gate. Energy efficiency is improved by employing SAPON technique for leakage current and power dissipation reduction. The circuit performs the subtraction of inputs A and B with Borrow-In (Bin) and generates Difference (D) and Borrow-Out (Bout) outputs with minimum power consumption during switching.

We propose SAPON-based NAND arithmetic circuits to obtain better power efficiency than conventional CMOS NAND designs. The SAPON technique is suitable for modern low power VLSI applications, since it minimises power dissipation and heat generation by minimising leakage current and unnecessary energy consumption.

This results in enhanced energy efficiency, extended battery life for portable devices and a dependable solution for low power CMOS VLSI design.

V. RESULTS AND DISCUSSION

The proposed SAPON technique Fig.6. is incorporated into the conventional CMOS NAND gate to achieve low-power operation. In a standard CMOS NAND gate, two PMOS transistors form the pull-up network while two NMOS transistors form the pull-down network. In the proposed design, an additional NMOS transistor is inserted between the pull-down network and ground. This transistor acts as a SAPON transistor and controls the current flow through the circuit.

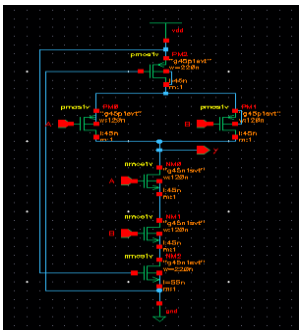

Fig.6.Schematic of Proposed SAPON technique

During active operation, the SAPON transistor remains ON, allowing the NAND gate to function normally and produce the required logic output. At the same time, the SAPON transistor limits unnecessary leakage current flowing through the pull-down path. As a result, static power dissipation is significantly reduced without affecting the logical functionality of the circuit. The reduced leakage current also minimizes heat generation and improves overall energy efficiency.

Simulation and waveforms

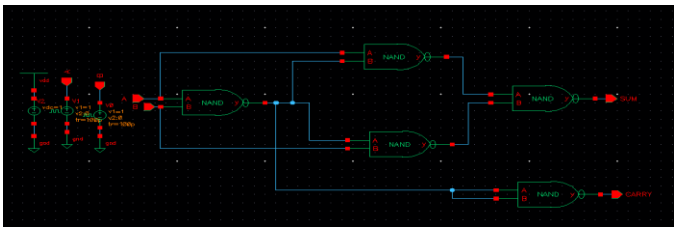

Fig.7.Schematic of Proposed Half Adder

The proposed Half Adder Fig.7. is implemented using SAPON-based NAND gates in the Cadence environment. The circuit accepts two binary inputs, **A** and **B,** and generates **SUM** and **CARRY** outputs. The first NAND gate produces an intermediate signal that is further processed by additional NAND gates to realize the XOR function for the SUM output, while the CARRY output is obtained through the NAND-based implementation of the AND function

Fig.8.Output Waveforms of Hlaf Adder

Fig.8. represents waveform confirms the correct operation of the proposed **SAPON-based NAND Half Adder**. Inputs **A** and **B** are applied in all possible combinations, and the corresponding **SUM** and **CARRY** outputs are observed.The waveforms obtained are in accordance with the half adder truth table, which confirms the proper working of the circuit. The application of SAPON based NAND gates has the advantage of decreasing power dissipation and preserving accurate arithmetic operation and reliable output transition.

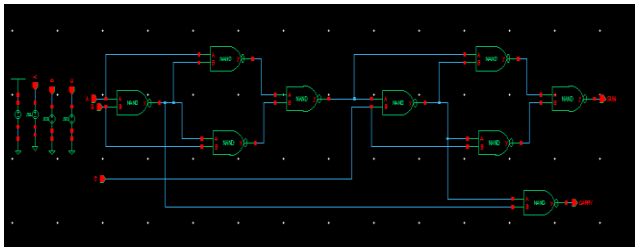

Fig.9.Schematic of Full Adder

As per the SAPON, Fig.9. is a construction of Full Adder using NAND gates. It has three inputs: A, B and Cin. The circuit is a binary addition circuit that uses an interconnection of NAND gates to produce SUM and Cout. All the required arithmetic operations are performed by only NAND gates, guaranteeing simplicity of design and reliable operation.

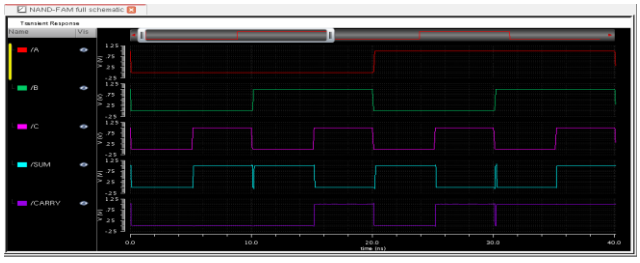

Fig.10.Output waveforms of Full Adder

The simulation waveform of the proposed SAPON-based NAND Full Adder is shown in Fig. 10, which indicates that it is working correctly. Different binary combinations of A, B and Cin are used for both inputs and the output binary combinations of SUM and CARRY are examined. The SUM output will be HIGH if there is an odd number of HIGH inputs, the CARRY output will be HIGH if two or more of the inputs are HIGH.

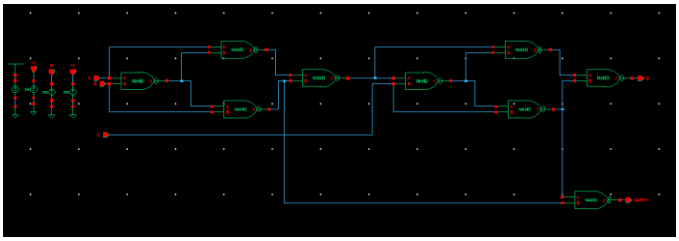

Fig.11.Schematic of Proposed Full substractor

The Full Subtractor implemented using SAPON based NAND gates is shown in Fig. 11. A, B, Bin (Borrow-In) are the three inputs to the circuit and D (Difference) and Bout (Borrow-Out) are the two outputs of the circuit. The subtraction is performed in a structured manner using NAND gates, with the use of only NAND configurations for the subtraction logic functions. The design method allows for an efficient function to be achieved with a simple and reliable circuit structure.

The use of the SAPON technique in every NAND gate allows leakage current to be minimized, and overall power consumption to be reduced. Therefore, the proposed full subtractor can be realized with energy efficient with the same accuracy in subtraction operation. The above features are suitable for low-power VLSI uses

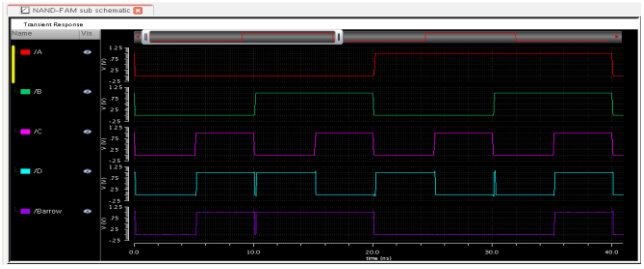

Fig.12.Output Waveforms of Full Substractor

Fig. 12 shows the simulation waveform of the proposed SAPON-based NAND Full Subtractor, validating its correct functionality. Various combinations of the inputs A, B, and Bin are applied, and the corresponding outputs Difference (D) and Borrow-Out (Bout) are examined. The Difference output indicates the result of the binary subtraction operation, whereas the Borrow-Out output becomes HIGH whenever the subtraction process requires a borrow condition.

Table.1. Comparision table between CMOS Universal gate and SAPON Universal gate

Parameter	MOS Count (CMOS NAND)	MOS Count (SAPON NAND)	Power (nW) CMOS NAND	Power (nW) SAPON NAND	Delay (ns) CMOS NAND	Delay (ns) SAPON NAND
Half Adder	20	30	193.0	162.1	4.94	4.94
Full Adder	36	54	303.7	250.9	14.95	14.95
Full Subtractor	36	54	309.7	255.2	14.94	14.94

A comparative analysis of the conventional CMOS NAND based arithmetic circuits with the proposed arithmetic circuits based on SAPON is presented in Table 1 with respect to the number of MOS transistors, power consumption, and propagation delay. The evaluation is done for half adder, full adder and full subtractor circuits. The proposed SAPON based implementations need a larger number of MOS transistors due to the extra SAPON circuits in each implementation. The number of transistors used in the Half Adder is increased from 20 to 30, in the Full Adder from 36 to 54 and in the Full Subtractor from 54 to 74. Still, although power increases and hardware improves, there is a significant decrease in power use. The power consumption of the Half Adder reduces from 193.0 nW to 162.1 nW and the power consumption of the Full Adder reduces from 303.7 nW to 250.9 nW. Likewise, the power consumption of Full Subtractor reduces from 309.7 nW to 255.2 nW. The above results show that the SAPON is very effective in leakage power reduction.

Besides this, the propagation delay is the same for every circuit, i.e., 4.94 ns for the Half Adder, 14.95 ns for the Full Adder and 14.94 ns for the Full Subtractor. This means that the proposed solution is power efficient without having to compromise on the speed of the circuits.

Energy efficiency of the arithmetic circuits is improved, and significant power savings compared to the conventional CMOS circuits are obtained, for the overall circuit based on the SAPON.

VI. CONCLUSION

The paper discussed the design and realization of low power NAND based arithmetic circuits using the SAPON technique in CMOS technology. The Half Adder, Full Adder and Full Subtractor circuits were implemented using SAPON enhanced NAND gates as the basic gates in the proposed approach. The conventional CMOS NAND gate structure was modified by using the SAPON technique, which reduced leakage current and the total power consumption, but did not affect the accuracy of the arithmetic operation. Arithmetic circuits have been designed and simulated in Cadence environment and the obtained simulation waveforms were correct in showing the correct arithmetic operations. The analysis of performance indicated that the designs using SAPON consumed less power than the conventional CMOS NAND-based designs and also were efficient in terms of energy consumption. Moreover, the proposed architecture retains the original delay characteristics and achieves substantial power saving, thus making it suitable for low power VLSI applications. These benefits make the design suitable for portable, battery-powered and energy efficient digital systems. Future research may target to further power optimize the circuit by extending the SAPON technique to different more complex arithmetic units and signal-processing architectures so as to obtain better performance of the circuits.

VII. ACKNOWLEDGMENT

The authors express their sincere gratitude to the faculty and management of **Vemu Institute of Technology (VEMU)** for their continuous support and guidance.

We also thank the Department of ECE for providing the necessary facilities to carry out this work for M.Tech.

REFERENCES

[1] N. H. E. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2011.
[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.
[3] S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd ed. New York, NY, USA: McGraw-Hill, 2003.
[4] M. Morris Mano and M. D. Ciletti, Digital Design, 5th ed. New York, NY, USA: Pearson Education, 2013.
[5] A. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design. Boston, MA, USA: Kluwer Academic Publishers, 1995.
[6] K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design. New York, NY, USA: Wiley-Interscience, 2000.
[7] N. Zhuang and H. Wu, "A New Design of the CMOS Full Adder," IEEE Journal of Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.
[8] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic," IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
[9] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full

Adder Cells," IEEE Transactions on VLSI Systems, vol. 10, no. 1, pp. 20–29, Feb. 2002.
[10] C. H. Chang, J. Gu, and M. Zhang, "A Review of 0.18-μm Full Adder Performances for Tree Structured Arithmetic Circuits," IEEE Transactions on VLSI Systems, vol. 13, no. 6, pp. 686–695, Jun. 2005.
[11] J. P. Uyemura, Introduction to VLSI Circuits and Systems. New York, NY, USA: Wiley, 2002.
[12] B. Razavi, Design of CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill Education, 2017.
[13] M. Alioto, Energy-Quality Scalable Integrated Circuits and Systems. Switzerland: Springer, 2017.
[14] D. A. Hodges, H. G. Jackson, and R. A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed. New York, NY, USA: McGraw-Hill, 2004.
[15] Y. Tsividis and C. McAndrew, Operation and Modeling of the MOS Transistor, 3rd ed. New York, NY, USA: Oxford University Press, 2011.