An Area-Efficient Low-Power Fully Non-Volatile Full-Adder Using Reconfigurable Logic

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Abstract- *The miniaturization of CMOS results in high static power consumption in traditional computer system. Logic-in-memory (LIM) architecture based on emerging non-volatile memory (NVM) can significantly reduce static power consumption by embedding computing and logic functions into NVM. Magnetic tunnel junction (MTJ) is considered as one of the most promising candidates for LIM circuits owing to its high speed, nearly infinite endurance, and 3D back-end integration technology. This paper introduces a reconfigurable LIM circuit integrating spin transfer torque based MTJs (STT-MTJs). Unlike the conventional non-volatile full-adders (NV-FAs) that perform the "Sum" and "Co" operations with two sub-circuits, the proposed circuit can perform both operations. Simulation results based on 28 nm CMOS process design kit and a perpendicular STT-MTJ compact model show that the proposed NV-FA has the advantages of small area and low power consumption.*

Keywords- Logic-in-memory, magnetic tunnel junction, reconfigurable, non-volatile full-adder

I. INTRODUCTION

As CMOS technology nodes scale into ultra-deep-micron nodes, the performance of CMOS logic circuits is limited due to the increasing leakage current. Magnetic tunnel junction based on spin transfer torque (STT-MTJ) has been confirmed to have a great potential to improve computing density and reduce the power consumption owing to its advantages of non-volatility, high speed, great CMOS compatibility and durability. In hybrid CMOS/MTJ logic-in-memory (LIM) architecture, MTJs are used to compose the logic network to reduce the distance of data communication. The integration of computational functions into MTJs improves energy efficiency and speed.

Non-volatile full adder (NV-FA) based on LIM architecture has been widely investigated for building high-density and low-power arithmetic/logic units. However, most MTJ-based NV-FAs face two problems. The operands are not completely stored in MTJs, which makes it difficult to fully take the advantage of zero static power consumption of spintronic devices. Moreover, existing NV-FAs need two sub-circuits to perform "Sum" and "Co" operations, resulting in large area. Reconfigurable logic has been demonstrated to be effective in improving the performance and scalability of logic circuits. This paper presents a novel reconfigurable fully non-volatile full-adder (RFNV-FA) with characteristics of small area and low power consumption. The proposed RFNV-FA is validated by using the 28 nm CMOS design kit and a perpendicular STT-MTJ model. The simulated performance of RFNV-FA is compared with other MTJ-based NV-FAs to confirm the high area efficiency and low power consumption advantages of this new design.

The aim is to design Digital Logic circuits at Nano scale level. Creating complete circuits on a single layer by reducing size and increasing switching speed. Simulation of the circuits can be done using QCA Designer version 2.0.3. Often (smaller) digital computing components today. Over the past few years the computing hardware industry and chip manufacturers in particular have tried to achieve these small scale hardware devices by almost a brute force scaling down of the involved components. Thus one saw the development of such things as TFTs (Thin Film Transistors) and a whole range of Thin Film Design innovations aimed only at one thing - to scale down the existing components and save space. In this process both success and failure were achieved. The success was an achievement of feature sizes of 60nm, and the development of commercial hardware such micro-controllers and processors built using such tiny devices. The failure was that the power leakage as device sizes shrunk down, started to grow exponentially. About 5 years ago, switching power leakage was so small that researchers almost neglected the issue completely but today with the tiny chips we have, power dissipation is a major headache. At feature sizes mentioned above, power loss due to switching alone is reaching values of up to 50%. However, the story does not end here; there are bigger evils to be tackled. Even if we were able to come up with schemes to ebb this loss of power, it would not success. The reason being the fact that as device dimensions scale down, the variation between two transistors produced by the same process becomes serious enough to hamper the scalability and hence the usability of the device. Perhaps even more threatening is the fact that Quantum effects are beginning to show up now. Going any further below this scale would require researchers to develop knowledge about high power losses and building up and controlling very large

Electric Fields capable of damaging the device. To add to this, quantum mean a very high probability of electrons tunneling through the wires and other devices thus creating more troubles for the already troubled scientists. The time is therefore apt, to look elsewhere for newer ways of doing things, in short to look beyond silicon. In Quantum Cellular Automata we explore one such paradigm which has shown quite some potential over the past decade.

This report starts by restly delving into some quantum mechanics and in particular talking about quantum dots. We then introduce the concept of a Quantum Cellular Automata and the various interesting properties it displays. We then move on to the design of basic building blocks of digital circuit design using Quantum Cellular Automata wherein we explore some things such as quantum wires, inverters and majority gates. After looking at some of these basic designs, we go on to explore the concept of clocking with reference to Quantum Cellular Automata and the build-up of very basic synchronous machinery in terms of a shift register. We then discuss a couple of large regular designs such as ROMs and FPGAs that may potentially be built using these automata. Finally, we describe our own efforts toward extending the work in synchronous circuits using QCA's wherein we discuss some synchronous modules we had success in creating and also discuss some difficulties experienced in the same.

II. LITERATURE REVIEW

2.1 IMPLEMENTATION OF A CROSSBAR NETWORK USING QUANTUM-DOT CELLULAR AUTOMATA

Author: Christopher R. Graunke, David I. Wheeler, Douglas Tougaw, and Jeffrey D. Will

Characterize the method for the implementation of wire-crossing networks using quantum-dot cellular automata (QCA) cells. Such wire-crossing networks, also called crossbar networks, are an important part of modern programmable logic devices, such as programmable arrays of logic.

2.2 QCADESIGNER: A RAPID DESIGN AND SIMULATION TOOL FOR QUANTUM-DOT CELLULAR AUTOMATA

Author: Konrad Walus, Timothy J. Dysart, Graham A. Jullien, and R. Arief Budiman

This paper describes a project to create a novel design and simulation tool for quantum-dot cellular automata (QCA), namely QCADesigner. QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation.

2.3 COPLANAR QCA CROSSOVERS

Author: R. Devadoss, K. Paul and M. Balakrishnan

The propose a new mechanism for coplanar wire crossing, which is based on the clocking of cells. Not only is the proposed solution robust and easy to incorporate in designs, it enables the QCA fabric to be a simple, regular grid of only a single type of cells. the coplanar wire crossovers using a single type of QCA cells, which has significant implications in fabrication and fault tolerance.

2.4 REVERSIBLE LOGIC-BASED CONCURRENTLY TESTABLE LATCHES FOR MOLECULAR QCA

Author: Himanshu Thapliyaland Nagarajan Ranganathan

Dealt with the design of concurrently testable latches which are based on reversible conservative logic for molecular QCA. Conservative reversible circuits are a specific type of reversible circuits, in which there would be an equal number of 1's in the outputs as there would be on the inputs, in addition to one-to-one mapping. Thus, conservative logic is parity-preserving, i.e., the parity of the input vectors is equal to that of the output vectors.

III. METHODOLOGY

QCA TECHNOLOGY

A brief description about full adder is given in this section used to data encoded using QCA method.

3.1 QCA DEVICE

Quantum dots are semiconductors that are on the Nano meter scale. Obey quantum mechanical principle of quantum confinement. Exhibit energy bad gap that determines required wave length of radiation absorption and emission spectra. Requisite absorption and resultant emission wavelength dependent on dot size.

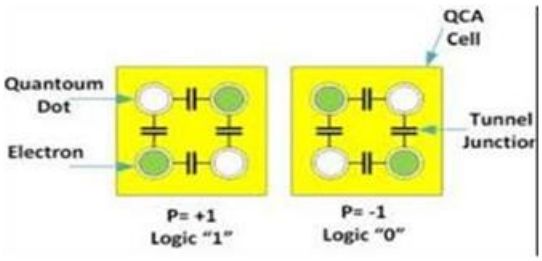

Figure1: Structure of QCA Cell

The isolated cell there are two energetically minimal equivalent arrangements of the two electrons in the QCA cell, denoted cell polarization P = +1 and cell polarization P = -1. Cell polarization P = +1 represents a binary 1 while cell polarization P = -1 represents a binary 0. This concept is also illustrated graphically Figure 1.

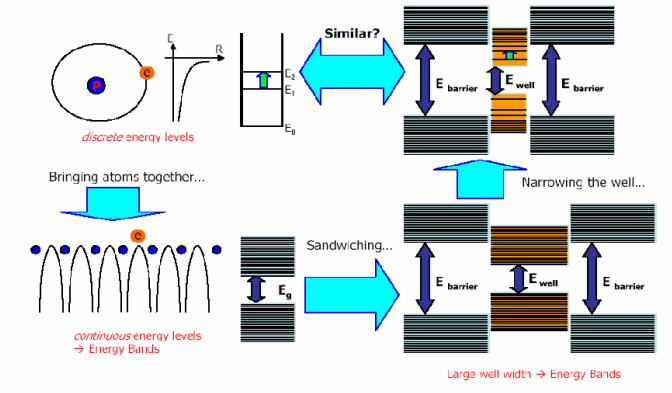

Figure 2: As the energy well, or the particle, shrinks the gap in energy levels increases

A proposal for implementing classical cellular automata by systems designed with quantum dots has been proposed under the name "quantum cellular automata" by Doug Tougaw and Craig Lent, as a replacement for classical computation using CMOS technology. In order to better differentiate between this proposal and models of cellular automata which perform quantum computation, many authors working on this subject now refer to this as a quantum dot cellular automaton.

The QCA clocking signal is used to control the potential barriers between Dots and no other external input is applied. When the potential of clocking signal is low the electrons are un localized. When the potential of clocking signal is high and sufficient then potential barrier increases which leads the electrons to be localized. When the potential barrier has reached it's highest point, the cell is said to be Latched. The QCA clocking signal is used to control the signal propagation along the QCA cells arrangement. There are Four-Different Phases in Clocking zones such as 'SWITCH, HOLD, RELEASE and RELAX'. Theses clocking zones are indicated in layout by different shades of gray background.

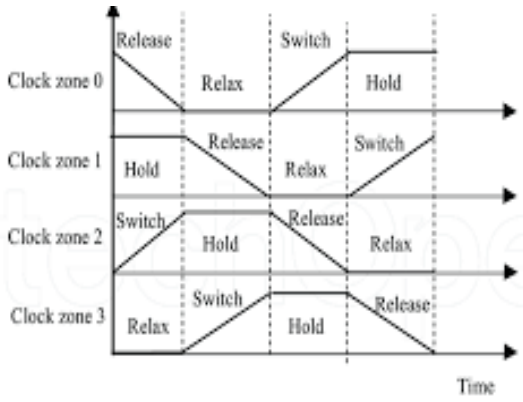

Figure 3: QCA Clocking Zones

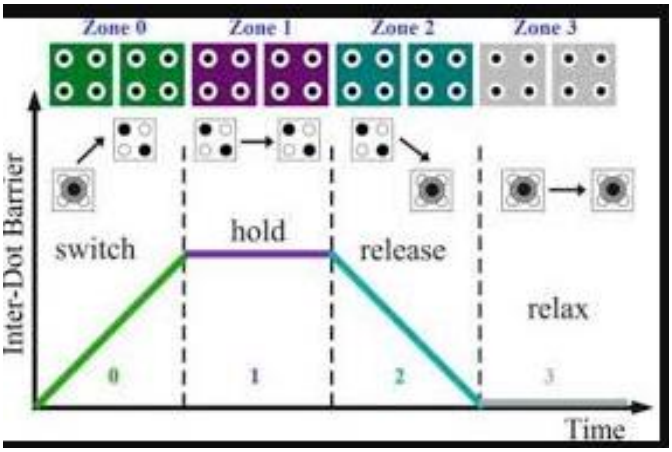

Figure 4: Four Phases of QCA Clock

SWITCH: During the switch phase, the inter dot barrier is gradually raised, and the QCA cell settles down to one of the two ground polarization states as influenced by its neighbors.

HOLD: During the hold phase, the inter dot barrier is held high, suppressing electron tunneling and maintaining the current ground polarization state of the QCA cell.

RELEASE: During this phase, the barriers are lowered and the cells are allowed to relax to an un polarized states.

RELAX: The barriers are kept low and the cells remain in un polarized state.

Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunnelling. Tunnelling paths are represented by the lines connecting the quantum dots in. Columbic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specific polarizations.

3.2 TWO HALF ADDER USING FULL ADDER DESIGN IN QCA TECHNOLOGY

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. Two of the input variables, denoted by A and B, represent the two significant bits to be added. The third input Ci, represents the carry from the previous lower significant position.

S =A'B'C + A'BC' + AB'C' + ABC
C = AB + BC + AC
Figure 5: Half adder using full adder

Expression of full adder:

Sum=a'b'c+a'bc'+ab'c'+abc=majority[majority(a,b,c)', majority(a,b,c'),c]
Carry = ab+bc+ca = majority(a,b,c)

IV. SIMULATION RESULTS

4.1 SIMULATION MODEL OF TWO HALF ADDER USING FULL ADDER

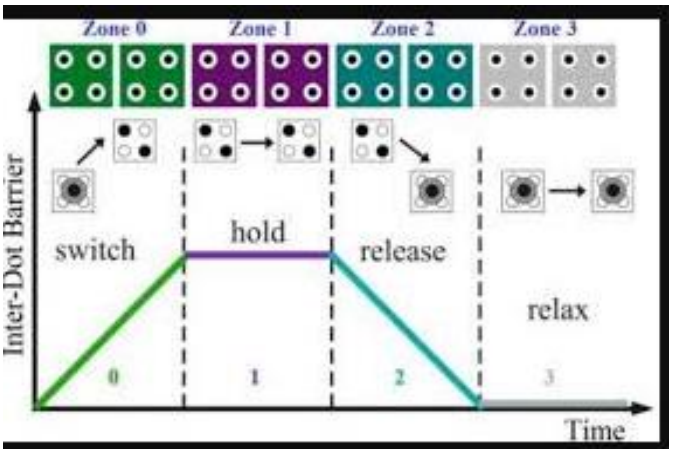

Figure 6: Simulation circuit of two half adder using full adder

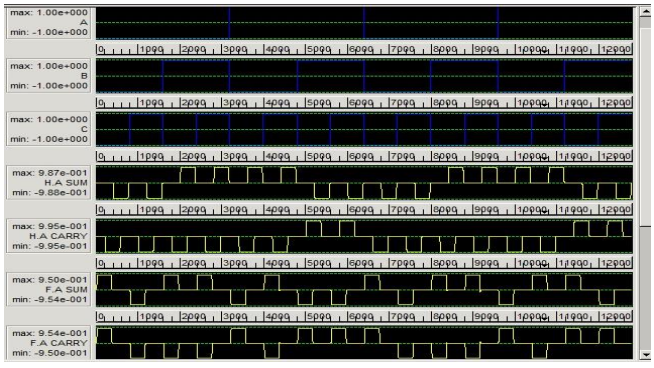

Figure 7: Simulation output of two half adder using full adder

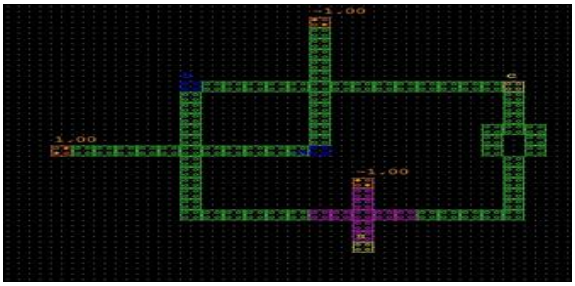
Figure 8: Simulation circuit of half adder

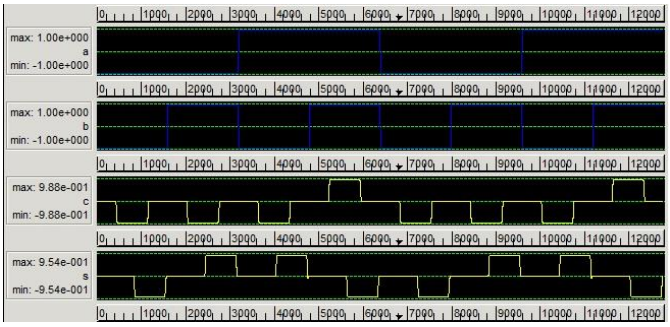

Figure 9: Simulation output of half adder

V. CONCLUSION

QCA is expected to achieve high device density, extremely low power consumption and very high switching speed. Half adder, Half adder using Full adder, was designed in QCA Designer and the simulation result was obtained. In this paper, we proposed a novel reconfigurable fully non-volatile full-adder which reduces the circuit area and the power consumption through a reconfigurable logic. By using a perpendicular STT-MTJ model and the 28 nm CMOS design kit, we successfully simulated and demonstrated the functionality of the circuit and investigated the effect of supply voltage and TMR ratio of STT-MTJ on the performance of the RFNV-FA. Simulation results show that our work has low dynamic power (0.95 μW) and sensing delay (116 ps). Meanwhile, we have the highest area efficiency compared to other previously proposed fully non-volatile FAs. Thus, the proposed circuit is appropriate for applications requiring low cost.

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