Design And Evaluation of Low Power Decoder Circuit Using Viterbi Decoder

M.Gayathri[1], R.Jamuna[2]
[1]Dept of ECE
[2]Assistant Professor, Dept of ECE
[1, 2] Tagore Institute Of Engineering And Technology(Tamilnadu)

Abstract*- This paper presents a new design of a 2 to 4 decoder constructed using 3-transistor NAND gates, contrasting it with the conventional 4 transistor NAND gate-based technique. The primary aim of this paper is to exhibit advancements in power efficiency, worst-case propagation time delay, and power delay product (PDP). These improvements underscore the efficacy of the 3-transistor NAND gate-based design, illustrating its potential for efficient and optimized decoder architectures. The simulation of the design is carried out using SPICE with 250nm technology.*

Keywords- CMOS, Delay, Low Power, NAND, PDP, VLSI.

I. INTRODUCTION

In VLSI circuits, power dissipation is a critical design parameter as it affects the performance, reliability, and cost of the VLSI system. In order to achieve the aforementioned objective, scientists suggested reduction in feature size and power supply voltage. However, the suggestion caused some unwanted consequences like tunnelling effects and reduction in the output voltage swing etc. In the current scenario of battery operated devices, the need for the low power has increased many folds and a new field of electronics for low power designing techniques has emerged. Low power design is a major issue in the electronics industry now a day, especially for battery-operated devices including computers, mobile phones, laptops, wearable devices, and implantable medical instruments. Therefore, along with factors like area and speed, power consumption also becomes a metric of utmost importance in measuring the circuit system performance.

The main advantages of CMOS circuits in digital systems are their high density and low power dissipation. However, for some applications, especially those that use battery-powered devices, power dissipation is still a critical concern. Therefore, various methods have been developed to lower the power dissipation of CMOS circuits at different design levels, such as technology, architecture, logic, and circuit. Supply voltage is one of the key factors which influences the power usage in CMOS circuits. By decreasing the supply voltage, the dynamic power dissipation, which is dependent on square of the voltage supplied, can be significantly lowered. However, decreasing the supply voltage also affects the circuit speed. Hence, it becomes necessary to make some compromises between power, robustness, and performance. Changes the supply voltage according to the environmental conditions and the workload. Another factor that influences the power dissipation of CMOS circuits is the switching activity. Switching activity refers to the number of transitions (from 0 to 1 or from 1 to 0) that happen in the circuit nodes during the operation. Switching activity determines the amount of charge and discharge currents that flow through the circuit, which contribute to the dynamic power dissipation. Therefore, lowering the switching activity can lower the power dissipation of CMOS circuits. Some methods to lower the switching activity include using efficient encoding schemes, exploiting signal correlations, reducing glitches, and optimizing logic and circuit design. A third factor that influence the power dissipation of CMOS circuits is the parasitic capacitance. Parasitic capacitance refers to the unwanted capacitance that exists between the circuit nodes and the ground or the power supply. Parasitic capacitance increases the load capacitance of the circuit, which affects the dynamic power consumption and the speed of circuit. Hence, lowering the parasitic capacitance can improve the power and performance of CMOS circuits. Some methods to lower the parasitic capacitance include using smaller transistors, shorter interconnects, and better layout techniques.

Decoders serve as pivotal components within digital systems, providing the capability to translate encoded inputs into specific outputs, thus enabling numerous applications across various domains. These circuits find extensive use in memory addressing, allowing computers to access particular memory locations in accordance with the address provided by the CPU. In data multiplexing and demultiplexing systems, decoders play a crucial role in routing information, directing it to the intended destination by decoding address information. Communication systems leverage decoders for error detection and correction, decrypting encoded data for error identification and recovery. These circuits can be implemented using various techniques, including logic gates, multiplexers,

ROMs, or programmable logic devices, with each method tailored to meet distinct design requirements and trade-offs.
The conventional design of decoders uses CMOS logic gates, which have high power consumption because of the direct path created between the ground and the power supply during switching. Various logic families and concepts have been tried to enhance the performance of the decoder circuits. These include adiabatic logic, dynamic logic styles, pass transistor logic (PTL), and transmission-gate logic (TGL).

II. LITERATURE REVIEW

2.1 DESIGN OF VITERBI DECODER USING HYBRID REGISTER EXCHANGE METHOD FOR LOW POWER APPLICATIONS

With increasing demand of wireless multimedia business, it is necessary to call for strict criterion on speed and power consumption of portable devices. Viterbi Decoder serves as an important role in error correction of communication devices.Significant power reduction can be achieved by modifying the design and implementation of Viterbi Decoder. In this paper we proposed the methods for survivor path storage and encoding as traceback (TB) and register exchange method (REM).REM consumes large power and area, due to huge switching activity.The problem of switching activity of Viterbi Decoder can be reduced by combining TB and REM and the method called Hybrid Register Exchange Method (HREM).The Viterbi Decoder is designed using REM, HREM and simulated on Xilinx tool and power is calculated on Xilinx power analyser. As the switching activity is reduced in HREM the Viterbi send coder achieves reduction in power in HREM as compared with REM.

2.2. VERY LOW POWER VITERBI DECODER EMPLOYING MINIMUM TRANSITION AND EXCHANGELESS ALGORITHMS FOR MULTIMEDIA MOBILE COMMUNICATION

A very low power consumption Viterbi Decoder has been developed by low supply voltage and 0.15 μm CMOS process technology. Significant power reduction can be achieved by modifying the design and implementation of Viterbi Decoder using conventional techniques traceback and Register Exchange to Hybrid Register Exchange Method (HREM), Minimum Transition Register Exchange Method (MTREM), Minimum Transition Hybrid Register Exchange Method (MTHREM), Register exchangeless Method and Hybrid Register exchangeless Method. By employing the above said schemes such as, HREM, MTREM, MTHREM, Register exchangeless Method and Hybrid Register exchangeless Method; the Viterbi Decoder achieves a drastic reduction in power consumption below 100μW at a supply voltage of 1.62 V when the data rate of 5 Mb/s and the bit error rate is less than 10-3. This excellent performance has been paved the way to employing the strong forward error correction and low power consumption portable terminals for personnel communication, mobile multimedia communication and digital audio broadcasting. Implementation insight and general conclusions can particularly benefit from this approach are given.

III. METHODOLOGY

VITERBI ALGORITHM

A brief description about Viterbi Decoder is given in this section used to decode data encoded using convolutional Decoder.

3.1 CONVOLUTIONAL DECODER

To encode the input data we use convolutional Decoder (k, n, K), where k number of output bits, n is number of input bits, and a constraint length K. There are 2K−1 states in VD. Therefore, there are 2K−1 surviving paths at each stage, and 2K -1 metrics, one foreach surviving path. For the formal specification, here we use (2, 1, 3) convolutional code. Thus, we can defined that the number of states in the trellis is 4. The generator polynomial for the Decoder is given by: g1 = [1, 1, 1] and g2 = [1, 0, 1]. So two memory elements will be require for designing convolution Decoder for code rate ½ and constraint length 3. Decoder design will work in serially time shifted data sequence manner. It involves the modulo-2 addition to generate output of selected input bit. Convolution Decoder can easily represented by state diagram, tree diagram & trellis diagram. A message encoded using a convolution Decoder follows called a trellis diagram. Each state transition on the diagram corresponds to a pair of output bits. There are only two allowed transitions for every state, so there are two allowed pairs of output bits, and the two other pairs are forbidden. If an error occurs, it is very likely that the receiver will get a set of forbidden pairs, which don't constitute a path on the trellis diagram. So, the task of the Decoder is to find a path on the trellis diagram which is the closest match to the received sequence.

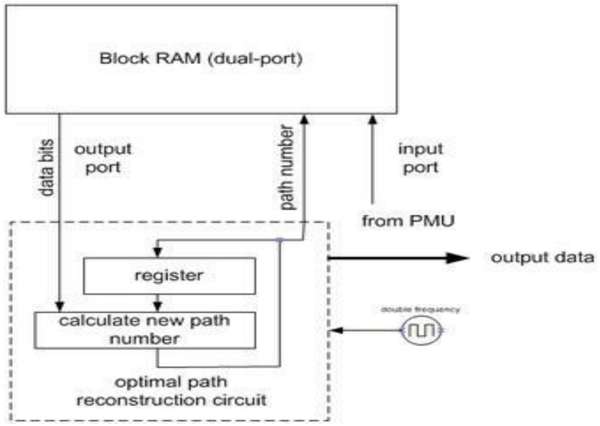


Figure1: Convolutional Decoder

3.2 VITERBI DECODING ALGORITHM

The Viterbi Decoder is assumed to be integrated in a larger synchronous system using a serial to parallel interface which continuously receives 2-bit symbols. Two bit output is generated for one input bit is first converted into soft decision. To implement a soft-decision VD, the output of the Decoder is translated from (0, 1) to (101, 011). 101 is the two‟s complement representation of the decimal number -3, and 011 is the representation of the decimal number 3 and then passes them to the Branch Metric Unit (BMU). The BMU computes the branch metric of each branch of the trellis by using Hamming distance. Each branch metric is added to the corresponding state metric, in theState Metric Unit (SMU), to generate the new state metric. The Add-Compare-Select unit receives two branch metrics and the state metrics. An ACS module adds each incoming branch metric of the state to the corresponding state metric and compares the two results to select a smaller one. The survivor path unit records the survivor path of each state selectedby the ACS module. Once the trellis diagram is reconstructed, tracing back through the trellis is performed.

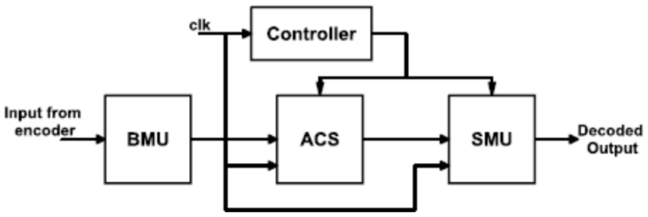


Figure 2: Synchronous Viterbi Decoder Using HREM

In the Viterbi Decoder; the register-exchange method is used to finish the survivor path storage and encoding. Frequent switching is the main disadvantage of register exchange method and long constraint length. The new proposed method designed for encoding data bits is known as hybrid register exchange method (HREM). Using this method switching activity can be reduced. Initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

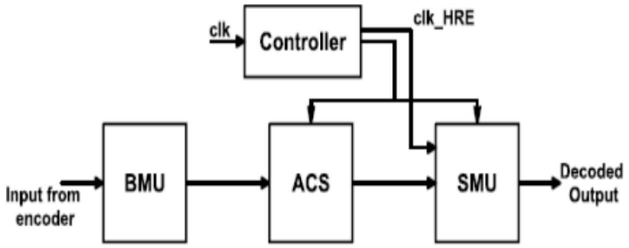


Figure 3: Proposed Asynchronous Viterbi Decoder Using HREM

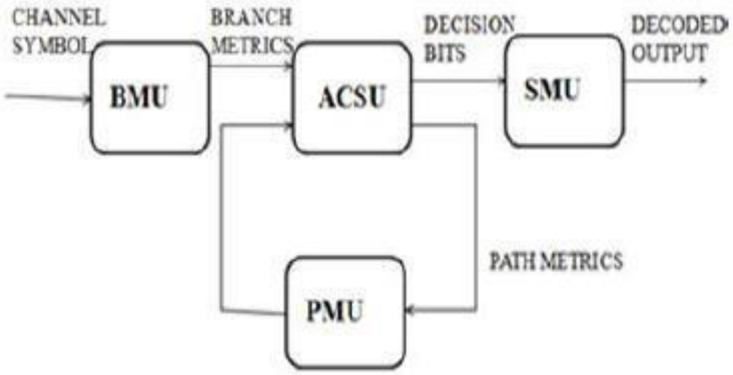


Figure 4: Block Diagram of Viterbi Decoder

In general, a ROM Decoder will require 1 out of N codes as input, which necessitates the usage of two input XOR gates. The “Wallace Tree Decoder” does not require these kinds of modifications because it receives the thermometer code as input directly. The ROM Decoder will address at least three lines if the comparator output has even a single bit defect, resulting in an error-free code. However, inaccuracy is much decreased with the Wallace Tree Decoder shown in Fig.2s Because the majority of the world's critical signals are analogue in nature. They are challenging to store and hard to process. As a result, they must be converted to digital pattern. An ADC converts analogue signals into digital data, allowing for more precise and dependable storage and processing.

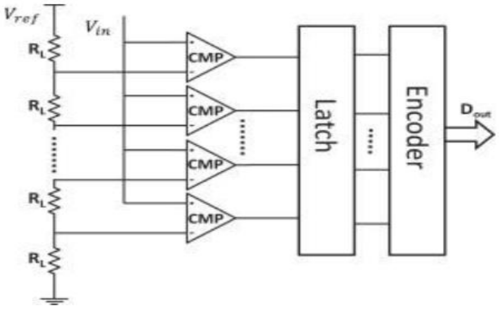


Figure 5:Block diagram of flash type ADC

1V. SIMULATION RESULTS

4.1 TOP LEVEL ARCHITECTURE

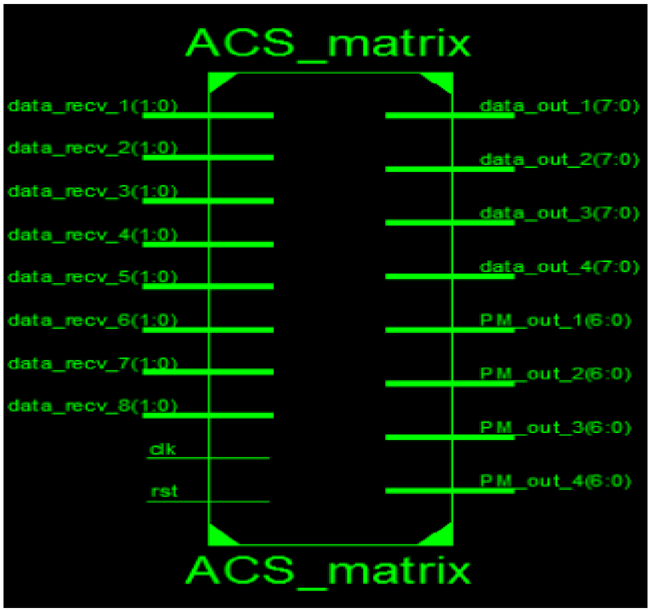


Figure 6: ACS MATRIX

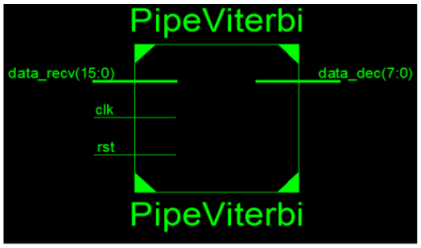
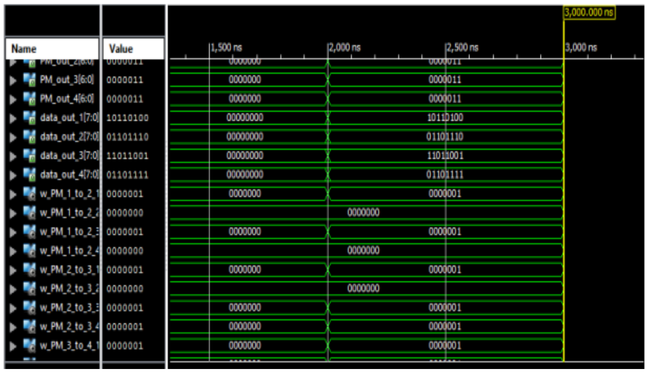
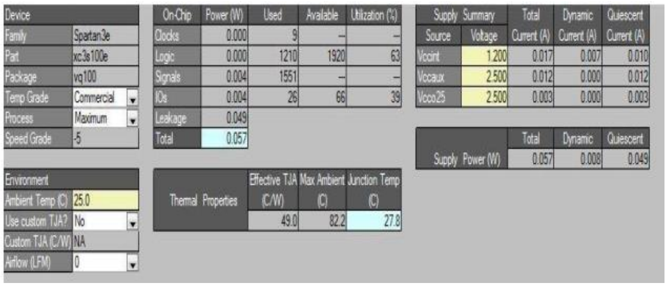


Figure 7: Pipeviterbi



Name	Value		
PM_out_3[6:0]	0000011	0000000	0000011
PM_out_4[6:0]	0000011	0000000	0000011
data_out_1[7:0]	10110100	00000000	10110100
data_out_2[7:0]	01101110	00000000	01101110
data_out_3[7:0]	11011001	00000000	11011001
data_out_4[7:0]	01101111	00000000	01101111
w_PM_1_to_2_1	0000001	0000000	0000001
w_PM_1_to_2_2	0000000	0000000	
w_PM_1_to_2_3	0000001	0000000	0000001
w_PM_1_to_2_4	0000000	0000000	
w_PM_2_to_3_1	0000001	0000000	0000001
w_PM_2_to_3_2	0000000	0000000	
w_PM_2_to_3_3	0000001	0000000	0000001
w_PM_2_to_3_4	0000001	0000000	0000001
w_PM_3_to_4_1	0000001	0000000	0000001

Figure 9: Simulation result of Viterbi Decoder



Device	
Family	Spartan3e
Part	xc3s100e
Package	vq100
Temp Grade	Commercial
Process	Maximum
Speed Grade	-5

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	9	--	--
Logic	0.000	1210	1920	63
Signals	0.004	1551	--	--
IOs	0.004	26	66	39
Leakage	0.049			
Total	0.057			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.017	0.007	0.010
Vccaux	2.500	0.012	0.000	0.012
Vcco25	2.500	0.003	0.000	0.003

	Total	Dynamic	Quiescent
Supply Power (W)	0.057	0.008	0.049

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	49.0	82.2	27.8

Figure 9: Power Analysis of Viterbi Decoder

V. CONCLUSION

Viterbi Decoder is designed using synchronous and asynchronous register exchange and hybrid register exchange method. The output waveform of the synchronous and asynchronous VD using HREM is shown in below respectively. VD is designed in Verilog using Xilinx 14.2. The dynamic power calculated for synchronous and asynchronous design is given .Asynchronous hybrid register exchange outperforms over synchronous and asynchronous register exchange & synchronous HREM. Both register exchange and hybrid register exchange module have been designed in synchronous and asynchronous technique. Asynchronous Hybrid register exchange method gives the 13.04 % reduction in dynamic power consumed when compared with its synchronous counterpart with much better increase in maximum frequency.

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