An Efficient BCD Adder Design Utilizing Reversible Logic Techniques

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Abstract- *Reversible logic gates are pivotal components digital circuit design, embodying the principle of reversibility that ensures each input state maps uniquely to a distinct output state without loss of information. Leveraging these principles, this paper presents a novel design and validation of a Binary-Coded Decimal (BCD) adder utilizing reversible logic gates, specifically ASK gates and New Gate (NG). Through the seamless integration of ASK and NG gates, the proposed design achieves significant improvements in efficiency and performance metrics. The design and validation processes are carried out using Xilinx software. Notably, it demonstrates a substantial reduction in gate count and ancilla inputs while effectively managing garbage outputs. The design features a gate count of 11, employs13 ancilla inputs, and generates 22 garbage outputs, show casing a remarkable 63.33% reduction in gate count compared to existing architectures. These findings highlight the efficiency, scalability, and potential applications of the proposed design in various domains including quantum computing, low-power systems, error-correction mechanisms, cryptography.*

Keywords- Ancilla Inputs, Garbage outputs, Low power, BCD Adder, Quantum Cost(QC).

I. INTRODUCTION

Reversible logic gates, unlike traditional irreversible gates,allow for the retrieval of input information from output data, adhering to the principle that no information is lost. Unlike conventional logic gates, reversible gates ensure that no information is lost during the computation process, allowing the system to be reversed and original inputs to be retrieved from the outputs. This characteristic is particularly beneficial in quantum computing, where operations must be reversible to maintain coherence and enable quantum gate construction. Unlike conventional logic gates, which dissipate energy with each bit of information loss, reversible logic gates are designed to be information-preserving, thus preventing energy dissipation as per Landauer's principle. This attribute is particularly advantageous in quantum computing, where maintaining coherence and minimizing energy loss are crucial for efficient computation. Reversible logic gates, by ensuring that each input state can be uniquely recovered from the output state, lay the groundwork for constructing quantum circuits that are not only energy-efficient but also capable of handling complex computational tasks.

The significance of reversible logic extends beyond quantum computing into fields like nanotechnology and optical computing. In these domains, the ability to minimize heat generation and energy consumption is paramount, especially as devices continue to shrink in size. Reversible gates enable the development of circuits that produce minimal heat, thereby enhancing the longevity and reliability of nanoscale devices. Additionally, optical computing, which relies on light for data transmission and processing, benefits from the low-energy dissipation properties of reversible gates, leading to faster and more efficient optical circuits. Each of these gates performs a unique purpose, such as copying, conditional control, or swapping operations, respectively. Because the quantum cost is a measurement of the complexity and resource needs of quantum circuits, the use of reversible logic is very necessary in order to cut down on the quantum cost.

The design of circuits using reversible logic gates is instrumental in applications that require low power consumption and high computational efficiency, such as digital signal processing (DSP), cryptography, and nanotechnology. This attribute is crucial in reducing power dissipation, as traditional logic gates dissipate energy due to information loss in the form of heat. Reversible gates, such as the Toffoli, Fredkin, and Peres gates, are widely used in constructing reversible circuits, each offering unique benefits in terms of functionality and complexity.

II. LITERATURE REVIEW

2.1 APPROXIMATE COMPUTING: AN EMERGING PARADIGM FOR ENERGY-EFFICIENT DESIGN

Approximate computing has recently emerged as a promising approach to energy-efficient design of digital systems. Approximate computing relies on the ability of many

systems and applications to tolerate some loss of quality or optimality in the computed result. By relaxing the need for fully precise or completely deterministic operations, approximate computing techniques allow substantially improved energy efficiency. This paper reviews recent progress in the area, including design of approximate arithmetic blocks, pertinent error and quality measures, and algorithm-level techniques for approximate computing.

2.2. MODELLING AND SYNTHESIS OF QUALITY-ENERGY OPTIMAL APPROXIMATE ADDERS

A formal model to prove that for signal processing applications using a quadratic signal-to-noise ratio error measure, reducing bit-wise error frequency is sub-optimal. Instead, energy-optimal approximate addition requires limiting maximum error magnitude. Intriguingly, due to possible error patterns, this is achieved by reducing carry chains significantly below what is allowed by the timing budget for a large fraction of sum bits, using an aligned, fixed internal-carry structure for higher significance bits. We further demonstrate that remaining approximation error is reduced by retaliation of conditional bounding (CB) logic for lower significance bits. A key contribution is the formalization of an approximate CB logic synthesis problem that produces a rich space of Pareto-optimal adders with a range of quality-energy tradeoffs. We show how CB logic can be customized to result in over-and under-estimating approximate adders, and how a dithering adder that mixes them produces zero-centered error distributions, and, in accumulation, a reduced-variance error. We demonstrate synthesized approximate adders with energy up to 60% smaller than that of a conventional timing-starved adder, where a 30% reduction is due to the superior synthesis of inexact CB logic. When used in a larger system implementing an image-processing algorithm, energy savings of 40% are possible.

III. METHODOLOGY

A brief description about BCD Adder is given in this section used to decode data encoded using CLA.

3.1 64- BIT BCD ADDER

Approximate computing forms a design alternative that exploits the intrinsic error resilience of various applications and produces energy-efficient circuits with small accuracy loss. In this paper, we propose an approximate hybrid high radix encoding for generating the partial products in signed multiplications that encodes the most significant bits with the accurateradix-4 encoding and the least significant bits with an approximate higher radix encoding. The approximations are performed by rounding the high radix values to their nearest power of two. The proposed technique can be configured to achieve the desired energy–accuracy tradeoffs. Compared with the accurate radix-4multiplier, the proposed multipliers deliver up to 56% energy and 55% area savings, when operating at the same frequency, while the imposed error is bounded by a Gaussian distribution with near-zero average. Moreover, the proposed multipliers are compare with state-of-the-art inexact multipliers, out performing them by up to 40% in energy consumption, for similar error values. Finally, we demonstrate the scalability of our technique. A parallel decimal BCD adder with improved performance is proposed in this paper by exploiting the properties of three different binary coded decimal (BCD) codes, namely the redundant BCD excess-3 code (XS-3), the overloaded decimal digit set (ODDS) code. The decimal carry-save algorithm based on BCD-4221/5211 is used in the PPR tree to obtain high performance adder.

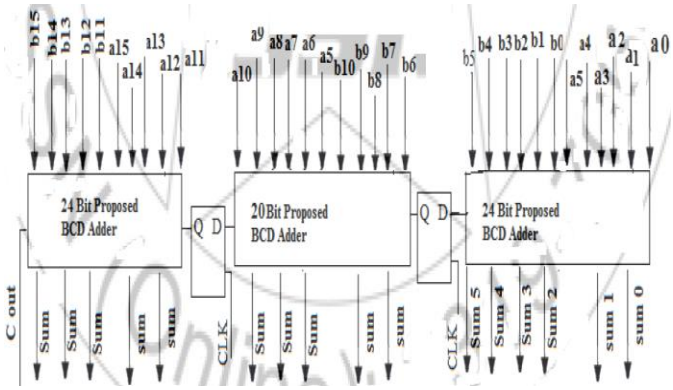

Figure1:Block diagram of 64bit BCD adder

The 64x64 bit is implemented using four 32x32 fault tolerant reversible Vedic multiplier. The outputs of four 32X32 bit multipliers are added with fault tolerant carry look ahead adder to obtain the final product. Now the basic building block of 64x64 bit fault tolerant reversible Vedic multiplier. The shown fig. 1 is a block diagram of MAC unit. The function of the MAC unit is given by the following equation $F = \Sigma Ai \times Bi$. The inputs for the MAC are fetched from memory location and fed to multiplier block of the MAC unit, which will perform the operation of multiplication and give the result to adder block which will accumulate the result and then will store the result into a memory location. That whole process is to be achieved in a single clock cycle. Multiplication is an important function in arithmetic operation. Multiplication based operation such as multiply and accumulate unit (MAC) and Arithmetic and logic unit (ALU). The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is

general formula applicable to multiplication operation. The strategy applied for developing a 64 x 64-bit Vedic multiplier is to design a 2 x 2- bit Vedic multiplier as a basic building module for the system. In the next stage of development a 4 x 4-bit multiplier is designed using 2 x 2-bit Vedic multiplier. Further in same manner 8 x 8, 16 x 16 and32 x 32- bit Vedic multiplier is designed. For the partial product addition for all stages of development a fast adders is used .Multiplier plays a very important role in today's digital circuits. The multiplier is based on an algorithm UrdhvaTiryagbhyam (Vertical and crosswise).This sutras shows how to handle multiplication of larger number (N X N bits) by breaking it into smaller sizes. Floating point number system is a common choice for many scientific computations due to its wide dynamic range feature. For instance, floating point arithmetic is widely used in many areas, especially in scientific computation, numerical processing, image processing and signal processing. The term floating point is derived from the fact that there is no fixed number of digits before and after the decimal point, that is, the decimal point or binary point can float. There are also representations in which the number of digits before and after the decimal or binary point is fixed; called fixedpoint representations. The advantage of floating-point representation over fixed point representation is that it can support a much wider range of values. The floating point numbers is based on scientific notation. A scientific notation is just another way to represent very large or very small numbers in a compact form such that they can be easily used for computations. The floating point multiplication operations are greatly affected by how the floating point multiplier is designed. Floating point number consists of three fields:

1. Sign (S): It used to denote the sign of the number i.e. 0 represent positive number and 1 represent negative number.
2. Significant or Mantissa (M): Mantissa is part of a floating point number which represents the magnitude of the number.
3. Exponent (E): Exponent is part of the floating point number that represents the number of places that the decimal point (binary point) is to be moved. Number system is completely specified by specifying a suitable base β, significant (mantissa) M, and exponent E. A floating point number F has the value. Multipliers are key components of many high performance systems such as FIR filters, Microprocessors, Digital Signal Processors etc. A system's performance is generally determined by the performance of the multiplier, because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a critical issue for an effective system design.

1V. SIMULATION RESULTS

4.1RTL SCHEMATIC 64 BIT BCD ADDER

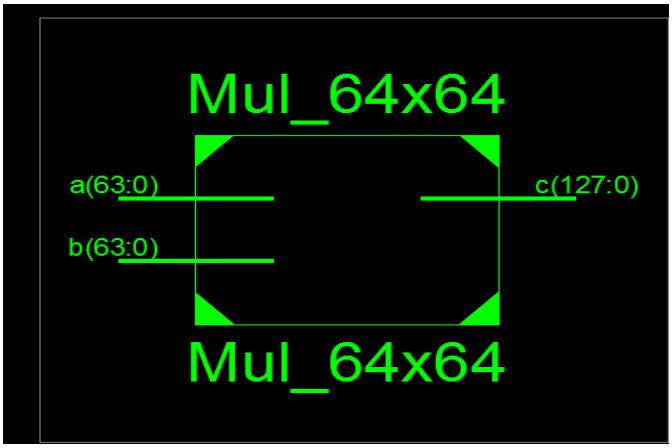

Figure2: RTL Schematic 64 Bit BCD Adder

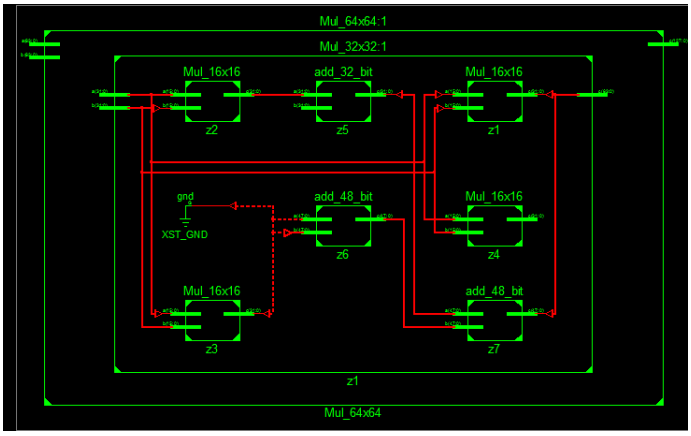

Figure 3: Technology view 64 Bit BCD Adder

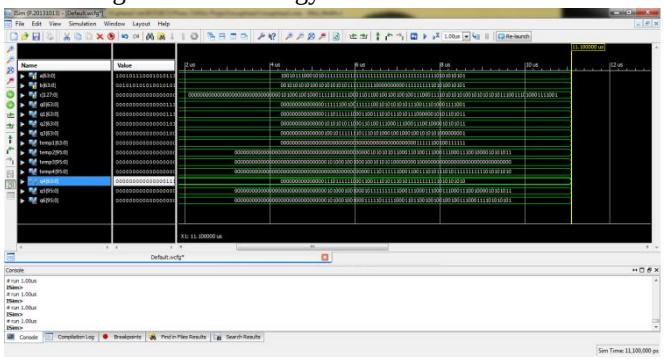

Figure 4: Xilinx Result of 64 Bit BCD Adder

V. CONCLUSION

In conclusion, the design of the Binary-Coded Decimal (BCD) adder using reversible logic gates, specifically ASK gates and the New Gate (NG), demonstrates significant improvements in both efficiency and performance metrics. By employing ASK and NG gates, the design reduces the overall

gate count and ancilla inputs, while effectively managing garbage outputs, leading to an enhanced performance of the BCD adder. The functionality and effectiveness of the design were validated through testing with Xilinx software and Verilog HDL. Simulation results confirmed the design's accuracy and efficiency, showing its ability to accurately perform BCD addition operations and maintain outputs within the valid BCD range. The proposed design includes a gate count of 11, utilizes 13 ancilla inputs, and generates 22 garbage outputs. Notably, there is a 63.33% reduction in gate count and a 40% reduction in garbage outputs compared to other existing architectures, highlighting the efficiency and scalability of the proposed design. In future, The efficient utilization of reversible logic gates in the BCD adder design can be extended to larger quantum circuits and algorithms in Low-Power applications.

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