Low PDP CMOS Full Adder Design

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Abstract- *In this work efforts are made to improve the performance of full adder with re-spect to power-delay product, power dissipation and time delays using 90nm CMOS technology. Currently there are two techniques used namely alternative internal logic structure and pass-transistor logic style that gives reduced power-delay product (PDP). We implement the full adder using above mentioned technologies and try to compare their performance and further develop a technology which will give the low PDP and low power consumption.*

Keywords- PDP,CMOS

I. INTRODUCTION

The power-delay product (PDP) is a measure of semiconductor device perfor- mance; lower power delay product means that power is better "translated" into speed of operation; figure of merit in digital IC's which shows that power needed to switch (lower the better) is as important to digital performance as a switching speed. Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architec- tures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation

In order to maintain speed, threshold voltage must be scaled down, but doing so standby current increases, which in turn implies that static power is the main contributor to total power and thus should be taken care of properly.

II. THEORY

The technology that has played an increasingly important role in the integrated circuit industry was Complementary Metal Oxide Silicon (CMOS). The basic principle behind the MOS field-effect tran- sistor was first proposed in 1925 by J.Lilienfeld and latter by O.Heil in 1935. At that time problems with materials occurred which have been overcame in later years. In 1965 the first MOS calculator was introduced, and latter in 1967 even different MOS devices that had a variety of commercial uses were presented.

In order to implement these circuits F. Wanlass built an nMOS tran-sistor as pMOS transistors were the only available at that time. Soon, these circuits concord the market because of their low power dissipation property. In the begin-ning CMOS was applied sparingly to general system designs since the processing technology required in the implementation of CMOS circuits was complex. As the technology improved and was able to support very large chip 6 sizes, the require-ments for low power dissipation circuits increased. Hence, the CMOS technology increased in the level of importance to the point where it is now the most dominant Very Large Scale Integration (VLSI) technology.

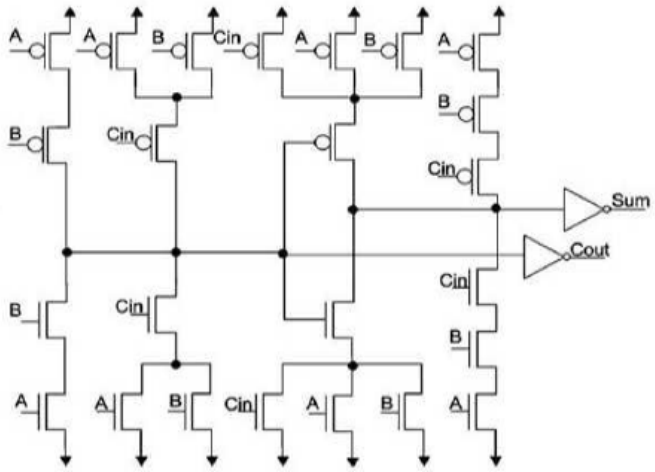

Fig. 1 C-CMOS full adder

III. METHODOLOGY

TIME-DELAY AND POWER DISSIPATION

The switching speed of CMOS gate is limited by the time taken to charge and dis-charge the load capacitance CL . An input transition results in an output transition that either charges CL toward VDD or discharges CL toward GND.

There are two components that establish the amount of power dissipated in CMOS circuit

- static dissipation due to leakage current or other current drawn continuously from the power supply; and
- dynamic dissipation due to switching of transient current, and charging and discharging of load capacitances.

HYBRID FULL ADDER CIRCUITS

The circuit is based on the explanation above works fine as long as the output does not tend towards either of the two high impedance cases. One such high impedance output can be prevented by adding an extra NMOS transistor whose source/drain is connected with input Cin and drain/source connected with SUM. This NMOS is switched on in the two situations when Semi XNOR gate gives an output 1, where value of SUM, in these states, becomes equal to Cin. Another high impedance can be removed by introducing a PMOS with its source/drain connected to SUM and drain/source to Cin

IV. RESULT AND DISCUSSION

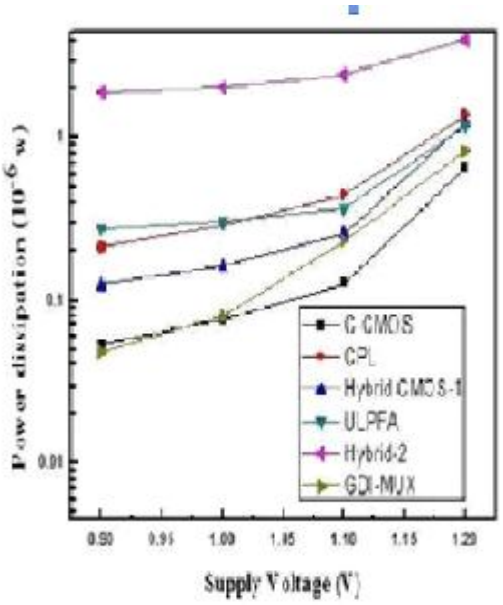

Fig.2 Power Dissipation Graph

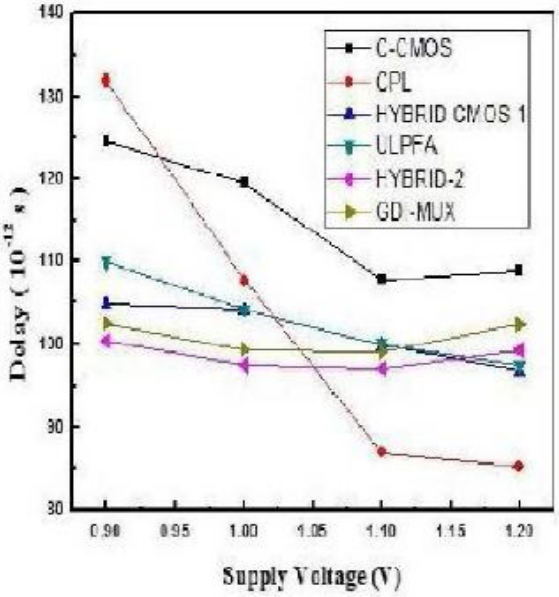

Fig.3 Delay Graph

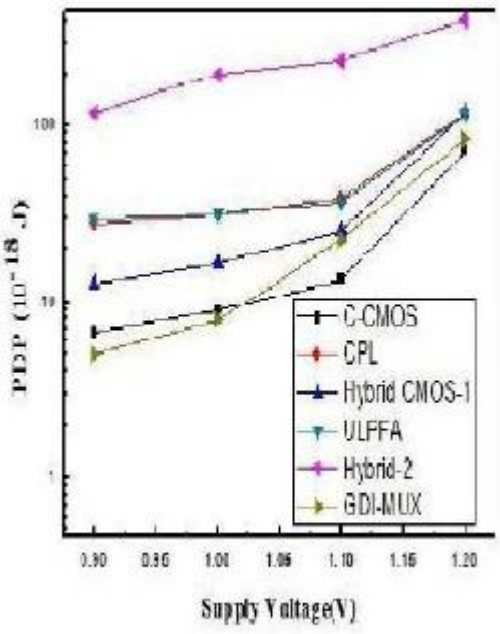

Figure 4: Power delay product graph

V. CONCLUSION

Various types of full adders with different logic styles have been implemented.. A comparison of all the designs shows the gradual improve- ment in power dissipation, delay and Power delay product (PDP). The considered reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design ensures the best PDP.

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