VLSI Implementation of Full Subtractor Using Split-Rail Charge Recovery Logic

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Abstract- *CMOS technology is evolving rapidly with the advancement in VLSI design. The gate count on the integrated chip is steadily rising which leads to enhanced power dissipation and heat generation. Therefore, a new paradigm that can circumvent these limitations needs to be devised. Adiabatic logic is one of the novel techniques used to attain high throughput with decreased power utilization in power-aware VLSI circuits Moreover, low-power arithmetic circuits are crucial these days to design high-end computing devices. The design of full subtractor using to implementation of SCRL (Split -Rail charge Recovery Logic) techniques are presented in this paper. The design and simulation are carried out on micro wind DSCH2.*

Keywords- Adiabatic logic, recovery of energy,Low power, Power dissipation.

I. INTRODUCTION

The appeal of CMOS design in VLSI technology is primarily driven by two factors: [1] low power consumption and a high level of integration. Due to the increase in chip density as technology advances, cooling techniques were unable to offer adequate and cost-effective system solutions. Electronics circuit and system design is a difficult and important process since it must deliver great efficiency with low power consumption [1].

The most important requirement is to pinpoint the source of power loss and take necessary action to address it utilizing proper methodology and technique that can produce the best outcomes. Adiabatic logic is one of the viable answers.

To reduce energy loss during the both charging and discharging phases of circuit operation, adiabatic logic can be used. [2]It is a charge recovery concept that runs on an intermittent AC power source rather than a steady DC supply. This is one of the main justifications for lessening power dissipation. Techniques for split rail-charge recovery are developed and used. Combinational circuits like multiplexers, half adders, full adders, half subtractors, and comparator simulation results show less power dissipation compared to the conventional method. Power reduction was suggested by Akshitha et al. using various partial adiabatic logic types for half adders and half subtractors[2].

The programmed that a micro wind DSCH2tool uses.[3] DSCH Micro wind is essentially a programmed for designing digital schematic circuits. This software for micro wind simulation enables users to model and simulate integrated circuits at the physical description level. This is easy navigation circuit simulation tool and it aided by massive symbol libraries. Micro wind is created as comprehensive system on desktop version to enable learners smart design strategies and procedures with more practice. It makes it simple for students to master the entire design process because to its built-in layout modification tools, mix-signal simulator, MOS characteristics viewer, and other features[3].

Designing and validating complicated logic structures is madepossible by DSCH's user-friendly environment of hierarchical logic design and quick simulation with delay analysis.

It is discovered that full subtractor designs have not yet extensively explored any of the designs reported using SCRL adiabatic techniques. The design of a full subtractor using the split rail charge recovery logic method is the focus of this paper. There are five distinct sections in the paper. Sections II and III discuss adiabatic logic and the design and implementation of a full subtractor, respectively. Section IV describes the current system, Section V describes a proposed system, and Section VI presents the results of the simulation.

II. ADIABATICLOGIC

Modern portable electronics require a significant amount of energy backup. The idea of adiabatic logic is illustrated in this section. It has been stressed that the energy recovery principle exists in adiabatic logic families.[4] The process between such a thermal system and its environment without a transfer of heat or substance is referred to as

"adiabatic" in science. The following three conditions are present in adiabatic logic circuits.

1. When there is a significant voltage difference between the transistor's sources and drain terminals, the transistor should be off.
2. When the transistor has current flowing through it, it should be turned on.
3. Diode should not be subjected to current[4].

Low-power electronic circuits which use reversible logic are known as adiabatic logic.[5] As an adiabatic process is a procedure where the total amount of heat or energy inside the system remains constant, the name "adiabatic process" was coined. The fundamental driver of research in this field is the promise of adiabatic circuits to significantly reduce energy dissipation as circuits become smaller and quicker. The majority of research has been on creating adiabatic logic using CMOS. Unfortunately, modern CMOS technology loses energy as heat, primarily when switching, despite being very energy-efficient compared to comparable technologies.

Two key guidelines that CMOS adiabatic circuits should adhere to in order to tackle this issue are listed below, along with an explanation of each. The first is to never switch on a transistor whenever the drain and source are at different voltages. The second advises against ever turning off a transistor that is currently conducting current. A variety of adiabatic CMOS digital circuits have been created.

The adiabatic logic circuits operate on the charge recovery principle. The energy is recycled rather than lost. Two categories of adiabatic logic families can be distinguished.:

- Partially or quasi adiabatic logic.
- Fully adiabatic logic.

Partially adiabatic logic can be classified as

- Efficient charge recovery logic (ECRL).
- 2N-2N2P adiabatic logic.
- Positive feedback adiabatic logic (PFAL).
- Clocked adiabatic logic (CAL).

Fully adiabatic logic can be classified as

- Pass transistor logic (PAL).
- Split rail-charge recovery logic (SCRL).

A comprehensive subtractor was implemented and analyzed in this study using SCRL[5].

III. DESIGN AND IMPLEMENTATION OF FULLSUBTRACTOR

Two binary numbers are entered into a subtractor circuit, which subtracts one of the inputs from the other.[6] It provides two outputs, difference and borrow, much like adders (carry-in the case of Adder). Two different subtractor exist.

1. Half Subtractor
2. Full Subtractor

Fig. 1 is the fundamental logic diagram for a complete subtractor with three inputs (A, B, and C) and two difference and borrow outputs[6]. Equations (1) and (2) show the terms for difference and borrowing.

difference and borrow expressions.

$$Difference=A\oplus B \oplus C \quad (1)$$

$$Borrow=A'C+A'B+BC \quad (2)$$

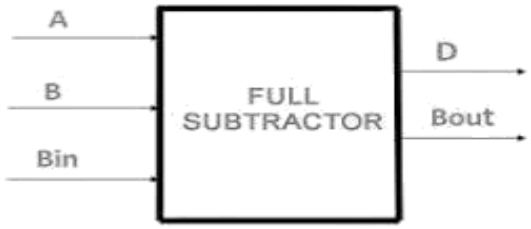

Fig 1 : full subtractor block diagram.

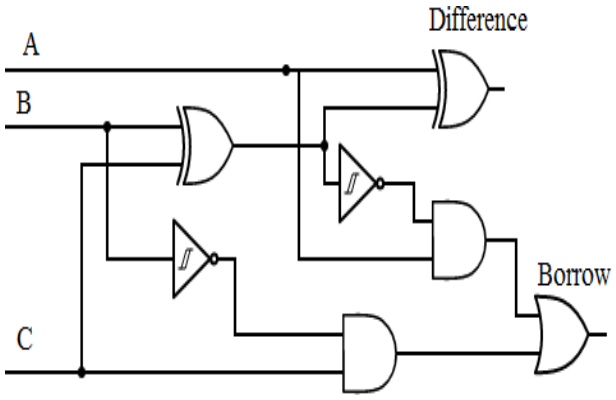

Fig 2 :full subtractor logic circuit diagram

IV. EXISTING SYSTEM

Using an initial logic circuit design and power consumption of 70.568 uW, a full subtractor to construct a micro wind tool was implemented**.**

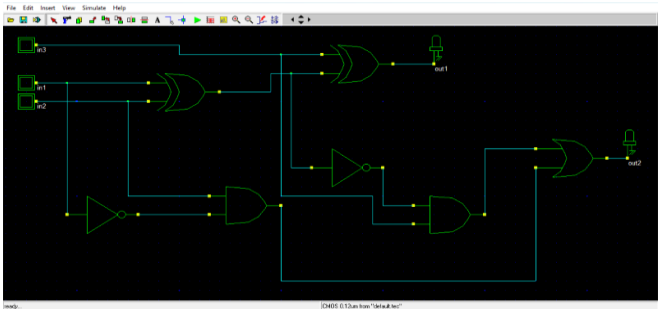

Fig 3: full subtractor logic circuit

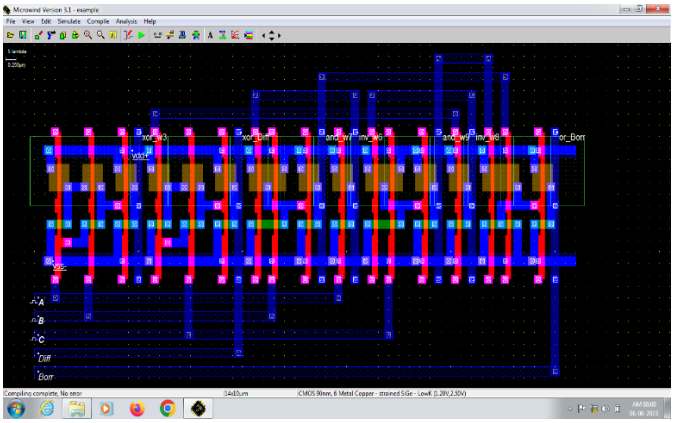

Fig 4: full subtractor layout design.

Reduced power VLSI design is valued by contemporary VLSI technology. The use of high power in the design results from the use of low power VLSI in the following stage to simulate a full subtractor design. The simulation results are shown below.

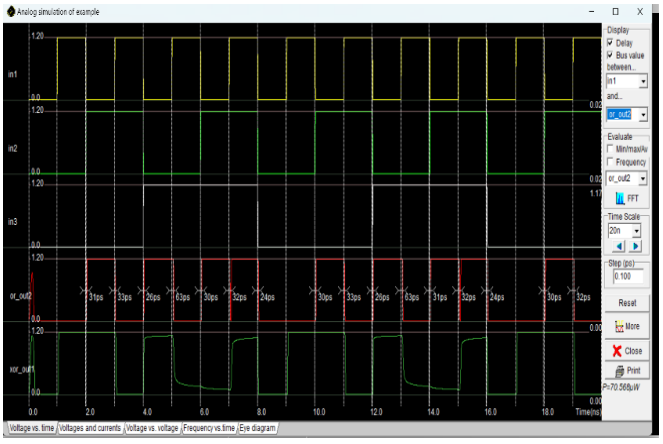

Fig 5 : full subtractor simulation output.

The simulation produces a full subtractor using high power as its output. We can now design a low power VLSI in adiabatic logic that used a design and construct a circuit methodology.

IV. PROPOSED SYSTEM

This paper's primary argument is founded on split level charge recovery theory (SCRL). [7] With a typical CMOS circuit, during a switching event, energy is transferred from the supplied power to the output or there is a transfer of charge from of the output to a ground terminal. The complete subtractor is a gadget that is intended for micro wind. Following analysis and implementation, an SCRL complete subtractor was used [7].

The fundamental issue with modern circuits is energy efficiency. This is made possible by the circuits' low power consumption and dissipation. the amount of energy lost during the load capacitor's discharge. In regard to power reduction, CMOS was crucial. this is primary motivation in a paper.

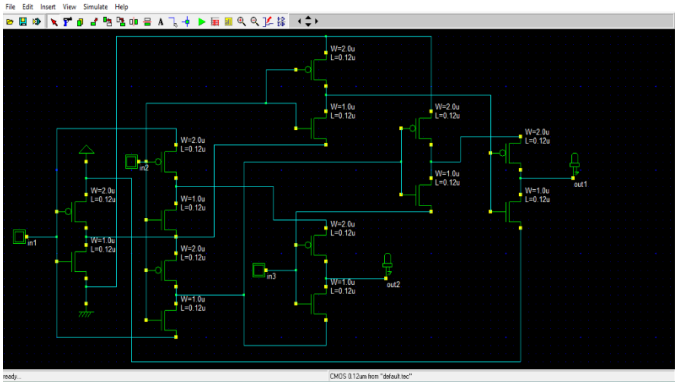

Fig 6 : full subtractor circuit in SCRL used .

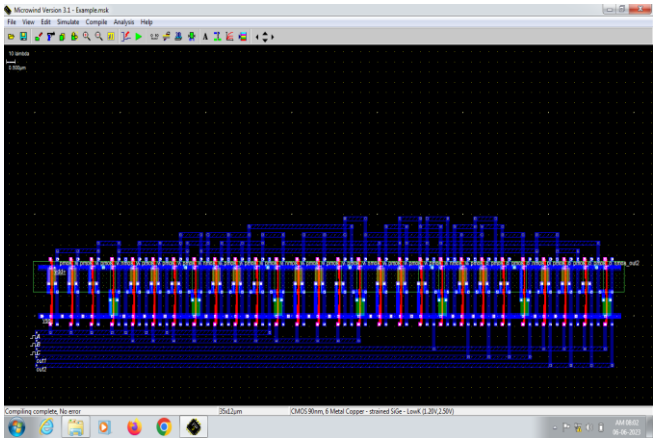

Fig 7 : full subtractor SCRL usinglayout design..

To create an EDA tool, the differences as well as borrowed logic circuits were schematically combined. Next, SCRL logic uses adiabatic logic to implement and analyze a circuit.

Combinational circuit

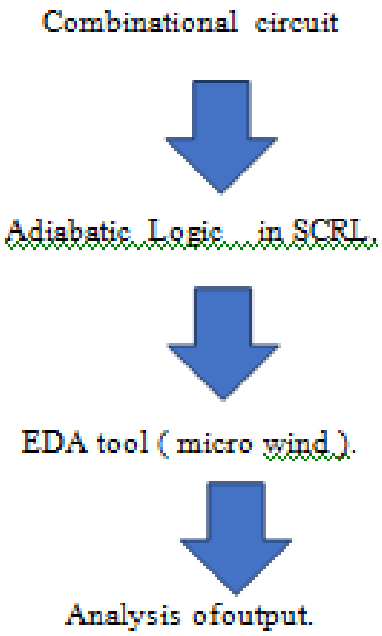

Fig 6 : Concept of proposed system

VI. SIMULATION AND RESULT

At the circuit and logic level, adiabatic techniques based on the energy recovery concept are one of the creative ways to reduce power. In this work, a full subtractor in SCRL logic was designed using an adiabatic logic design approach. Micro wind is used to create and simulate the logic.

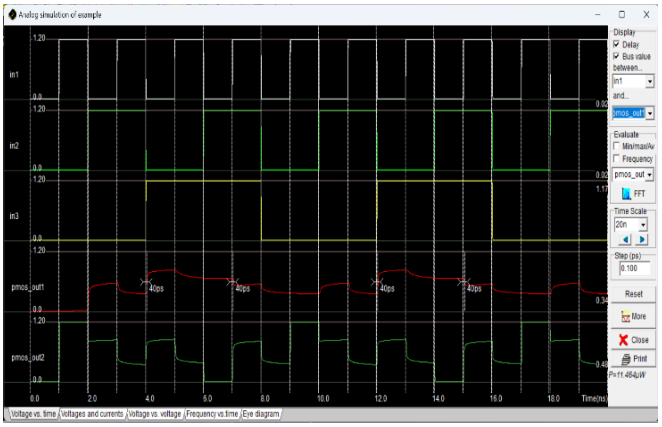

Fig 8 : simulation output of with adiabatic logic.

The total power utilized in P = 11.464 uW after the power consumption in a full subtractor circuit was successfully lowered.

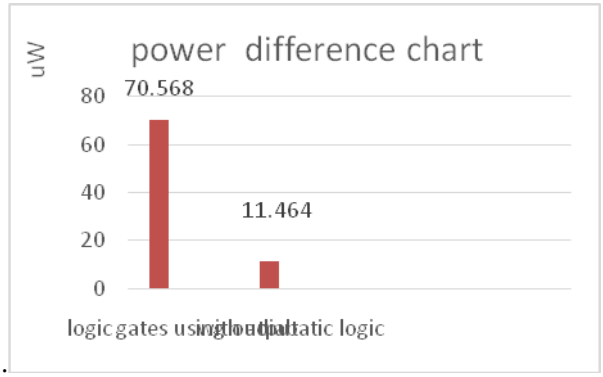

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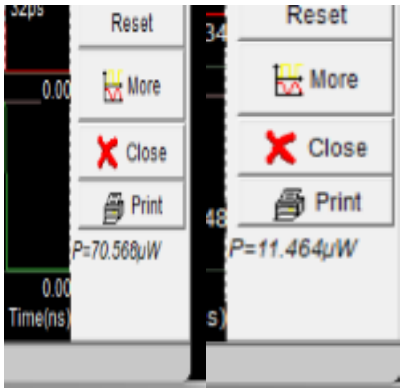
Fig.9: Comparison of Different power using chart.



a b

a - without adiabatic logic power utilization .
b - with adiabatic logic power utilization .

V. CONCLUSION

This paper described how a full subtractor was designed using a variety of adiabatic methods. All of the circuits that have been designed have been simulated and subsequently examined for various performance metrics. It is clear from the design that, when compared to other full subtractors available in the literature, the proposed full subtractor based on the SCRL technique has shown a significant improvement in power consumption,. Thus, despite having a greater number of transistors, the proposed subtractor had also demonstrated its ability to conserve energy. We can therefore draw the conclusion that adiabatic logic is a superior technology with good potential in low-power applications.

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