Fault Tolerant Reversible of Various Adders Using Different Low Power Consumption Techniques

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Abstract- *GDI technique allows minimization of area and power consumption of digital circuits. The reversible gate preserves same parity between output and input vectors is called fault tolerant but the dimension should be 3. In this design, Peres Gate is designed using Gate Diffusion Input using 8 transistors. The proposed new Peres Gate is used to design full adder with power efficient and fault tolerant. In this work power consumption 51.62µW is achieved for supply voltage 1V and the total area is 492µm2. The schematic is designed in DSCH 2 and layout is done in Microwind 2.*

Keywords- Peres Gate, Reversible Logic Gate, Low Power, Gate Diffusion Input(GDI), Full adder, 120nm Technology, Microwind 2, DSCH 2.

I. INTRODUCTION

In VLSI digital circuits, power and area reduction is the important parameter which decides the efficiency of the circuit [1] [4]. Power consumption is the primary factor in high performance computing application, Image processing applications.

The author R. Landauer has said that to compute irreversible A logic, kTln2 joules of heat energy generates per bit information lost[2]. The author Bennett said that by using reversible logic can eliminate of kTln2 energy dissipation[3].

Another one design technique known as Gate Diffusion Input (GDI) style that replaces CMOS logic and it was developed for fabrication in SoI and twin-well CMOS process.

II. LITERATURE WORK

a. GDI Technique

The GDI [5] is power power and area efficient methodology to design. The structure of GDI cell is shown in fig.1. This structure having 4 terminals G, P, N and D as shown in fig.1. G is the common input between nMOS and pMOS, N and P are diffusion nodes. Here G, P and N acts as inputs and D acts as an output.

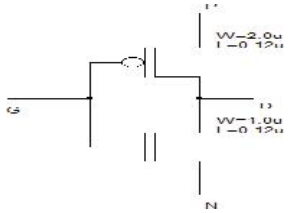


Fig.1. Gate Diffusion Input(GDI) Cell

b. Reversible Logic Gate (PERES Gate)

In reversible logic, numbers of inputs are equal to number of outputs and reversible logic circuits are having one to one mapping. The fig.2 shows the symbol of Peres Gate (PG)[6].Thisishaving3inputsand3outputs.Theoutputequationsa relistedin equations(1),(2)and(3).

P= A (1)
Q= A⊕B(2)

R=AB⊕C

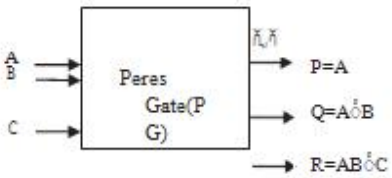


Fig.2.PeresGate

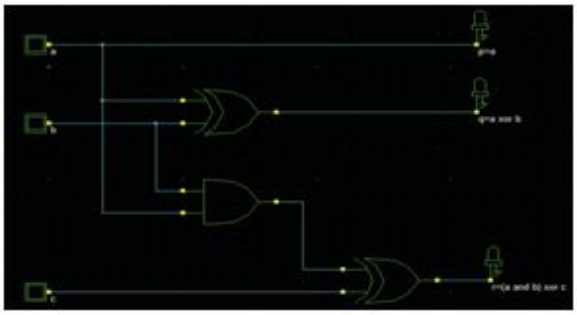


Fig.3.InternalStructureofPeresGate

We have also implemented the existed Peres Gate using Logic Gates to express the internal structure as shown in fig.3. In proposed work, we have designed Modified Peres Gate using Gate Diffusion Input with less number of transistors.

III. PROPOSED WORK

To ensure all the digital devices be more efficiently working by designing in way that the speed is high and power is conserved by scaling down power dissipation.

Slower operation in PTL due to reduced current drive. Due to direct path static power consumption will increase, it leads to latchup problems and in CMOS technology the numbers of transistors are required more. Slower operation in PTL due to reduced current drive. Due to direct path static power consumption will increase, it leads to latchup problems and in CMOS technology the numbers of transistors are required more. To overcome this problem, the Gate Diffusion Input technique is proposed reduce number switching activities as well as power consumption. The GDI technique uses less number of transistors and reduces the area. In this design, we have designed Peres gate using Gate Input Diffusion using 8 transistors is shown in fig.6.The proposed new Peres gate is used to design full adder with power efficient and fault tolerant using reversible logic gates is shown in fig.7. In this design first we have designed 3T XOR gate and 2T AND gate [1]. Peres gate is also comes under parity preserving reversible gates because it satisfy the following equation (4) and feedbacks, fan outs are not allowed in this reversible logic.

$A \oplus B \oplus C = P \oplus Q \oplus R$ (4)

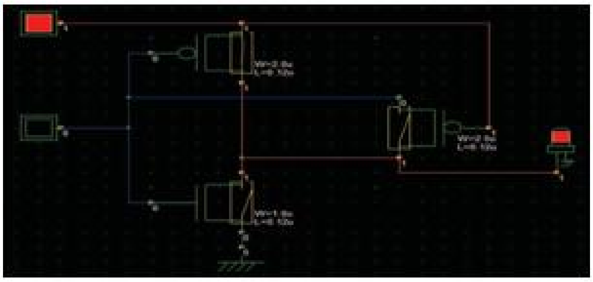


Fig.4. 3T XOR gate using GDI technology [1]

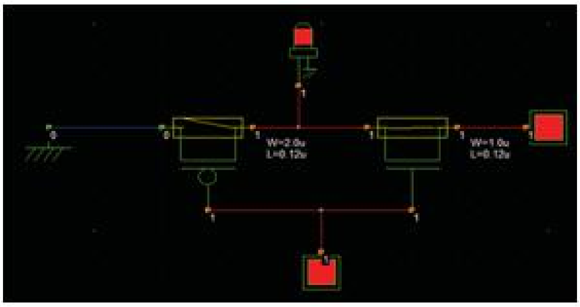


Fig.5.2 TAND gate using GDI technology

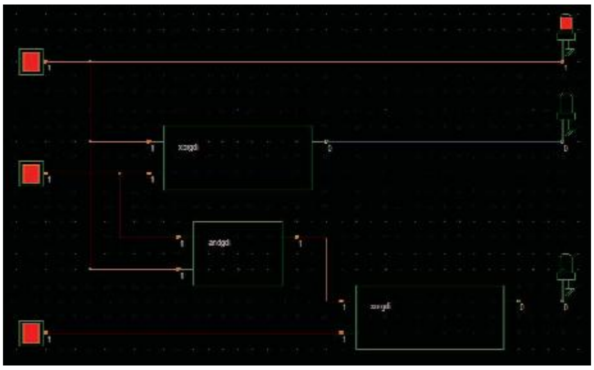


Fig.6.Peres gate using GDI Technology

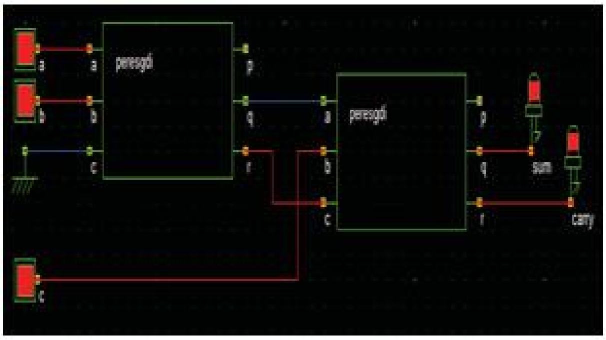


Fig.7(a).FulladderusingmodifiedPeresgate

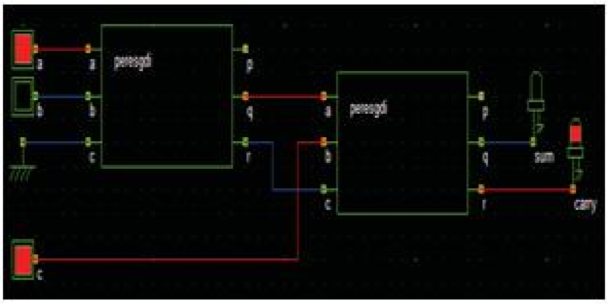


Fig.7(b).Full adder using modified Peres gate

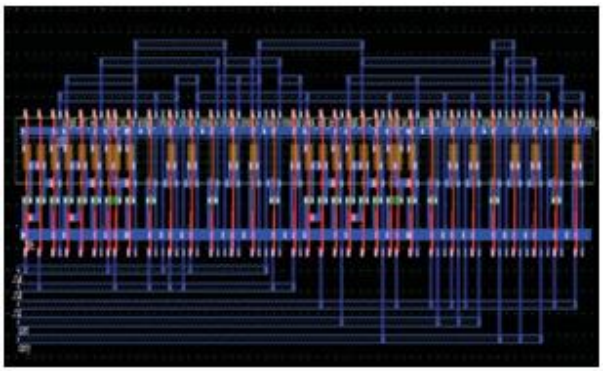


Fig.8.Layout of Full adder using modified Peres gate

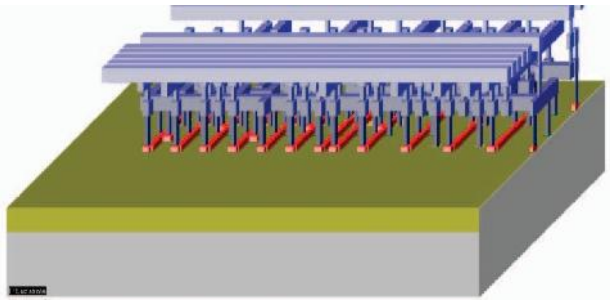


Fig.9. 3D Process of Full adder using modified Peres gate

IV. RESULTS

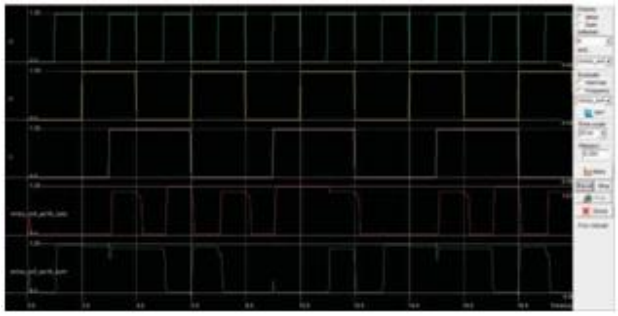


Fig.10.Simulation results with supply voltage 1.2V

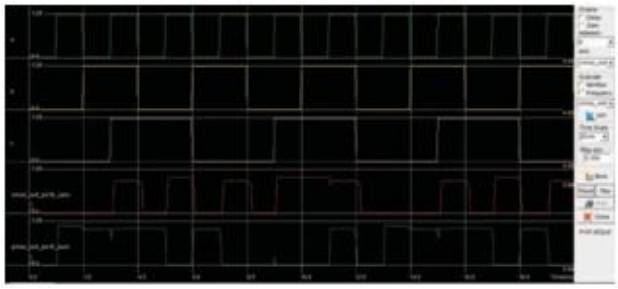
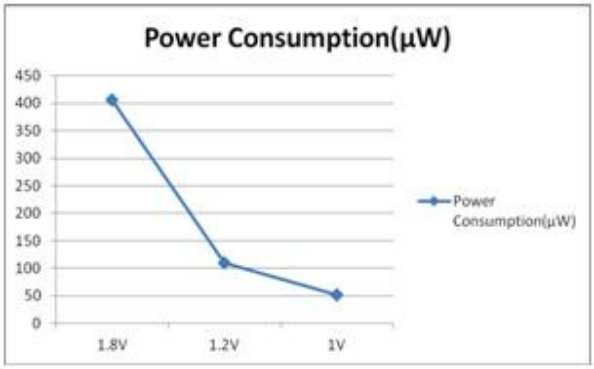


Fig.11.Simulation results with supply voltage 1.0V

Fig.12.Area analysis layout width=41µm and length=12µm

Table1:Power Analysis of Full adder using modified Peres gate with voltage scaling

S.No.	Supply Voltage	Power Consumption
1	1.8V	406µW
2	1.2V	110µW
3	1.0V	51.62µW



Graph 1.Power Analysis of Full adder using modified Peres gate with voltage scaling

Area Analysis:

The proposed full adder layout width is 41 µm and length is 12µm. The total area is 492µm^2.

V. CONCLUSION

In this design, Peres Gate is designed using Gate Diffusion Input using 8 transistors. The proposed new Peres Gate is used to design full adder with power efficient and fault tolerant. In this work power consumption 51.62µW is achieved for supply voltage 1V and the total area is 492µm^2.

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