Timing -Error -Tolerant

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Abstract- *the timing error is now getting increased attention because of high rate of error occurrence on semiconductor. In this paper, the clock controlling system is used in flip-flop to prevent the timing error. Timing error would be detected and corrected by only modifying the clock of flip-flop without changing the system clock with minimum logics. In this project we going to compare timing dilution method &timing borrow techniques.*

Keywords- timing error, semiconductor, clock ,timing dilution, timing borrowing.

I. INTRODUCTION

The timing-error rate is increased because the clock frequency is increased. The timing error occurs due to the delay in combinational circuits that are located in between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly.

To deal with the timing error, many related methods have been proposed One of the representative methods of timing-error-tolerant systems is the temporary error-detection system

Another existing system that corrects a timing error by borrowing time has been presented, which also does not require an additional clock for the correction of the timing error. It has a timing violation predictor that can detect the violations on the halfway of the critical path.

After an error is detected, the system controls the flip-flop to become a transparent state. While the system can avoid the penalty of the clock, it requires a large amount of hardware, such as an additional flip-flop and latch. Furthermore, since the location of the halfway of the combinational circuits is inaccurate and it is hard to be chosen, the transparent window can be made erroneously.

In this project, we propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. In the critical path, the abnormal data transition after that the rising edge of the clock which have been caused by a timing error, is detected and corrected by controlling the transparent window of the clock. The timing error which would corrected directly through a minimum number of logics. Furthermore, our time-borrowing method that copes with the successive errors are introduced. If the timing error occurs in two stages successively, modified CLK in the second stage maintains a transparent window for enough time to make normal data be stored without changing system CLK.

II. EXISTING SYSTEM

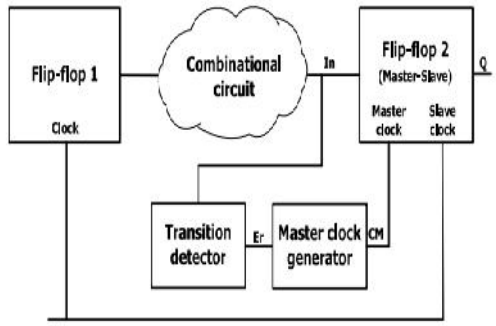
In this existing system they had used many types of error detection method among that dynamic flip-flop conversion system is taken as the existing approach.

The circuit is composed of one timing violation predictor, one data-arrival detector, and the original flip-flop. The dynamic flip-flop conversion system has 430% hardware overhead since the additional hardware consists of 68 transistors. Compared with the power overhead of the other methods, the proposed system requires less power overhead than other existing methods.

METHOD	AERA OVERHEADED	POWER OVERHEAD
PROPOSED SYSTEM	175%	24%
Dynamic flip-flop conversion system	430%	36%

III. PROPOSED SYSTEM

A new timing-error-tolerant system that can correct a timing error is developed. When a timing error causes a delayed arrival of an input on a flip-flop, the proposed system can detect a delayed input of the flip-flop, and the flip-flop passes through the data by making a transparent window.



[1] The proposed system consists of a "transition detector" and "master clock generator." The "transition detector" detects the input transition of a flip-flop, and it produces a pulse of the error-flagged signal. According to the FIG It Based on the output of the transition detector, the "master clock generator" produces a pulse for a certain period only when a clock is high.

While a pulse is "1," the flip-flop passes the input to the output since the pulse makes a transparent window by controlling a clock of master in the flip-flop. Thus, the abnormal data that are stored in the flip-flop can be restored with delayed normal data. To avoid hold time violation, a pulse is generated with a minimum time, which is required for the setup time.

Using the information acquired from the timing analysing tool, the critical paths of the circuit and the setup-time information of each element in the circuit are determined.

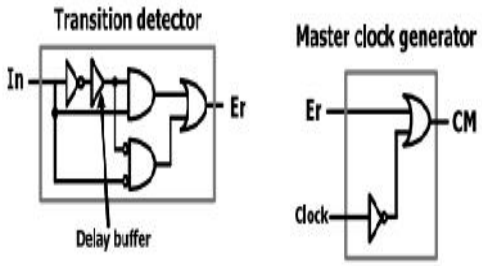


FIG:INTERNAL STRUCTURE OF TRANSITION DETECTOR AND MASTER CLOCK GENERATOR

We make full use of such results to choose the best location for our proposed system. If a single-stage error occurs, in the delayed arriving data signal is recovered because the master latch is transparent for the pulse period.[1] However, if a successive-stage error occurs due to the lack of setup time in the second-stage flip-flop, the delayed arriving data signal in the second stage cannot be stored because of the setup-time violation. To deal with the successive-stage error, we devised the time-borrowing technique. The time-borrowing circuit is provided in the second stage,

(1) Proposed timing-error-tolerant system with time-borrowing techniques:

In this article, we propose a timing-error-tolerant method that can detect and also correct a timing error immediately through a simple mechanism. by using a Time borrowing Circuit In this critical path, the abnormal data transition after that rising edge of the clock, which would have caused by a timing error, is controlled and detected by controlling the Transparent window of the clock.

The timing error is corrected directly through a minimal no.of. Logics. Likewise, our time-borrowing system that copes with the successive errors is introduced as shown in the block diagram

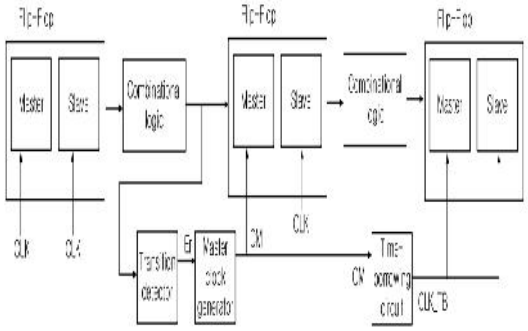


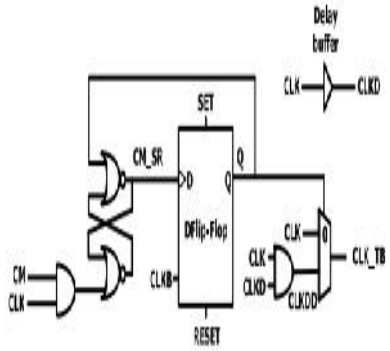
FIG : PROPOSED SYSTEM BLOCK DIAGRAM

The timing error is corrected directly through a minimal no,of. logics. Furthermore, our time borrowing method that copes with the successive errors is introduced. If the timing error, which may occurs in two stages consecutively, modified CLK in the alternate second stage maintains a transparent window for enough time to make normal data be stored without changing the system CLK. we can observe that two clocks were being used they are CLK is(System clock) and CLK_TB was(Time borrowed clock).

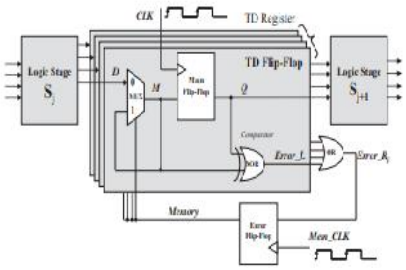
Time borrowing techniques:

When a timing error occurs on the input data of the first stage, the CM signal is set to "1," which also induces the CM_SR high level. After CLK is fallen, Q is set to "1." While the Q signal sets the high period, the delayed CLK (CLKDD) is chosen as the main CLK for the second stage. After all, the new CLK maintains a transparent window for enough time. A CM is high for a certain period of time after a timing error occurs.

Thus, the delayed data can be stored as normal data.The time-borrowing scheme can be used on any location that has a short setup time for the flip-flop.



(2) Time Dilation Technique:



This topology utilizes a multiplexer (MUX)& XOR gate per system Flip-Flop which (Main FlipFlop) to provide timing error detection and correction of the capabilities.

After error detection the logic evaluation time is extended by a clock cycle for error correction, by re-feeding the Main Flip-Flop with the correct and valid data of the MUX-latch.In the fault free case, the data arrive in time at the D input of the TD Flip-Flop, they propagate to the M input of the Main Flip-Flop and they are captured at the Q output by the triggering edge of the clock signal CLK.

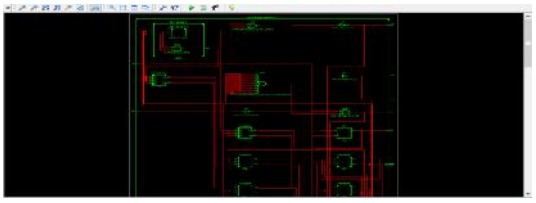
IV. CONCLUSION

We propose a timing-error-tolerant method that can correct a timing error immediately with a compact circuit structure. By using the simple mechanism of time borrowing method and dilation method timing error has been deled. Comparing to other method of timing error tolerance the time borrowing techniques and the time dilation techniques were using minimal no.of.logics to process

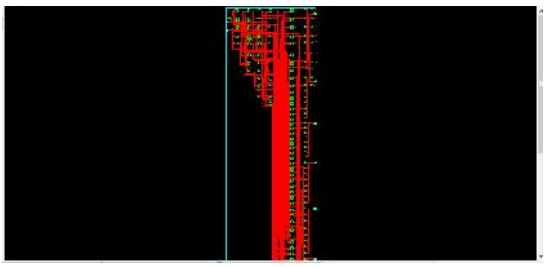
V. SIMULATION

- **Time borrowing techniques:**

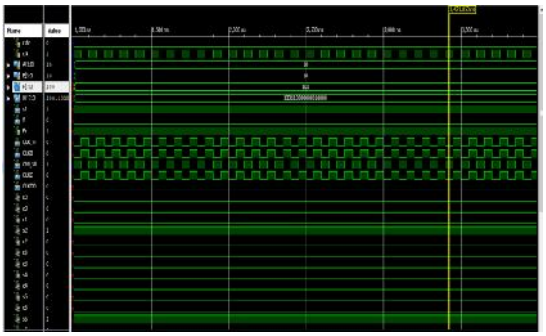
(1)TIMING BORROW TECHNIQUES RTL:



(2)TIMINGBORROWTECHNIQUES LUT

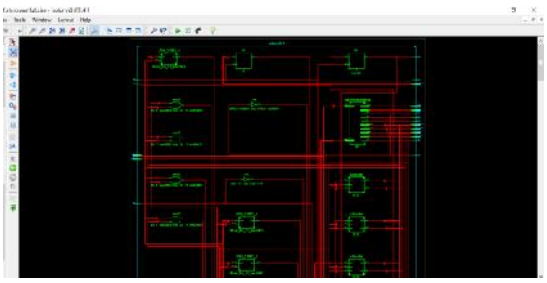


(3)TIMING BORROW TECHNIQUES SCHEMATIC

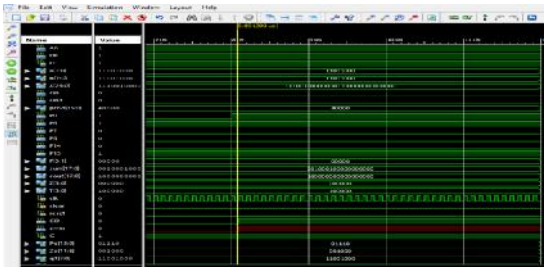


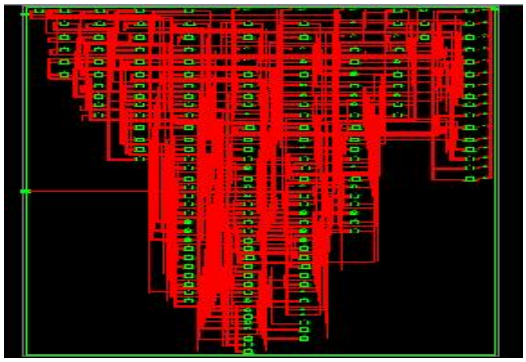
- **Time Dilation Technique:**

RTL:



SCHEMATIC:





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