Single Phase Five Level Inverter With One Leg Control Strategy

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Abstract- *There is a rapid growth in the usage of technology pertaining to power inverter with reduced harmonics. Investigations were conducted by researches for reducing its harmonics for decades. This led to the five-level inverter development. It periodically studies with numerous switches of power semiconductor which in turn increases its complexity of control. The paper deals with simulation and execution of hardware for controlling the one leg methodology for the design of five level inverter (single phase) with productive switch control worked at line frequency for attaining demands at higher level.*

Keywords- One leg, Multilevel inverter, single phase, nine-level.

I. INTRODUCTION

Inverter is a basic circuit that converts dc power to ac power at required voltage and frequency. For example, I am giving dc voltage (that is unidirectional) to the inverter, I will be getting sinusoidal waveform at the output in the ideal case. Multilevel inverters are gaining huge attention for medium voltage and high power applications. There are many topologies or levels for MLI but still many other topologies are under research because day by day industry application is changing and based on those applications what best topology we have for that MLI that is still under research.There are three topologies of level, the first topology is diode clamped [1], second is capacitor clamped which is also called flying capacitor [2] and third category is cascaded H-bridge inverter [3]. It can be symmetrical or it could be asymmetrical. In fact, flying capacitor can be symmetrical or asymmetrical. An H-bridge is built of four switches, that controls the flow of current to a load. It looks like letter H, so it is named as H-bridge. Number of levels at the output of H-bridge depends on state of switches. Half part of H-bridge is half bridge.

However, in a multilevel inverter there are much more level by increasing the number of levels at the output, we try to make the waveform more near to the sinusoidal waveform. By increasing the number of levels, we are reducing the harmonic content in the waveform [4,5]. This is the major benefit of using the MLI. In multilevel inverter we are trying to create smoother stepped output. It gives you extremely low distortion, it means increase in the number of steps waveform is becoming more and more sinusoidal because of that harmonic content is reduced. It has lower dv/dt [6,7]. Multilevel inverter have high voltage operation capability that means they can give you different voltage level, we can increase the voltage at the output by small voltages at the input side.

II. PROPOSED SYSTEM

A. The proposed topology is described below

This is the simple circuit diagram of single phase five level inverter. It consists of five switches from S1 to S5, one diode, one resistive load and two dc sources. Here we have used Mosfet as a switch. we are much interested to know about potential. To know this we have few modes of operation. In our proposed system we have five modes of operation let's see one by one. we need to cascade two H-bridges to get five level at the output, but in our proposed system we have used only one H-bridge to get three level at the output and we have used extra one mosfet switch to get five level at the output.

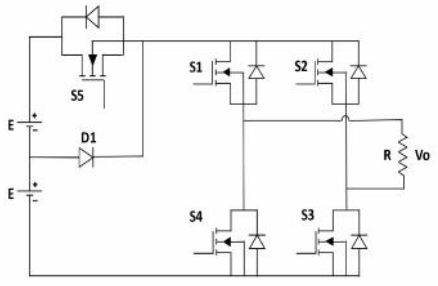

Figure 1: Circuit of proposed five-level inverter

B. Description of voltage levels switching states

The operation mode 1

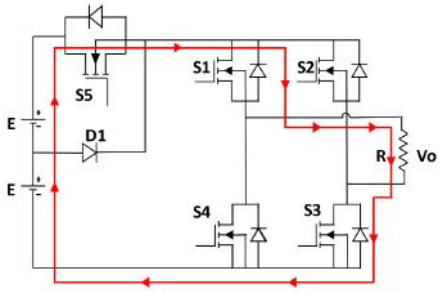

Figure 2:Conduction Mode 1

In this mode of operation, the switches S1, S3, S5 are in ON states. The Two DC sources are in series connection and so voltage across the load is 2E.

The operation mode 2

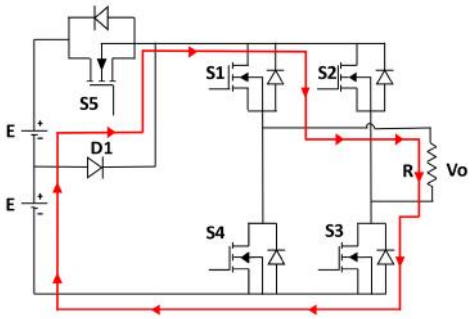

Figure 3:Conduction Mode 2

In this mode of operation, the switches S1, S3 are in ON states. The positive of the supply is connected to diode D1 and negative of the supply is connected to switch S3 and voltage across load is E.

The operation mode 3

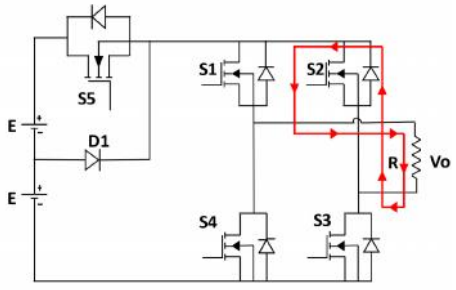

Figure 4:Conduction Mode 3(a)

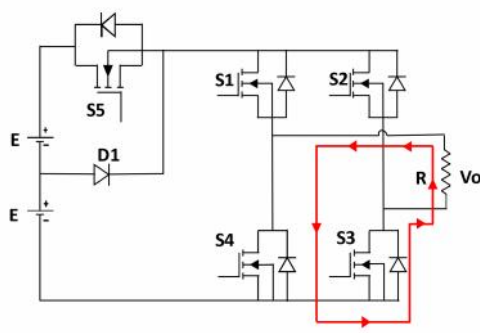

Figure 5:Conduction Mode 3(b)

In this mode of operation, there are two cycles positive and negative cycles. In positive cycle the switches S1, S2 are in ON states. In negative cycle the switches S3, S4 are in ON states. The circuit is not closed. This is completely disconnected from the power supply. There will be no voltage appearing across the load.

The operation mode 4

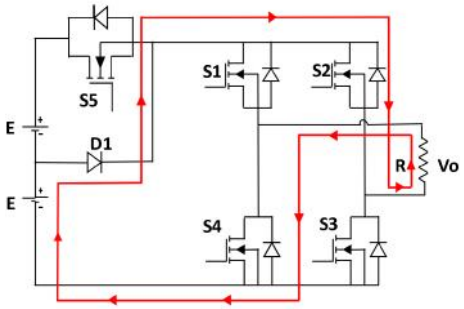

Figure 6:Conduction Mode 4

In this mode of operation, the switches S2, S4 and diode D1 are in ON states. The positive of the supply is connected to diode D1 and negative of the supply is connected to switch S4 and voltage across load is E. The point to be noted here is that the load voltage of mode 2 and this mode is same but differ only in direction.

The operation mode 5

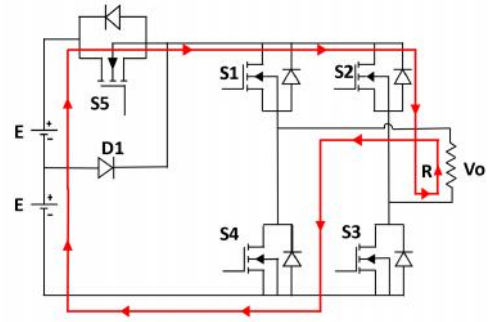

Figure 7:Conduction Mode 5

In this mode of operation, the switches S1, S2, S5 are in ON states. The negative voltage will be appearing across the load that is -2E. The point to be noted here is that the load voltage of mode 1 and this mode is same but differ only in direction.

c. switching states

S1	S2	S3	S4	S5	D1
1	0	1	0	1	0
1	0	1	0	0	1
0	1	0	0	0	0
0	0	1	0	0	0
0	1	0	1	0	1
0	1	0	1	1	0

Table 1: switching states of proposed inverter

C.Switching logic circuit

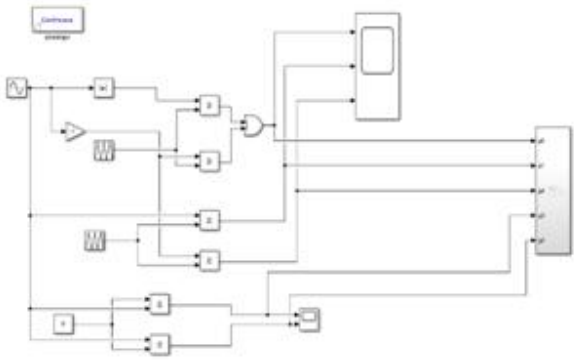

Figure 8:Simulink model for switching logic implementation

Firstly, sinusoidal wave is fed into absolute value to get the positive cycle of the sinewave and the it is compared with carrier wave. The gain -1 and carrier wave is compared. After comparison both the outputs is fed into OR GATE to get gate pulse for switch S5.

The constant 0 is compared with sinusoidal wave to get gate pulse for switch S2 and S3.

The sinusoidal wave is compared with carrier wave, the output after comparison is fed into the switch S1 and S4.

D. Input pulses to the switches

The repeating sequence that is being compared with the sinewave to get the desired pulse(S1 and S4). The repeating sequence is obtained by setting the time values as [0 5e-5 1e-4] and Output values as [0 0.5 0]. This is the pulse fed into switch S1. It is obtained by comparing the sinewave with high frequency carrier wave (CR 1). Input pulses for S2 and S3is obtained by comparing the sinewave with constant 0.The sinusoidal wave is fed into absolute value to get the positive cycle of the sinewave and the it is compared with repeating sequence. This repeating sequence is obtained by setting the time values as [0 5e-5 1e-4]and Output values as [0.5 1 0.5]. The gain -1 and repeating sequence is compared. After comparison both the outputs is fed into OR GATE to get gate pulse for switch S5.

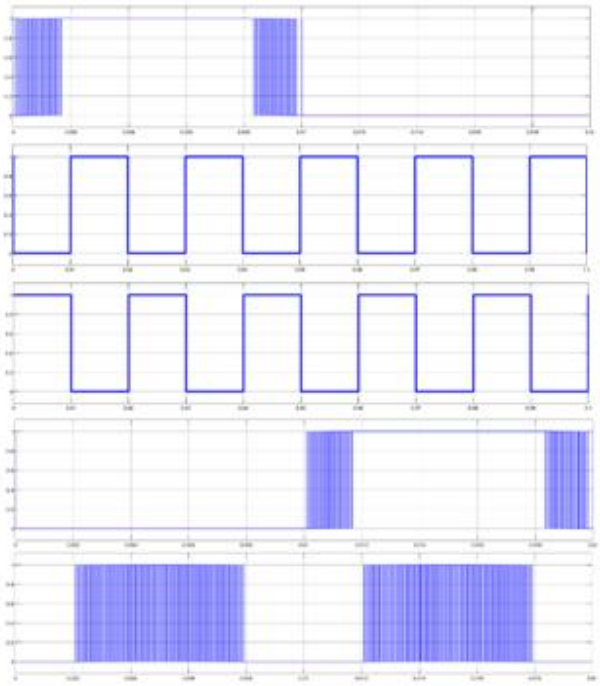

Figure 9:Input pulses to the switches from S1 to S5

E. Input pulses to the switches

We will discuss the simulation diagram of the single phase five level inverter and its output waveform.

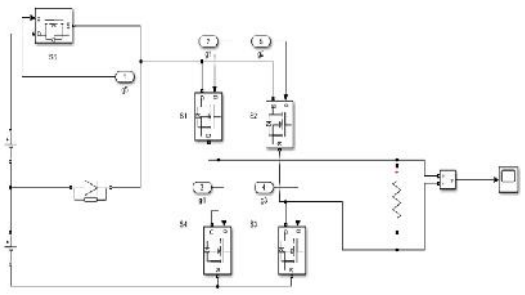

Figure 10:Power circuit for the five-level configuration

III. RESULT AND DISCUSSION

A. *Simulation results*

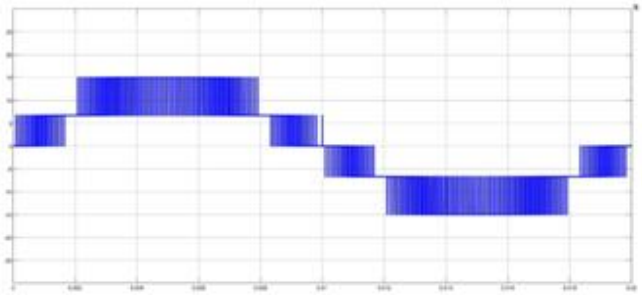

Figure 11:Simulation result of output voltage

This is the output voltage waveform obtained from our proposed system. The output waveform of five levels as shown in the figure. The input DC voltage fed into the inverter is 15 Volts and the peak value of the obtained five level voltage waveform is also 15 Volts.

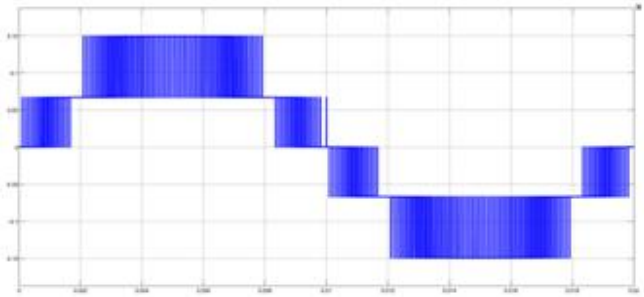

Figure 12:Simulation result of output current

This is the output current waveform obtained from our proposed system. The output waveform of five levels as shown in the figure.

B. *Experimental Results*

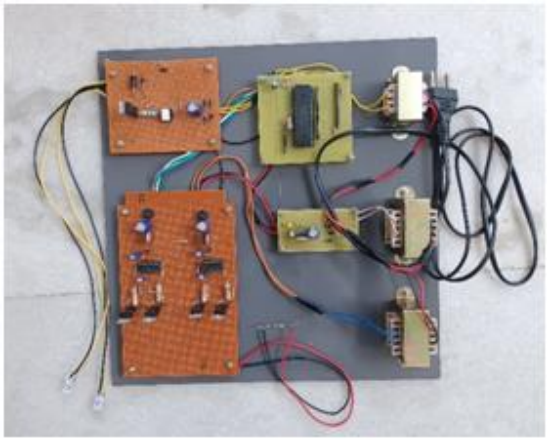

Figure 11:Complete hardware module

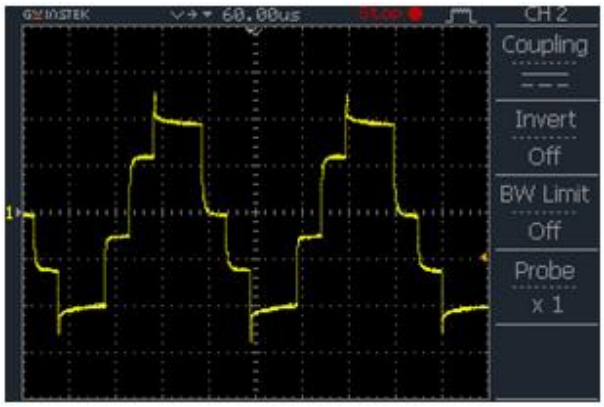

Figure14: Five level inverter output voltage waveform

The Fig. 14 shows the output voltage waveform for the hardware of the proposed single phase five-level inverter.

IV.CONCLUSION

The strategy for one leg control in five-level inverter (single phase) demonstrated in the paper includes 3 levels of excessive switching frequency on advantageous value. By using this approach, the losses in switching are likely to get appropriately decreased.

V. ACKNOWLEDGMENT

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