Single Dc Source Nine-Level Switched Capacitor Boost Inverter Topology

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Abstract- *Using a single dc source and two switched capacitors, this study provides a novel boost inverter structure with a nine-level output voltage waveform. Because the capacitor voltages are self-balancing, there are no sensors or extra circuitry. The output voltage is twice as high as the input voltage, obviating the need for an input dc boost converter, particularly when the inverter is fueled by renewable energy. By contrasting contemporary and classic inverter topologies, the virtues of the suggested topology in terms of the number of devices and cost are highlighted.*

Keywords- Multilevel inverter, capacitor voltage balancing, boosting, nine-level.

I. INTRODUCTION

Multilevel inverters (MLIs) have emerged as a possible solution for medium and high voltage/power applications that demand high-quality dc-ac power conversion. The neutral point clamped (NPC), flying capacitor (FC), and cascade H bridge (CHP) topologies are the most common MLI topologies. Such topologies have been extensively studied and are well-proven in practical applications. However, for the next number of output levels, the number of components required for NPC and FC will increase. In order to reduce the number of dc voltage sources, topologies with switched capacitor (SC) units are proposed. The SC unit has been employed in a variety of configurations, resulting in a variety of output voltage levels. A nine-level output voltage waveform may be achieved with two dc voltage sources and two capacitors, however the structure lacks input voltage boosting. Taking these considerations into account, this study seeks to synthesis a nine-level voltage using the SC technique to reduce the component count. The following are the main characteristics of the proposed MLI:

1. One dc source is employed.
2. Self-voltage balancing is achieved across the capacitors.
3. The output voltage is twice the input voltage.
4. The capacitor voltages are independent of the load power factor and modulation index.

II. PROPOSED SYSTEM

A. The proposed topology is described below

The suggested single-phase SCMLI topology is depicted in Fig.1, along with the highest voltage stress across each switch as an element of the input dc voltage source, i.e., V_{dc}. A total of ten switches makes up the proposed topology. The switches are usually IGBT or MOSFET, depending on the converter's frequency of operation, voltage, and power rating. The dc supply voltage is split in half using two capacitors, C_1 and C_2. The capacitor voltages are kept at half the provision voltage, i.e., $V_{dc}/2$, by turning the switches ON and OFF in a systematic and consecutive manner. With a voltage boosting factor of twice, the suggested topology generates nine levels over the load. The proposed topology's switching table, as well as the modification of capacitor voltages V_{C1} and V_{C2} given in the below Table 1.

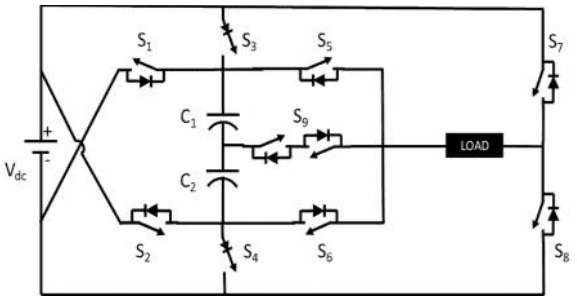


Figure 1: Circuit of proposed nine-level inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	V0	Vc1	Vc2
0	0	1	1	0	1	0	1	0	0	C	C
0	0	1	1	0	0	0	1	1	Vdc/2	C	C
0	0	1	1	1	0	0	1	0	Vdc	C	C
0	1	0	0	0	0	0	1	1	3Vdc/2	--	D
0	1	0	0	1	0	0	1	0	2Vdc	D	D
0	0	1	1	1	0	1	0	0	0	C	C
0	0	1	1	0	0	1	0	1	Vdc/2	C	C
0	0	1	1	0	1	1	0	0	-Vdc	C	C
1	0	0	0	0	0	1	0	1	-3Vdc/2	D	--
1	0	0	0	0	1	1	0	0	-2Vdc/2	D	D

Table 1: Switching states of the proposed inverter

B. Description of voltage levels

The proposed design generates nine layers across the load. In this section, the blocking voltages of all non-conducting switches are reported for all five levels in the positive half cycle, as shown in Fig. 2 (a)-(e).

(i)State i (Zero voltage state): The capacitors C_1 and C_2 are made to charge to their peak voltage in this voltage state, as shown in Fig. 2 (a), by connecting them directly across the dc voltage source. Turning on the switches S_3 and S_4 accomplishes this. In the case of an inductive load, the load terminals are shorted and a path for current flow is given by turning on the switches S_5 and S_7.

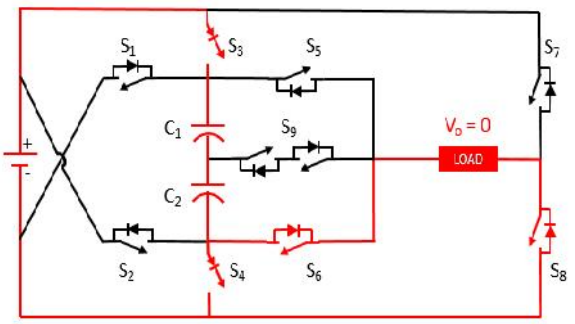
(ii) State ii ($+V_{dc}/2$): Switches S_5 and S_7 are turned off by pressing S_8 and S_9. The capacitor voltages V_{C1} and V_{C2} are kept at $V_{dc}/2$ in this state. By turning on the switches, the first voltage state equal to $V_{dc}/2$ develops across the load, as shown in Fig. 2 (b). The dc voltage source V_{dc} is subtracted from the capacitor voltage V_{C1}, which is equal to $V_{dc}/2$.

(iii) State iii ($+V_{dc}$): By turning on switch S_5 and shutting off switch S_9 as presented in Fig. 2, the whole source voltage emerges across the load (c). The voltages of both capacitors are kept at $V_{dc}/2$. Until this voltage condition, the energy is held in both capacitors.

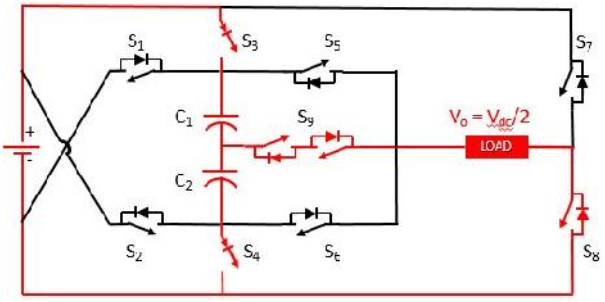
(iv) State iv ($+3V_{dc}/2$): The switches S_3 and S_4 are turned off in this voltage state, and the energy stored in capacitor C_2 is used to create the third voltage state. V_{C2} is the voltage.

(v) By turning on switch S_2, (v) was added to the dc voltage source Vdc. The voltage is held at $V_{dc}/2$ and the condition of capacitor C1 remains unchanged. Figure 2 depicts this voltage state (d).

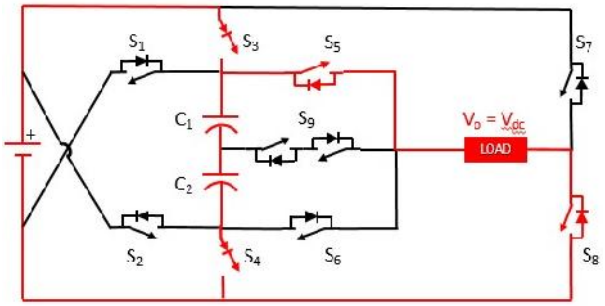
(vi) State v ($+2V_{dc}$): In this voltage state, the energy contained in both capacitors are released, and their voltages are added to the dc voltage source. As seen in Fig. 2, raising the dc voltage source results in $2V_{dc}$ across the load (e).



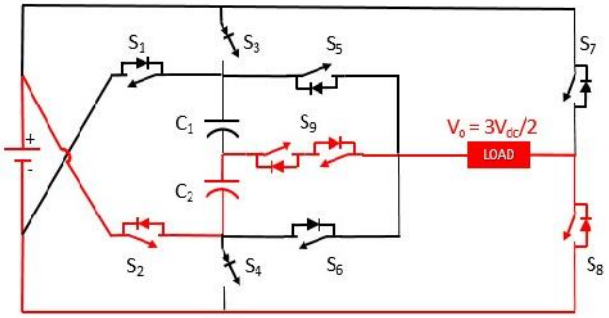
(a)



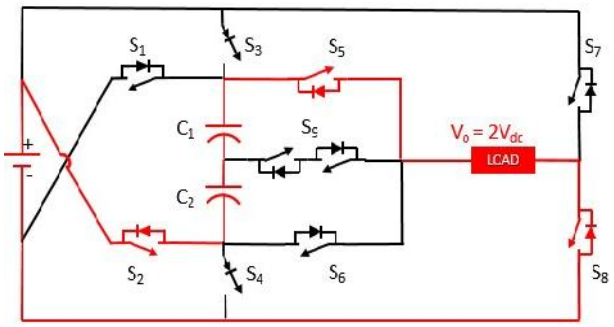
(b)



(c)



(d)



(e)

Figure 2: Positive half cycle voltage states of proposedsystem (a) $V_o = 0$, (b) $V_o = V_{dc}/2$, (c) $V_o = V_{dc}$, (d) $V_o = 3V_{dc}/2$, and (e) $V_o = 2V_{dc}$

The voltage stress across all switches for each level at the output is summarized in Fig. 3. To achieve the boost feature, the switches S_1 and S_2 are cross-connected between the dc voltage source and capacitors. Due to the cross-connection, these switches must block the $2V_{dc}$. In order to prevent the switches S_3 and S_4 from conducting in the boost

mode of operation, they are linked in series with diodes. The bidirectional switch S_9 is required to block half of the supply voltage, and the switches S_3 to S8 are required to block the supply voltage V_{dc}. The voltage stress across all switches for each level at the output is summarized in Fig. 3. Between the dc and the ac, the switches S_1 and S_2 are cross-connected.

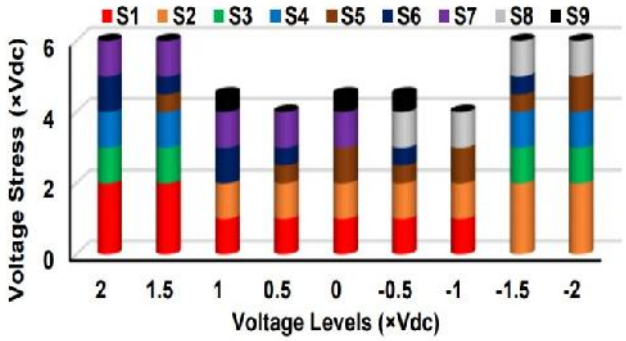


Figure 3: Voltage stress across all switches

C. Modulation Technique

The phase disposition pulse width modulation (PD-PWM) approach was applied for the proposed topology. Four carrier signals of equal magnitude and high frequency were compared with a sinusoidal reference signal V_{ref} with an output voltage frequency in PD - PWM.

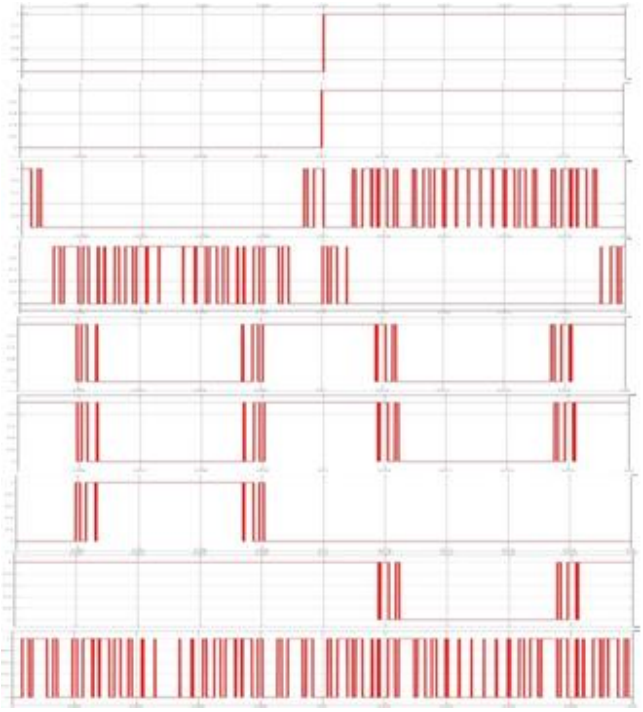


Figure 4: PD-PWM technique with generated gate pulses for all switches consecutively

According to Table I, the comparison yields gate pulses for the switched. Table I was used to determine the logic for the proposed nine-level topology, which was then implemented using logic gates. The unique signals are shown in Fig. 4 based on the switching logic. The modulation index for the PWM in Fig. 4 (b) can be calculated as follows:

$$MI = V_{ref}/4V_{cr} \quad (1)$$

D. Capacitor voltage balancing

One of the key elements of the suggested architecture is the capacitors C_1 and C_2 self-voltage balancing. Both voltages must be balanced, with the output voltage being half that of the input voltage. In terms of charging and discharging patterns across a basic cycle, the capacitors C_1 and C_2 have thebehaviour sameas shown in Table 1. During the voltage levels of zero, $V_{dc}/2$, and Vdc, the capacitors C_1 and C_2 are charged. Figure 5 shows the equivalent circuit during the charging of the capacitors (a). The parasitic resistance of diodes, switches, and equivalent series resistance (ESR) of capacitors are all present in the charging loop. The lower the value of these elements, the smaller the value of the charging loop's time constant RC. The capacitor voltages will be half of the input voltage if the voltage drops of the switches and diodes are ignored.

$$V_1 = V_2 = V_{dc} / 2 \quad (2)$$

During the boost mode of operation, the capacitors are discharged by connecting them in series with the input source at voltage levels of 3Vdc/2 and 2Vdc, as indicated in Fig. 5 (b) and (c), respectively. The fully charged capacitors begin to dissipate their charge, and their voltage falls below Vdc/2. However, when capacitors are discharged, as illustrated in Fig. 5 (b) and (c), the time constant RC is substantially higher than when the capacitors are charged. The capacitors are slowly discharged as a result of this. The voltage across the capacitors rises to Vdc/2 when the next charging condition arrives. As a result, both capacitors charge and discharge for several durations over a whole fundamental cycle, and each capacitor voltage can be maintained at Vdc/2 with some ripple voltage.

III. RESULT AND DISCUSSION

A. Simulation results

MATLAB software was used to simulate the proposed nine-level topology. The varied simulated waveforms for the suggested topology are shown in Fig. 5. The ac output voltage has a peak value of 200V, which when

supplied to a series-connected resistive-inductive load (Z = 50mH + 20) produces a peak current of 6A. The voltage across both capacitors is around 50V, with 45V and 51V as the minimum and maximum values, respectively. In addition, Fig. 6 shows the FFT of the output voltage, which has a THD of 13.5 percent after eliminating all lower-order harmonics. Furthermore, the proposed topology's performance was evaluated using a dynamic load and modulation index (MI).The output voltage, current, and capacitor voltages are shown in Fig. 9 (a) with a load change from a purely resistive load of Z = 50 to a series-connected resistive-inductive load of Z = 50mH + 50. Both capacitor voltages are balanced when the load type is changed, demonstrating that the load type has no effect on capacitor voltage balancing. The MI has been reduced from 1.0 to 0.6, then to 0.4. The number of levels is lowered to seven when the modulation index is 0.6, and to five when the modulation index is 0.4. Both capacitor voltages, however, remain balanced.

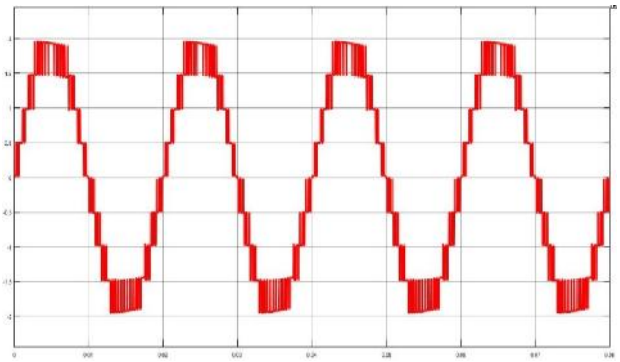


Figure 5: Simulation result of output voltage

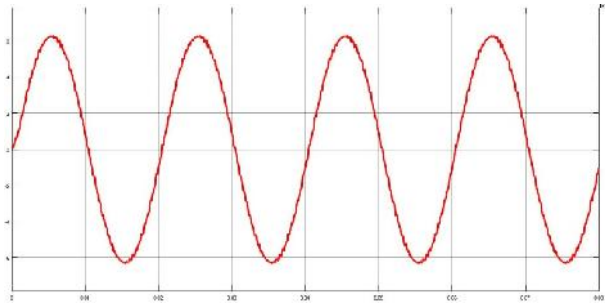


Figure 6: Simulation result of output current

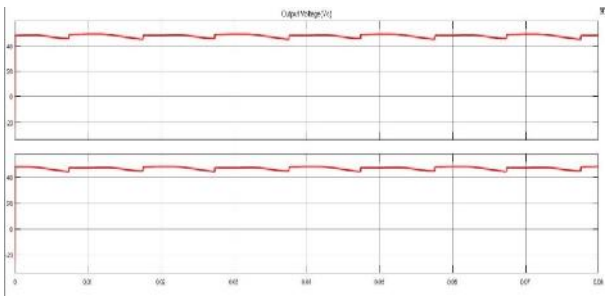


Figure 7: Capacitor voltages

B. Experimental Results

To verify the feasibility of the proposed nine-level topology, a laboratory prototype was developed to carry out the experimental work. The switching frequency of 2.5 kHz has been selected for the PD-PWM. For the experimental results, the magnitude of the dc input voltage source was fixed to 12V. Figure shows the output voltage and current waveform for the connected resistive load with R=10 Ω. One of the main features of the proposed topology has been the twice voltage gain and this has been confirmed by the output voltage, which has a 24V peak resulting from a 12V dc input voltage. In addition, both capacitor voltages are depicted. Both capacitor voltages, i.e., V_{c1} and V_{c2} are well balanced and are equal to half of the dc voltage source, i.e., 6V. The Fig. 8 shown below is the hardware setup.

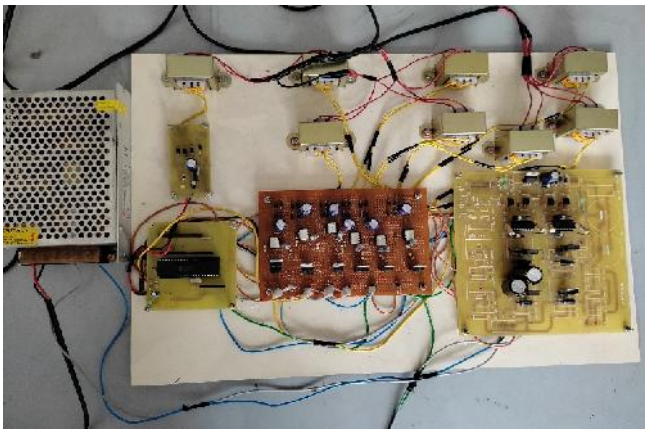


Figure 8: Hardware setup of the proposed topology

Figure 9: Experimental result of the output voltage

The Fig. 9 shows the output voltage waveform for the hardware of the proposed single phase single dc source nine-level inverter.

IV. CONCLUSION

In this research, a new single-phase nine-level MLI topology is developed. The proposed design for a nine-level boost inverter is based on switching capacitors with fewer switches. The proposed topology's potential in terms of reduced component requirements for the same number of voltage levels is highlighted in a detailed comparison study. The cost comparison supports the suggested topology's lower price with a single dc voltage source for nine-level and shows that it is cost-effective. The proposed topology also has an advantage over other topologies due to the efficiency comparison. The proposed topology is ideal for low and medium voltage applications because to the reduced number of components, lower cost, and improved efficiency. The proposed topology's viability has been demonstrated by a variety of findings obtained under varied loading circumstances. The improved performance of the suggested architecture is supported by various
simulation and hardware results.

V. ACKNOWLEDGMENT

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REFERENCES

[1] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, “A New Multilevel Inverter Topology With Reduce Switch Count,” IEEE Access, vol. 7, pp. 58584–58594, 2019.

[2] Y. Nakagawa and H. Koizumi, “A Boost Type Nine-Level Switched Capacitor Inverter,” IEEE Trans. Power Electron., pp. 1–1, 2018.

[3] N. Sandeep, J. Sathik, U. Yaragatti, and V. Krishnasamy, “A Self Balancing Five-Level Boosting Inverter With Reduced Components,” IEEE Trans. Power Electron., pp. 1–1, 2018.

[4] M. Khenar, A. Taghvaie, J. Adabi, and M. Rezanejad, ”Multi-level inverter with combined t-type and cross-connected modules,” IET Power Electronics, vol. 11, no. 8, pp. 1407-1415, 2018.

[5] M. Saeedian, J. Adabi, and S. M. Hosseini, ‘‘Cascaded multilevel inverter based on symmetric—Asymmetric DC sources with reduced number of components,’’ IET Power Electron., vol. 10, no. 12, pp. 1468–1478, Oct. 2017.

[6] C. H. Hsieh, T. J. Liang, S. M. Chen, and S. W. Tsai, ‘‘Design and implementation of a novel multilevel DC-AC inverter,’’ IEEE Trans. Ind. Appl., vol. 52, no. 3, pp. 2436–2443, May/Jun. 2016.

[7] E.Babaei, S. Alilu, and S. Laali, ‘‘A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge,’’ IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932–3939, Aug. 2014.

[8] H. Abu-Rub, J. Holtz, J. Rodriguez, and Ge Baoming, “MediumVoltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.