Enhanced Bandwidth And Slew Rate Validation of A Class AB Voltage Follower Using 22nm CMOS Technology

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Abstract- *In this recent signal processing application of digital products will have a high priority in bandwidth allocations, in this method of signal transmission and reception will cause additional complication to demodulated original data, it will affect bandwidth and slew-rate due to more signal traffic in today digital world. In this paper, we describe a conventional voltage follower (CNV-VF) with enhanced bandwidth and slew rate with static power dissipations. We propose a method of CNV-AB-VF can boost the maximum output current without increasing the static power dissipations and enhanced the slew rate using some more additional transistors, and here this proposed work will compare CNV-AB-VF method to existing method of CMOS FVF. Finally, this work developed in TANNER EDA, and compared all the parameters in terms of area, delay and power*

Keywords- 130nm Technology, 22nm technology, MOSFET circuits, negative feedback, voltage follower (VF), wide bandwidth (BW)

I. INTRODUCTION

The bandwidth (BW) of the CMOS voltage follower is given approximately by $BW_{CNV} = g_{m1}/2\pi\ C_L$, where g_{m1} is the transconductance of M_1 and C_L is the load capacitance. The negative slew rate (SR^-) of the circuit is limited by the bias current I_B to a value $SR^- = I_B/C_L$, while the positive slew rate (SR^+) can have a relatively large value, since the maximum positive output current is not limited by I_B. In practice, a symmetrical slew rate (SR) is desirable, since the lowest of the positive and negative SRs limits the large signal speed. This means that in practice, the SR corresponds to min $\{SR^+, SR^-\}$. Both the SR and the BW can be increased at the expense of increasing I_B and consequently the static power dissipation. In the modern sub-micrometer CMOS technology, low power consumption is a key requirement for increasing the battery life of portable systems. Class AB VFs (CNV- AB-VFs) can boost the maximum negative output current (and consequently SR^-) without increasing the static power dissipation essentially. Till date, many different CNV-AB-VFs have been reported that have improved the SR without improving the BW. Often, the desired class AB operation is achieved at the expense of increasing the supply voltage, the power dissipation, circuit complexity, and the silicon area. For high-speed applications, both the SR and the BW are equally important.

Three figures of merits can be used to characterize and compare the performance of VFs. First, the current enhancement figure of merit, $FOM_{CE} = I_{outMAX}/I_{Qtotal}$, where I_{outMAX} is the maximum output current and I_{Qtotal} is the total quiescent current. This is related to the SR improvement and the large signal performance of the circuit. Second, the BW figure of merit, $FOM_{BW} = BW(\text{MHz})C_L(\text{pF})/P^Q(\mu\text{W})$, where P^Q is the total quiescent power dissipation of the circuit. Since FOM_{CE} determines the speed limitation for large signals and FOM_{BW} limits the speed of small signals, a third global speed figure of merit [6], [7] can also be defined that corresponds to the geometric mean of the previous two figures of merit $FOM_{GLB} = (FOM_{CE}FOM_{BW})^{1/2}$.

In this paper, we propose to design voltage followers using 22nm technology to achieve the following advantages like: low power, high density, Low area and Less hardware complexity. We proved this by demonstrating using the voltage followers like CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF.

II. VOLTAGE FOLLOWERS

A. CONVENTIONAL VF (CNV-VF)

A voltage buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation.

Fig. 1 shows a Conventional Voltage Follower with 3 transistors M_1, M_2 and M_B used. It is the basic architecture for all voltage followers.

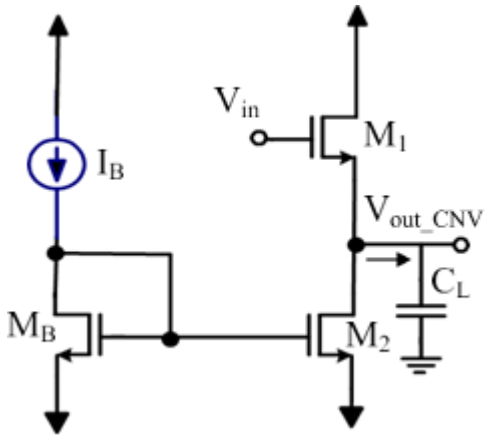

Fig. 1. CNV-VF.

B. FLIPPED VOLTAGE FOLLOWER (FVF)

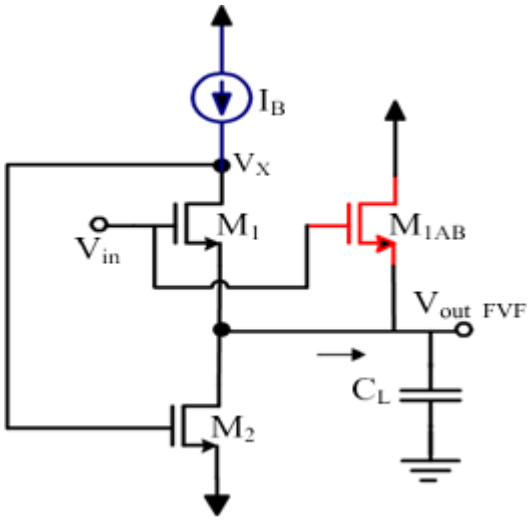

Fig 2 FVF

Fig. 2 shows a class AB flipped VF (FVF) with an additional transistor M_{1AB}, which operates as a CNV-VF and can improve SR^+. However, its output swing is limited by the gate–source voltage of M_2. The input/output peak-to-peak swing is given by $V_{inpp} = V_T - V_{DSsat}$, where V_T is the threshold voltage of the transistor. This swing is very small and independent of the supply voltage. This is a very serious limitation, since in the modern technology, lower values of threshold voltage (V_T 0.4 V) are used. Maximum peak output signals of the circuit with a low distortion are on the order of only 0.15V.

C. CONVENTIONAL CLASS AB VF (CNV-AB-VF)

Fig. 3 shows a CNV- AB-VF that has a resistor R_L inserted between the drain of M_1 and V_{DD}. M_1 and M_2 have equal quiescent currents I_B. It can be considered as a dynamic FVF without the swing limitations of the circuit in Fig. 2, since the dc operating points at node V_x is independent of the dc operating point at node V_Y and they are connected in the presence of ac signals.

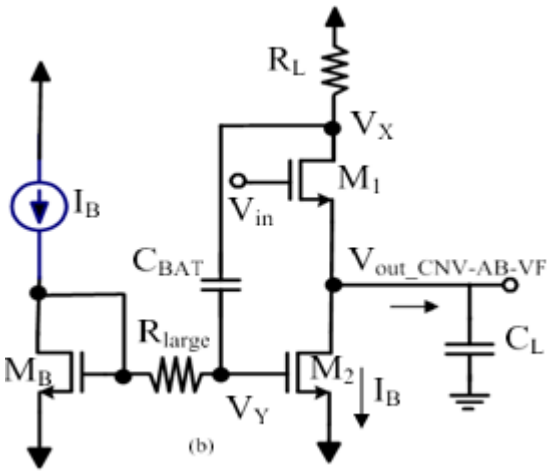

Fig 3 CNV-AB-VF

The Circuit in Fig. 3 operates as follows: transient variations in V_{in} generate variations in V_x which are 180° out of phase with V_{in}. These variations are transferred from node V_x to node V_y using a capacitor C_{BAT} that acts as a floating battery for fast changes in V_x. Furthermore, R_{large} and C_{BAT} form a high-pass circuit for signals passing from V_X to V_Y. This changes the current of M_2 as a function of the variations in Vin. Negative (positive) values of Vin lead to positive (negative) values in V_x and V_Y, which increase (decrease) the dynamic drain current of M_2. This leads to maximum negative output currents that can be essentially larger than I_B and therefore much higher negative SR than the CNV-VF. An additional advantage of the SR enhancement circuit (R_L, R_{large}, and C_{BAT}) is that the local negative feedback through C_{BAT} in the presence of ac signal decreases the output impedance of the follower by the gain $1 + g_{m2} R_L$ of the negative feedback loop. This also helps to enhance the BW of the follower. In the circuit shown in Fig. 3, both the BW and the maximum negative output current (and SR^-) increase with R_L. However, the increase of R_L leads to a decrease in the maximum positive output current (and in the SR^+), since it is in series with the drain of M_1. This does not allow optimizing SR^+, SR^-, and BW simultaneously.

D. PROPOSED CLASS AB VF (PRP-AB-VF)

The proposed VF is shown in Fig. 4. It overcomes the limitations of the FVF shown in Fig. 2 and of the CNV-AB-VF shown in Fig. 3. It is derived by merging the conventional

follower in Fig. 1 with the circuit in Fig. 3. This is done by adding a transistor M_{1AB} connected as a CNV-VF. M_{1AB} can provide a large positive output current which is independent of the value of R_L. To maintain equal quiescent power dissipation as the CNV-AB-VF and the CNV-VF, the current mirror ratio W_{2P} /W_B of the proposed VF is 1:1 where W_{2P} and W_B are the widths of M_{2P} and M_B. The PRP-AB-VF can deliver simultaneously nearly symmetric and large maximum positive and negative output currents and exhibits moderate-to-high BW enhancement with little area overhead and with the same static power dissipation, as the CNV-VF in Fig. 1. The PRP-AB-VF is intended to be used as a buffer for amplifiers.

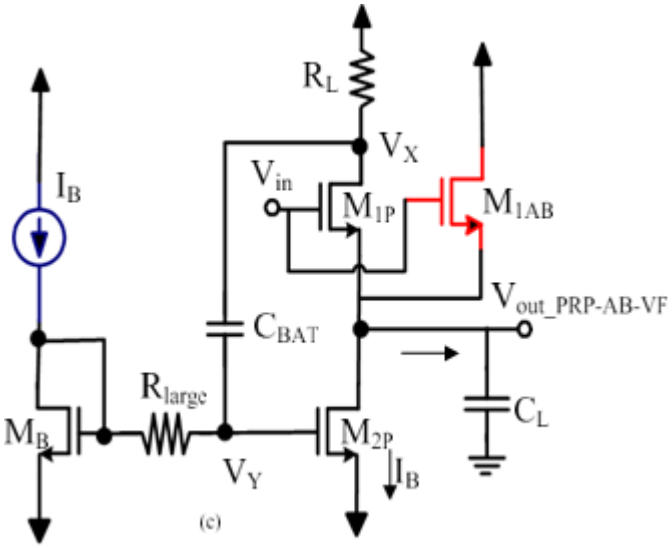

Fig 4 PRP-AB-VF

III. VOLTAGE FOLLOWERS USING 130nm CMOS TECHNOLOGY

When Voltage followers are constructed using 130nm CMOS technology, we may observe the following disadvantages: High power, Low density, High area and Hardware complexity is more. We have proved this by implementing the voltage followers using Tanner EDA tool.

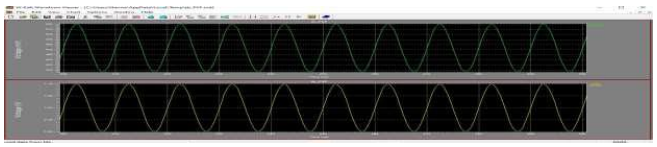

Fig 5 waveforms of CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF in 130nm Technology

The Fig 5 shows the input and output waveforms obtained in W-Edit for the voltage followers CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF. It is obtained by drawing the schematics in S-Edit.

```
* BEGIN NON-GRAPHICAL DATA

Power Results
VVDD from time 0 to 0.0005
Average power consumed -> 6.704188e-011 watts
Max power 5.618213e-010 at time 2.84375e-006
Min power 1.734138e-012 at time 6.09688e-005


* END NON-GRAPHICAL DATA
*

* Parsing                    0.01 seconds
* Setup                      0.01 seconds
* DC operating point         0.00 seconds
* Transient Analysis         0.04 seconds
* Overhead                   0.86 seconds
* ------------------------------------------
* Total                      0.93 seconds

* Simulation completed

* End of T-Spice output file
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* BEGIN NON-GRAPHICAL DATA

Power Results
VVDD from time 0 to 0.0005
Average power consumed -> 3.487353e-008 watts
Max power 3.589388e-008 at time 0.00030963
Min power 2.385435e-008 at time 0.00048753

* END NON-GRAPHICAL DATA
*

* Parsing                    0.00 seconds
* Setup                      0.02 seconds
* DC operating point         0.00 seconds
* Transient Analysis         2.36 seconds
* Overhead                   0.80 seconds
* ------------------------------------------
* Total                      3.17 seconds

* Simulation completed

* End of T-Spice output file
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Fig 6 Power Reports of CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF in 130nm Technology

The Fig 6 shows the Power reports obtained in L-Edit for the voltage followers CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF. It is obtained by drawing the schematics in S-Edit.

IV. VOLTAGE FOLLOWERS USING 22nm CMOS TECHNOLOGY

The 22nm Technology is the latest technology introduced in 2014. When Voltage followers are constructed using this CMOS technology, we may observe the following

advantages: Low power, High density, Low area and Hardware complexity is less. We have proved this by implementing the voltage followers using Tanner EDA tool.

The Fig 7 shows the input and output waveforms obtained in W-Edit for the voltage followers CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF. It is obtained by drawing the schematics in S-Edit. We may observe that the output follows the input in a more precise way.

Fig 7 waveforms of CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF in 22nm Technology

The Fig 8 shows the Power reports obtained in L-Edit for the voltage followers CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF. It is obtained by drawing the schematics in S-Edit. We may observe that the Power of voltage followers is relatively lower in 22nm when compared to 130nm.

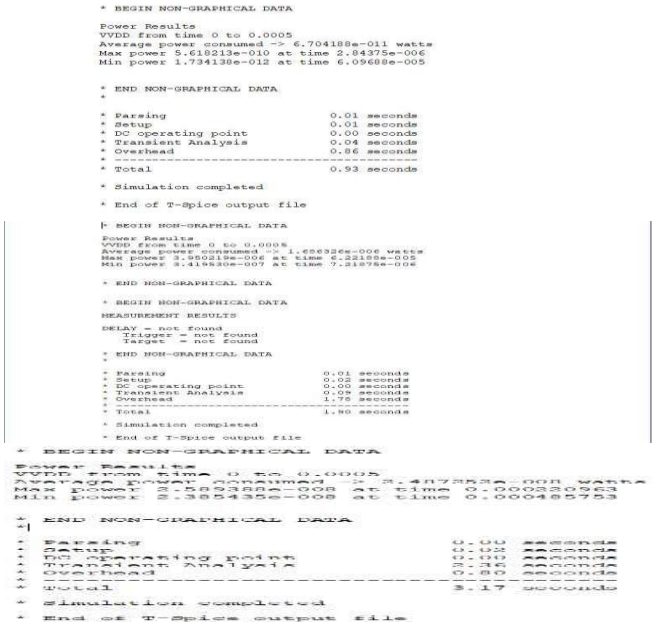

Fig 8 Power Reports of CNV-VF, FVF, CNV-AB-VF and PRP-AB-VF in 22nm Technology

V. COMPARISON OF VOLTAGE FOLLOWERS USING 130nm AND 22nm CMOS TECHNOLOGY

We have compared the various parameters of Voltage followers like number of MOSFETs, Silicon area, Supply voltage, Bias current, Load capacitance, Output Voltage, Quiescent Power, Maximum output current, Total quiescent current and Figure of Merits. The following Table shows the obtained results.

	Analysis, Comparison, and Experimental Validation of a Class AB Voltage Follower With Enhanced Bandwidth and Slew Rate							
	Existing work (130 nm)				Proposed work (22nm)			
	CNV-VF	FVF	CNV-AB-VF Reported	CNV-AB-VF Proposed	CNV-VF	FVF	CNV-AB-VF Reported	CNV-AB-VF Proposed
MOSFET'S	3	3	3	4	3	3	3	4
Silicon Area (nm)	390	390	390	520	66	66	66	88
Supply (V)	2	2	2	2	1.8	1.8	1.8	1.8
I_{Bias}(nA)	0.1	1	5	5	0.1	1	1	1
Load Cap(pf)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
V_{out}^{Max+}(mV)	820	520	765	740	700	450	700	710
Quiescent Power(uW)	2.3 uW	366.04 uW	0.0247 uW	0.0248 uW	0.3122 nW	5.466 nW	0.0923 nW	1.7781 nW

	Analysis, Comparison, and Experimental Validation of a Class AB Voltage Follower With Enhanced Bandwidth and Slew Rate							
	Existing work (130 nm)				Proposed work (22nm)			
	CNV-VF	FVF	CNV-AB-VF Reported	CNV-AB-VF Proposed	CNV-VF	FVF	CNV-AB-VF Reported	CNV-AB-VF Proposed
IoutMax(mA)	0.95	0.87	0.9	0.975	0.45	0.37	0.4	0.475
IqTotal (mA)	0.1	1	5	5	0.1	1	1	1
BW (Mhz)	3.4	13.4	18	50	20	28	35	70
FOMCE = IoutMax / IqTotal	1.5	14.5	3.2	19.5	2.3	19.8	5.6	25.5
FOMBW = (BW*CL)/PQ	820	520	765	740	700	450	700	710
FOMGLB = (FOMCE*FOMBW) ^1/2	2.8	2.03	15	41.6	28.8	30	210	280

Table 1 Comparison of Various Parameters in 130nm and 22nm technology

We may observe that all parameters are relatively optimized in 22nm technology. We have achieved the highest Global figure of merit for all the voltage followers in 22nm. This proves that 22nm technology is more advantageous and accurate.

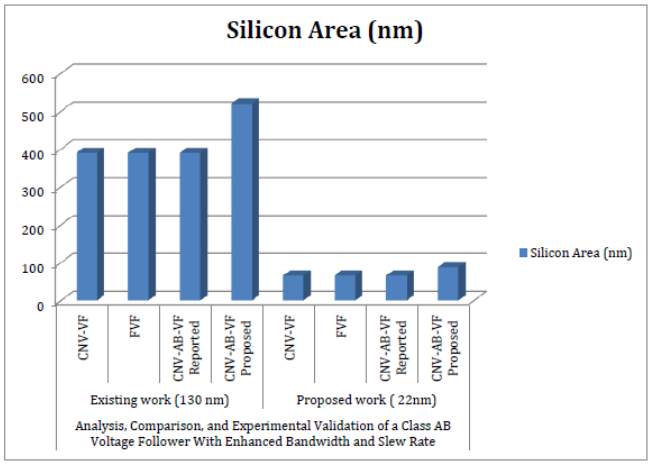

Fig 9 Bar chart of Silicon areas of VFs in 130nm and 22nm

The Fig 9 shows the bar chart of Silicon area of all voltage followers in 130nm and 22nm technology. The silicon area is relatively lower in 22nm. Which in turn reduces the size of the chip required.

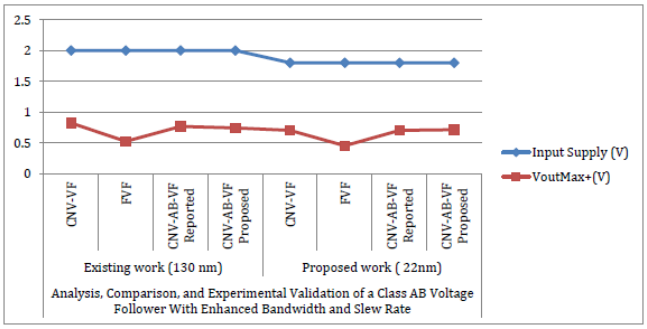

Fig 10 Line chart of Voltages of VFs in 130nm and 22nm

The Fig 10 shows the line chart of input and output voltages of all voltage followers in 130nm and 22nm technology. The 22nm consumed the voltage less and lowered the output voltage as much as it can.

VI. CONCLUSION

A simple modification to the VLSI technology used has been done by replacing the 130nm CMOS technology with 22nm CMOS technology. The 22nm technology consecutively improved the bandwidth and positive, negative slew rates and lowered the silicon area. This has been demonstrated by experimenting all the voltage followers in tanner. It has been shown that the proposed technology has the highest global figure of merit of all the VFs reported in the literature. It has 13 times higher current efficiency and 14.8 times higher FOM_{BW} than the VFs in 130nm with the same power dissipation.

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