A Literature Survey on Different I2C Protocol And It's Different Application

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Abstract- *In this survey paper focused on different I2C Protocol Data Transmission. In the current generation I2C protocol play an important role in the area of protocol communication between different Integrated IC. In the last decade there are many research work proposed in the area of I2C protocol. In this review paper focus on the different I2C protocol and its specification. Also discuss the different problems arise in I2C protocol such as Transmitting and receiving the information, communication protocols, Integrated Circuit and I2C peripherals. These are the major problems discussed in this survey paper.*

Keywords- *I2C protocol, communication, transmit 8-bit,Inter Integrated Circuit, EEPROM, SCL and SDA etc.*

I. INTRODUCTION

An embedded system physical size get reduce by reducing the size of transistor. But the number of interconnected devices also increases which increases the problems. Philips Electronics design the protocol to overcome all these problems in the communication between different Integrated IC called Inter IC protocol.I2C protocol is used by different devices such as keyboard, memory, cell phone ,TV, etc. Physically I2C bus consists of two wires SCL and SDA. These are active high, bidirectional and half duplex in nature. I2C is multi master bus it means that more than One IC is capable for data transpiring .All the devices connected to SCL and SDA line having unique address. Any devices act as transmitter or receiver depending on the nature of the device. Here master initiate the data transfer and data get exchange between master and slave. SCL line controls all the communication between master and slave. By using clock stretching SCL and SDA line avoid collision.SCL and SDA line are bidirectional lines.

Today consumers demands more functionality, speed, energy efficient and power optimized device. A system consists of a set of components that provide a useful behaviour or service. Power dissipated on clock lines in a logic chip is approximately 30-50%. Clock signals have been a great source of power dissipation because of high frequency & load. Clock signals do not perform any computation & mainly used for synchronization. Hence these signals are not carrying any information. Gated-clock is one of the most important techniques to reduce power dissipation. By the gated-clock technique, power dissipated on clock lines including synchronous storage elements such as flip-flops and latches can be saved by shutting off the clock of devices when there is no function required. To increase the speed, we have studied two communication protocols SPI & I 2C. Both SPI and I2C offer good support for communication with low-speed devices, but SPI is better suited to applications in which devices transfer data streams, whereas I2C is better at multi-master "register access" applications.

Transmitting and receiving the information between two or more than two devices require a communication path called as a bus system. A I2C bus is a bidirectional two-wired serial bus which is used to transport the data between integrated circuits. The I2C stands for "Inter Integrated Circuit". It was first introduced by the Philips semiconductors in 1982. The I2C bus consists of three data transfer speeds such as standard, fast-mode and high-speed-mode. The I2C bus supports 7-bit and 10-bit address space device and its operation differ with low voltages.

The I2C is a serial bus protocol consisting of two signal lines such as SCL and SDL lines which are used to communicate with the devices. The SCL stands for a 'serial clock line' and this signal is always driven by the 'master device'. The SDL stands for the 'serial data line', and this signal is driven by either the master or the I2C peripherals. Both these SCL and SDL lines are in open-drain state when there is no transfer between I2C peripherals.

II. LITERATURE REVIEW

K. Bagdalkar, P. et.al. [2020], In this research work researcher proposed working of the I2C controller is validated through SCL and SDA signals on the oscilloscopeI2C signal analyzer and the real-time ADC sensed signals are transferred to host pc for monitoring in the Simulink through RS232 port. In spite of the robust data processing capability of FPGA it

lacks data acquisition interface on-board. One of the peripherals that are missing on the FPGA is analog to digital converter, this paper presents an efficient solution through interfacing a very low cost PCF8591 ADC with FPGA. The two parameters which define the performance of ADC are sampling precision N and sampling rate fs the PCF8591 is 8-bit ADC with maximum conversion rate defined by the maximum speed of the I2C bus which is limited to 100 kHz as the I2C module presents on-chip of PCF8591 supports standard bus mode. These two conditions limit the use of PCF8591 ADC from sensing high-speed signals such as audio signals but at the same time make the PCF8591 ADC most suitable for sensing low-speed signals like current, voltage and power from Hall Effect sensor [1].

Bagdalkar, P. et.al. [2019], In this research work researcher proposed a PROFIBUS peripheral device that can provide interface to CPU/MCU. The implemented circuit satisfies the high performance requirements of equipment for industrial networks, according to IEC 61158-2. The circuit consists of Manchester encoder/decoder, time-critical hardware timers and other functions necessary to implement the data link layer for industrial networks using PROFIBUS-PA protocols. The communication between the CPU/MPU and the proposed device is conducted on I2C serial communication standard. This paper describes the protocols used to read/write commands and data on the device. The circuit was validated on FPGA and can be used as an alternative to commercial models that work with the old parallel ports that are leaving the market [2].

Thiago P. Mussolini et.al. [2019] This work proposes a PROFIBUS peripheral device that can provide interface to CPU/MCU. The implemented circuit satisfies the high performance requirements of equipment for industrial networks, according to IEC 61158-2. The circuit consists of Manchester encoder/decoder, time-critical hardware timers and other functions necessary to implement the data link layer for industrial networks using PROFIBUS-PA protocols. The communication between the CPU/MPU and the proposed device is conducted on I 2 C serial communication standard. This paper describes the protocols used to read/write commands and data on the device. The circuit was validated on FPGA and can be used as an alternative to commercial models that work with the old parallel ports that are leaving the market[3].

Rupal G. et.al. [2018] This research work proposed exhibits how different interfaces are utilized to transmit and receives information to and from the on-board computers and FPGA. So, any low-speed of the peripheral devices in the satellite can be interfaced by means of I2C and MIL-STD-1553 protocols. The outcome shows the least utilization of resources. The above-discussed methods for interfacing the system can be utilized in satellites. The satellites require this interfacing between the systems or on-board computers. The chip design of the I2C protocol for AIS receiver is done successfully using VHDL programming in Xilinx ISE 14.2 and verified on Vertex 5 FPGA for pre synthesis. The Model sum simulation waveform depicts the successful data transfer in transmitter end to receiver end. These methods are particularly made us here to Interface S-AIS receiver and on board computers[4].

Deepika et.al. [2018] Simulation results of the dual master design agree well with the expected or desired I2C bus controller behavior. After one of the master gains control of the bus, it performs the desired function and exhibits behavior which agrees well with the I2C specification. The interfacing of master (FPGA) and the slave device i.e. DC motor also shows the expected behavior and shows how this design works on a physical device. Both the software and hardware part of the design has been successfully implemented. The device utilization on the FPGA was also efficient but it can be further be optimized in the future designs. This project deals with the extension of a single master I2C bus controller to a dual master design i.e. two masters have been able to control the bus. This approach can further be extended to more than two masters and they try to access the bus. The decision logic can be chosen in multiple ways depending on the requirement of the designer. In the future, this design can be made much more beneficial and automated by using logic in which depending on the internal conditions of the protocol, one master wins and others lose the arbitration process [5].

Kumari, R.et. al. [2017], I2C abbreviation is Inter Integrated Circuit. It is a serial bus protocol found by Philips Semiconductor. I2C bus is popular because it is simple to use. I2C protocol is used for communicating low speed devices to processors. It is used to enable the faster device to communicate with slower devices without any data loss. I2C bus controller interfaces the master and slave devices. FPGA acts as a master and MEMS motion sensor (1TG MPU 6050) acts as a slave. In this work focus on MEMS motion sensor data based passed to the FPGA using I2C protocol. MEMS motion sensor has 16-bit ADCs for digitizing the accelerometer outputs. I2C bus on FPGA gives more simplicity because it requires only two wires and less number of pin connections. Hence in this paper we are going to design an I2C bus protocol using Verilog code which interfaces FPGA board with MEMS motion sensor. Noisy data from the MEMS motion sensor is denoised by using haar wavelet coefficients[6].

R. Muhammed, [2016], In this research work BMP280 digital temperature and pressure sensor is successfully interfaced with Arrow's Be Micro CV FPGA Board (Altera Cyclone VE) using I2C protocol in this prototype. The sensors and interface are now finalized as a result of this prototypic study. The upgraded DFE module will be featuring BME280 digital TPH sensor interfaced via I2C protocol. The advantage of BME280 sensor is its ability to measure temperature, pressure and relative humidity together. So instead of using three different sensors for TPH, we can use a single sensor and that will save a considerable space in the PCB. Since it is a digital sensor, we can also eliminate the need for an ADC chip in the future version of the module[8].

W. Andrysiewicz et. Al. [2015] The implementation of the I2C-compatible serial interface for asynchronous ADCs that output data irregularly in time is reported in the paper. The device contains I2C hardware master-transmitter functionality and is capable of operating fully autonomously in I2C bus communication system. The CMOS implementation of the I2C-compatible interface for asynchronous ADCs is presented in the present paper. The device contains I2C hardware master-transmitter functionality and is capable of operating fully autonomously in I2C bus communication system. Future work can address the design improvements related to further reduction of power consumption: FIFO clocking when idle at the price of slightly more complex shift logic, and a mechanism stopping the clock generator when device is idle. [11]

Francesconi, Juan, et. al.[2014] In this work, the Universal Verification Methodology (UVM) is analysed through its application in the development of two test benches for unit verification. The first one targets a First Input-First Output (FIFO) buffer module and employs all the basic UVM components; a scoreboard with a Reference Model and a Functional Coverage collector are also implemented. The second one verifies an I2C EEPROM slave module; a bus functional model for the I2C protocol is defined to facilitate the driver implementation, raising the level of abstraction and allowing the reuse of the verification component for other I2C devices. [13]

Leal-del Río, Tatiana, et. al. [2014] Currently, the most used serial communication protocols to exchange information between different electronic embedded devices are the SPI and I2C. This paper describes the development and implementation of these proto-cols using a FPGA card. For the implementation of each protocol, it was taken into account different modes of operation, such as master/slave mode sending or pending data mode. For the implementation of the I2C protocol was necessary to perform a tri-state buffer, which makes a bidirectional data line for a successful communication between devices, allowing to take advantage of these sources provided by the FPGA. Verilog is a hardware description language better known as HDL and it was used in the work to implement and simulate these communication protocols with the software version 14.7 of Xilinx ISE Design Suite[14].

Eswari, B, et. al. [2013] This research work implements serial data communication using I2C (Inter-Integrated Circuit) master bus controller using a field programmable gate array (FPGA). The I2C master bus controller was interfaced with MAXIM DS1307, which act as a slave. This module was designed in Verilog HDL and simulated in Modalism 10.1c. The design was synthesized using Xilinx ISE Design Suite 14.2. I2C master initiates data transmission and in order slave responds to it. It can be used to interface low speed peripherals like motherboard, embedded system, mobile phones, set top boxes, DVD, PDA's or other electronic devices This project demonstrates how I2C Master Controller (Master) transmits and receives data to and from the DS 1307 (Slave). So that any low speed peripheral devices can be interfaced using I2C bus protocol as master. In future, this can be implemented as real time clock in networks that contains multiple masters and multiple slaves to co-ordinate the entire system by clock synchronization techniques [15].

Zhao, F, et. al. [2011] In this research work, a design method of schematic mapping system based on inter-integrated circuit (I2C) bus and universal serial bus (USB) is introduced. The test principle which is adept by the system and the hardware design structure of the schematic mapping system are explained. Then this paper details hardware design structures of control-circuit, test-circuit and flexible needle bed. At the last, the system software structure and design are analysed[21].

III. I2C COMMUNICATION

The I2C bus protocol is most commonly used in master and slave communication wherein the master is called "microcontroller", and the slave is called other devices such as ADC, EEPROM, DAC and similar devices in the embedded system. The number of slave devices is connected to the master device with the help of the I2C bus, wherein each slave consists of a unique address to communicate it. The following steps are used to communicate the master device to the slave:

Step1: First, the master device issues a start condition to inform all the slave devices so that they listen on the serial data line.

Step2: The master device sends the address of the target slave device which is compared with all the slave devices' addresses as connected to the SCL and SDL lines. If anyone address matches, that device is selected, and the remaining all devices are disconnected from the SCL and SDL lines.

Step3: The slave device with a matched address received from the master, responds with an acknowledgement to the master thereafter communication is established between both the master and slave devices on the data bus.

Step4: Both the master and slave receive and transmit the data depending on whether the communication is read or write.

Step5: Then, the master can transmit 8-bit of data to the receiver which replies with a 1-bit acknowledgement.

3.1 I2C

Transmitting and receiving the information step by step serially with respect to the clock pulses is called I2C protocol. It is an inter-system and short-distance protocol, which means, it is used within the circuit board to communicate the master and slave devices.

3.2 I2C Protocol Basics

In general, the I2C bus system consists of two wires that are used easily to expand the input and output peripheral features such as ADC, EEROM and RTC, and other basic components to make a system whose complexity is very less. Example: Since 8051 microcontroller has no inbuilt ADC – so, if we want to interface any analog sensors to the 8051 microcontroller – we have to use ADC devices such as ADC0804-1 channel ADC, ADC0808- 8 channel ADC, etc. By using these ADCs, we can interface the analog sensors to the microcontroller.

3.3 I2C Basic Commands Sequence

1. Start Bit Condition
2. Stop Bit Condition
3. Acknowledgement Condition
4. Master to slave Write operation
5. Read Operation Slave to Master

3.4 Start and Stop Bit Condition

When the master (microcontroller) wishes to talk to a slave device (for example ADC), it begins communication by issuing a start condition on the I2C bus, and then issues a stop condition. The I2C start and stop logic levels are shown in the figure.

The I2C start condition defines as a high to low transition of the SDA line while the SCL line is high. An I2C stop condition occurs when the SDA line toggles from low to high while the SCL line is high.

The I2C master always generates the S and P conditions. Once the I2C master initiates a START condition, the I2c bus is considered as being in busy state.

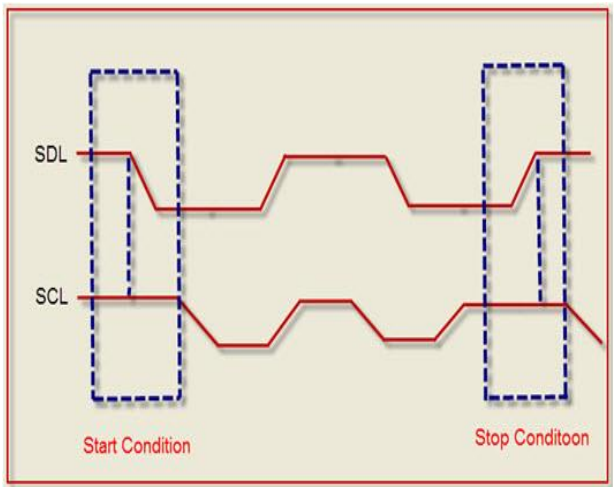

fig 3.1 Start and Stop Bit Condition

IV. CONCLUSION

In this survey paper focus on A Literature Survey on Improve I2C Protocol Data Transmission. The important outcome of this paper is shown in the section of comparative analysis.

In this survey paper observe that the mutual coupling is the major problem in A Literature Survey on Improve I2C Protocol Data Transmission. Also most of the design antenna suffers from lower gain problem.

In future design a better A Literature Survey on Improve I2C Protocol Data Transmission that can improve all these problem in this Transmitting and receiving the information, communication protocols. In future try to fast Fourier. that can conform good better result in terms of I2C protocol.

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