Sparse Channel Estimation and Channel Capacity Maximization Using Multi HOP MIMO OFDM Systems

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Abstract- *Power and energy utilization has recently grown-up to be a vital issue and as an end result, invention of power management techniques should be necessary at all levels of system design such as circuit and device level. The proposed MIMO generator does not required the amending the occupational logic and does not vitiate system recital. This paper first explains about the power manageable components and then illustrates how the system employs the dynamic power management techniques to minimize the power consumption. We diminish the power utilization of Built-in self-test by using dynamic power management scheme which is used in low power design of MIMO generator, especially the power management unit is integrated. We have designed the built in self-test as a group of power manageable components. When the system starts its action, it may exist in one of the power states. Each power state of the system requires different amount of power for its functionality. The dynamic power management technique tells about states of affairs of the systems with an intention of obtaining low power utilization. Corresponding to different power states of system components, different power supply is provided. By using our proposed scheme, we can reduce the power utilization of System on Chip by 37.675%.*

Keywords- MIMO, System Level modulation Management, Power Manageable Components

I. INTRODUCTION

In early days the most important circuit design considerations of VLSI circuit designers are the circuit performance and circuit size. With the significant intensification in portable computing and wireless communication in the last few years, power dissipation has turn into critical issue. These domain applications use battery power-driven systems. So that the power minimization technique should concentrate on design for performance and design for power at all levels of system design. Still the battery based embedded system designs do not survive, power should be preserved for general applications and real time purposes. Low power System designers should give more attention on reducing the power dissipation of the systems. The technique which is developed to avoid the power wastage is called power management technique.

Many power usage minimization techniques have been offered to circuit designers. Some techniques are power down the system which is unused for a long time; switch the system into sleep mode and by providing adaptive clock and voltages to different power states of the system.

We can achieve the minimization of power usage in synchronous circuits by decreasing the switching activity of the clock when the circuits are not performing any significant operations. A power down technique which is used to shut down any unused module in the systems wants added sense to watch the behavior of supplementary systems inside an entire system. A discriminating power down strategy requires additional sense to monitor the activity of various modules within a system. We can use the control lines to gate the clock to different modules within the system. So that for the idle system the clock is not given so that that there is no power wastage. A little care have to be taken when is put into low power states when that module idle period exceeds predetermined time out period. The power minimization technique decides the transition of system power states and when the transition should be occurred. Some of techniques which use the power shut down policy are timeout policy, history based policy and stochastic based policy. Nowadays the design power minimization technique thinks that the modules in the system have some characteristics such as transition between the states, power utilization in each power stages of the system.

II. RELATED WORK

Numerous techniques (Rahul.M.Rao, Jeffery L.Burns, Richard B.Brown, et al, 2002) over the earlier

periods have been introduced to reduce the power consumption of the system by maintaining the performance of the system in efficient manner.

Weiping Liao, Lei He, Kevin M. Lepak et al (2005) have been introduced power management technique which is based on micro architecture level temperature and voltage aware performance. They implement the leakage power model with temperature and voltage scaling and then they show that the total energy varies from 38% and 24% respectively between 65° C and 110° C. They deliberate about relationship between thermal runaway and leakage power and the evaluation of leakage power may demonstrate the way to the malfunction of thermal controls, and overestimation of leakage power may result in extreme performance penalties of up to 5.24%. From these analyses they realize the necessity of temperature aware power minimization using this scheme to dynamic circuits in which clock is used to keep the information stored on dynamic nodes. At this stage we have to be slow down the clock than discontinuation of clock. So the power is reduced. However in this paper, we are concentrating on system level power management technique.

The primary stage of system design is to estimate the impact of power management technique enforced at system level. One of the system power stages that are sleep mode of the system is the extension of discriminating power down scheme. The whole system performance should be monitored than monitoring each module in the system. When the system is idle for some threshold time out duration, then the entire system is shut down. This is known as sleep mode. At this time the inputs which are given for the sleep mode systems should be monitored for its action, which will initiate the system activity by giving wake up signal.

One of the low power techniques which are mostly used by VLSI circuit designers is dynamic power management technique. This technique uses the system resources in efficient manner by controlling their mode of performance and switches the idle systems to the shutdown mode when the idle time period is more than the threshold time out period. The implementation of dynamic power management system on any complex systems is a more difficult process since it requires many design considerations and suspicious debugging method. Power dissipation in integrated circuits depends on the components operations modes. The operation modes are active and standby modes.

In power slow down based power management technique, one of the modules technique. In addition, they study optimal voltage scaling for finest presentation by means of dynamic power and thermal management under special wrapping Options. They explain the circuits which are designed by considering the temperature-aware power minimization technique shows efficient performance than the system which is designed without temperature aware power minimization technique by 6.59%. The advanced cooling techniques are also employed to improve the performance of the circuit.

Fei Hu et al (2006) investigate dynamic power optimization techniques that are resistant to process variation. That is, the power dissipation of the optimized circuit should maintain low power dissipation even if certain degree of process- variation exists. We consider process-variation in terms of the delay variations and classify them into the inter-die and intra-die variations. They propose two new linear programming (LP) models to obtain solutions that continue to maintain low power dissipation under the process variation. The LP models may be based on either worst case timing analysis or statistical analysis. The resulting circuit performance is more variation resistant in terms of power utilization and critical delay model.

Mohammad Ghasemazar and Massoud Pedram et al (2011) has addressed the problem of system- level dynamic power management in the state of chip multiprocessor architectures that are manufactured in nano scale CMOS technologies with large process variations or they are operated under widely varying environmental conditions over their lifetime. They adopt a Markovian Decision Process based approach to CMP power management problem. This proposed technique models, the underlying variability and uncertainty of parameters in system level and finds the optimal policy that stochastically minimizes energy per request. This technique uses well-established prediction techniques to estimate the system state and take globally optimal action accordingly. Compared to the baseline power management algorithms, this technique gains an average power saving of 13%.

Kanika Kaur and Arti Noor et al (2011) describes regarding a variety of strategies, methodologies and power minimization techniques which are used for low power circuit and systems designs and then they have been compared some of the power management design technique properties such as routing delay, power and timing.

III. PROPOSED DYNAMIC POWER MANAGEMENT SCHEME

3.1 Power management system design

We design a system with set of power manageable components which are present under the control of power

manager. We are not concentrating on power manageable components design but we concentrate on how they react with the outer environment. The purpose of this investigation is to be awake of what kind and amount of data to be transmitted between a power manager and system modules in order to employ valuable schemes or methods. In this paper first we describe about power manageable isolation. Then we describe about the dynamic power management technique for systems which has more number of interacting components. Finally we implement the proposed dynamic power management technique to a system and then we show that how it reduces the power consumption of the system.

3.2 Description of power and in phase quadrature component

We have explained the working methodology of power manageable components in general manner. In system level design a power manageable component have been considered as an individual well-designed block. The required important feature of power manageable component is, there should exist several modes of operation. For a given power performance target and power resource availability non manageable components are designed. By using the power manageable components we can switch the system state from the high performance high power mode of operation to low performance low power mode of operation. The power manageable components may have either wide range of modes of operations or number of modes may be large.

Generally if the number of modes of operation is large means we can control the power manageable component in smooth manner so that we can reduce the power dissipation. But in real time modes of operation reduced small for the reason that the circuit design becomes more complex and hardware design for sustaining power minimization should be powerfully prohibited. Another important real time property of power manageable component is that the switching of operation modes has a cost. In several designs, the cost is considered based on either circuit performance loss or circuit delay. If a switching action is not on the spot, and when the component is not ready during state transition, performance is lost every time a transition is started.

Nearly in all practical circuit design applications, the power manageable components are designed as a finite state representation called power state machine (PSM). The system states represent the operation modes. Generally, high-power states have higher performance and smaller switching Latency than states with lower power. In the Flow diagram (Fig.1), the circle represents the server status. The status of server is the combination of work mode and the power mode. Work modes represents either idle or busy or switching activity mode. Power mode represents sleeping or active. The server may present in various work modes with same power mode. The components are able to be managed internally or externally based on the accomplishment of the equivalent scheme.

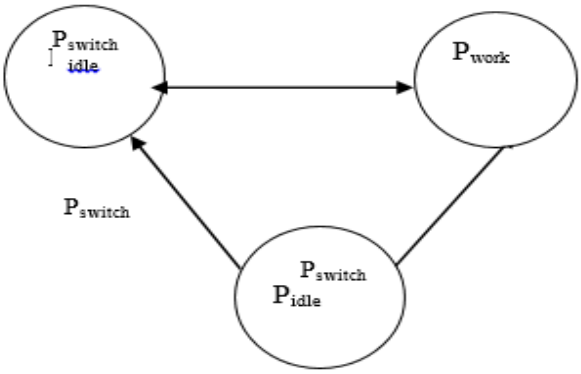

Fig 1: System power states

3.3 In phase Quadrature system design

We consider a system as a collection of components. The components within the systems may interact with each other and there is an externally controllable power manageable component. The performance of the system components can be controlled by controller. In many applications the system components are controlled by software implementation. The system controller has all the exact information about the system components. From this we can conclude that one of the important modules of system controller is power manager implementation. The important service of any power manageable system is, it should give the information about the system components to the power manager. To reduce the system design time, the interface between the power manager and the system components should be standardized. Information about the workload is one of the vital requirements of power management technique. The listener block used to gather the workload information of all the power manageable components which are available in the system, while the controller gives commands to switch the component into different states.

The three reasons which are main causes for power consumption in VLSI circuits are

1.Leakage current which can be estimated by the method used in its fabrication. And it consists of reverse bias current and sub threshold current.
2.Short circuit current which is the result of DC path between the supply voltage changes when the outputs are changing.

3.Switching current this is the result of capacitor charge and discharge during logic changes.

The leading source of power consumption is the switching power dissipation and is given, for a circuit node, by:

$$Pi = C.V^{2}.E.f \qquad (1)$$

Where *C* is the capacitance,
V_{dd} is the input supply voltage,
E is the average number of transitions in the circuit per 1/f time, and
f is the clock frequency

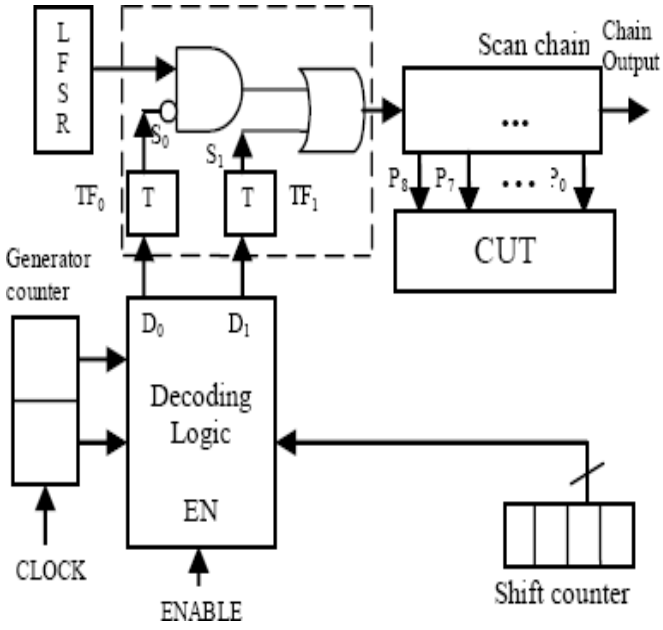

Fig 2: MIMO management system architecture

We can reduce the power consumption of the circuits by reducing the load capacitance, C. This can be done by using small transistors with low capacitances in non-critical parts of the circuit. Reducing the frequency of operation f will cause a linear reduction in dynamic power, but reducing the supply voltage V_{dd} will cause a quadratic reduction.

This paper presents a new system level dynamic power management design to decrease the power usage of system. We form architecture with four different systems which are controlled by power manageable component. The systems may exist in any type of power states. Many algorithms can be used for categorizing the system power states. We consider a simple threshold based dynamic power management scheme. We consider three system stages. When the system performs a task, it is said system state too early on to a sleep state may show the way to wastage of power, for the reason that the energy required for the system to come back to busy state from sleep state is typically high. Due to this reason we employ a threshold based power management technique. This technique waits at the idle state for a threshold amount of time out duration, after that the system state is changed to sleep stage.

To be in busy state. In busy state the components dissipate the same amount of power. So it does not contribute any power wastage. When the system has no task to carry out, we believe that an incident no task is detected by the power manager. As an effect, the series of work arrivals and executions are modeled as an order over the incident set {task, no task}. If the system does not have any work to do means, that system is switched into an idle state. The energy dissipated from this state to come back to busy state, upon arrival of a task is small. The final state of the system is sleep state, if any system does not want to dissipate any power that system state is changed to sleep mode. But, changing the

In the proposed system the required power for data transmission is calculated principally. For sending little amount of data system requires small quantity of power. For sending huge amount of data system requires large amount of power. The power manager system compares the calculated power with the subsystem power requirement. The power requirement for the data transmission is calculated. The system is selected to transmit the data based on the power requirement. One of the systems is selected to transmit data and at the same time the other systems are kept in sleep mode. So that we can reduce the power consumption of the overall system.

By reducing the supply voltage required for the transmission of the data the power consumption has been reduced. Dynamic power is proportional to the square of the input supply voltage. Therefore, reducing the voltage considerably improves the power consumption. In addition frequency is directly proportional to the supply voltage, the frequency of the circuit can also lowered, and thereby a cubic power reduction is possible. From this we can know that, the delay of the circuit depends on the supply voltage.

$$T_{delay} = g.C.V_{dd} / (V_{dd} - V_t)\ \text{^}2 \qquad (2)$$

Where
T_{delay} is the circuit delay g is the gain factor,
C is the capacitance,
V_{dd} is the input supply voltage, and
V_t is the threshold voltage.
By reducing the supply voltage we can reduce the power consumption and it increases the execution time.

3.4 Proposed MIMO algorithm

Step1: Get the input
Step2: Set threshold values for each power stages of the system.
Step3: Pass given inputs according to threshold values.
Step4: Calculate the required amount of power to transmit the input data.
Step5: Set the capacitance, voltage and frequency values to each stages of the system.
Step6: Power can be calculated using the formula Power=capacitance*(voltage) ^2*frequency.
Step7: Find out the power states of the sub systems. Step8: Find the power of the subsystems based on its power states,

If (state = Active)
High power, Else if (state=standby)
Medium power,
Else
Low power.

Step9: Compare the amount of power required transmits the input data and subsystem power and set threshold value for each system.
Step10: Based on the threshold values of subsystems we can transmit the data.
Step 11: If data is transmitted to one of the subsystems, the other subsystems are put into sleep mode.

IV. PERFORMANCE ANALYSIS

4.1 Simulation results

The simulation environment is created in MODELSIM by using VERILOG language for the programming. We consider the four systems which are in active, sleep, deep sleep and idle mode respectively. The power manager system calculates the required power to send the data to the subsystems. Normally we can send heavy or large amount of data to the system which is in the active mode. We can also send small amount of data to the systems which requires less amount of power. We have calculated the power which is required in the normal dynamic management system for character data transmissions. And also we have calculated the power required for character data transmission using the proposed dynamic power management system. From the results we can say that the proposed algorithm reduces the power consumption in the systems.

4.2. Input power estimation

Depending upon the given input data the power is calculated. High amount of data has been passed to the system which is in the active state. So that to transmit high amount of data the input voltage and frequency must be high. So it consumes high power.

$$P_{high}=C.f_{high}.V_{high} \quad (3)$$

To transmit fewer amounts of data it requires fewer amounts of input voltage and frequency because the system is switched to low power state.

$$P_{low}=C.f_{low}.V_{low} \quad (4)$$

We have calculated the amount of power which is required to transmit the given input data to the system using the above equations 3 and 4. The given input data and the calculated power required for the data transmission have been plotted in the following graph.

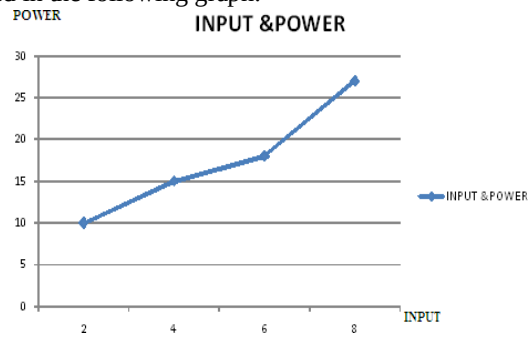

Fig 3: Input data and required power

4.3. Comparison result

In this we have compared our proposed dynamic power management system with existing power management system. In the existing system without dynamic power management consumes more amount of power is required to transmit the data to the system. By using our proposed dynamic power management technique we can reduce the power consumption of the overall system by switching the subsystems to sleep mode which are not participated in the data transmission. From the result we can say that our proposed DPM technique reduce the power consumption of system by 37.675%.

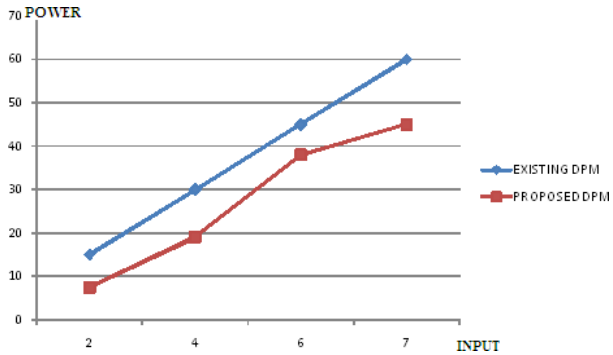

Fig 4: Comparison of existing and proposed I/Q

V. CONCLUSION

In this work we have analyzed the importance of dynamic power management technique in system level power management to reduce the power consumption for data transmission. There are many dynamic power management techniques available. We have proposed a new dynamic power management technique in order to reduce the power consumption at system level. From the results we can conclude that the proposed technique reduces the power consumption nearly 37.675% compared with the system which is designed without any power management technique.

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