Multilevel Hybrid Inverter Using Square Pulse Width Modulation Switching Strategy

Kesav Moorthy[1]. Madeshwaran[2], Pammisehkar Aswin Sai[3], Narayanan V[4], Sabari. L. Uma Maheshwari[5]
[5]assistant Professor
[1, 2, 3, 4, 5] R.M.K Engineering College
Business Development Manager Jhonson Control India Pvt Ltd ,Pune

Abstract- *This Paper presents a single-phase cascaded transformer based multilevel inverter with a modified carrier-based level shift sinusoidal pulse width modulation (LS-SPWM) technique. The developed topology has two bridges with individual low frequency transformers. The bridges can generate quasi-square waveform and pulse width modulated waveform independently and energized the two transformers whose secondary terminals are cascaded to attain 19-level output voltage waveform across the load. The anticipated configuration has the least number of components to reduce the cost and enhance the reliability of the converter for medium power applications with inbuilt isolation. Furthermore, this letter presents the most common LS-SPWM technique with a new carrier to enhance the fundamental magnitude and shifts the dominant harmonics into three times of the traditional strategy for the same modulation indices. The performance of the proposed topology is validated with experimental results.*

Keywords- Carrier-based pulse width modulation, multilevel inverter (MLI), total harmonic distortion (THD).

I. INTRODUCTION

IN RECENT past, multilevel Inverters (MLIs) are considered as the most important power converter for various applica- tions, such as power-active filters, ac traction, direct grid integration systems, electric vehicles, etc. In reality, the quality of multilevel output voltage waveform is enriched as the number of levels moving high. Moreover, an appropriate switching strategy raises their potentiality in terms of good power factor, smaller filter size, improved efficiency, less voltage stress on power devices, and reduce energy waste. In current scenario, diode clamped MLI, flying capacitor MLI, and cascaded MLI are drawn more attention to accomplish the above-mentioned applications. In this perspective, many new inverter configurations with a claim of less device count are suggested in the literature [1], [2]. In [3], the author suggested a cascaded transformer-based MLI with single dc supply. Herein, all H-bridges are connected to individual transformers to attain optimal output voltage levels. How- ever, it has drawn a huge number of switches and heavy weight transformers. It is addressed in [4] and [5] by replacing the H-bridges with a new arrangement of semiconductor switches. Additionally, the transformer-based MLIs are very much suitable for medium and high power applications [6]. At the same time, other kind of MLIs like asymmetrical or hybrid archetype utilizes an isolated dc supplies and capacitors to get desired multilevel output waveforms . Owing to the traditional control techniques have their limitations like:

1) complex to design and implement (in space vector pulse width modulation (SVPWM)) when levels exceed more than five;
2) initial guess (in selective harmonic elimination (SHE)) plays a major role in Newton–Raphson method to calcu- late the switching angles;
3) a wide sideband harmonics are existed in sinusoidal pulse width modulation (SPWM) technique.

To mitigate aforementioned problems, we proposed a novel carrier-based SPWM technique for a new hybrid MLI. The basic intention behind the implementation of a new control technique is to improve the magnitude and harmonic profile of the load voltage. The recommended topology has the capacity to boost up the number of output voltage steps using only 12 power switches, two dc sources results in reduced gate driver circuits and power supplies.

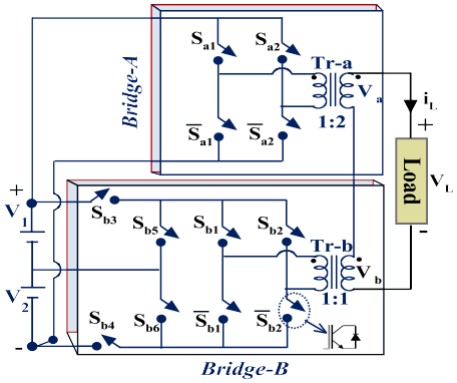

Fig 1.1 Proposed 19 Level Invverter

II. PROPOSED19L-INVERTER CONFIGURATION

A. Proposed Topology Operating Principle

The Proposed System Topology is present in above figure contains two bridges .Bridges A is traditional H-bridge generates three level voltage waveform. Bridge –B is a PWM inverter build with an H Bridge and four individual switches**.** An antiparallel diode (D) of the switch conducts only for allowing negative current through it and the insulated-gate bipolar transistor (IGBT) (sw) is con- ducted to permit the positive current. Regarding the input dc supply, the magnitude of input dc source V_1 selected as twice the magnitude of the dc source V_2 . In proposed topology, the transformer ratios are 1:2 and 1:1. Thus, the dc supplies are fixed to 2:1 ratio to realize 19-level output voltage waveform. Moreover, the load current and the secondary currents of the transformers should be the same, since the secondaries of the two transformers are shorted through the load. In fact, the primary current waveforms of the transformers are accomplished 19-levels even though primary voltages are different and these can be observed for resistive loads. . Let us consider V_{dc} is equal to the magnitude of V_2 (input dc source).

1) First state: this level is designated as 1L, switches S_{a1} , S_{a2} of Bridge-A and S_{b1} , S_{b2} , S_{b4} , and S_{b5} of Bridge-B are ON, Thus, the load voltage $V_L = 0 + V_2 = V$dc.
2) Second state (2L): Switches S_{a1} , S_{a2} of Bridge-A are connected to short the transformer-A primary windings and S_{b1} , S_{b2} , S_{b3} , and S_{b6} of Bridge-B are ON, then V_1 dc source is connected to the Bridge-B, Thereby, voltage across the load becomes $V_L = 0 + V_1 = 2V_{dc.}$
3) Third state (3L): Switches S_{a1} and S_{a2} of Bridge-A are connected to short the transformer-A primary windings and then S_{b1} , S_{b2} , S_{b3} , and S_{b4} of Bridge-B are ON, V_1 and V_2 dc sources are connected to the Bridge-B, therefore, voltage across the load is $V_L = V_1 + V_2 = 3 V_{dc}$.
4) Fourth state (4L): from this state the Bridge-A starts to share the load power. Switches S_{a1} , S_{a2} of Bridge-A and S_{b1} , S_{b2} , S_{b3} , and S_{b6} of Bridge-B are ON, thus, the load voltage $V_L = 2(V_1 + V_2) + (V_1) = 6 V_{dc}$ $2 V_{dc} = 4 V_{dc.}$ The Bridge-A output peak voltage magnitude is increased from 3 V_{dc} to 6 V_{dc} since the turn's ratios of Tr-a is considered as 1:2.
5) Fifth state (5L): Switches S_{a1} , S_{a2} of Bridge-A and S_{b1} , S_{b2} , S_{b4} , and S_{b5} of Bridge-B are ON, Thus, the load voltage $V_L = 2(V_1 + V_2) + (V_2) = 6 V_{dc}$ $1 V_{dc} = 5 V_{dc}$.
6) Six state (6L): Switches S_{a1} , S_{a2} of Bridge-A and S_{b1} , S_{b2} of Bridge-B is activated. Thus, the load voltage $V_L = 2(V_1 + V_2) + 0 = 6 V_{dc}$.
7) Seventh state (7L): Switches S_{a1} , S_{a2} of Bridge-A and S_{b1} , S_{b2} , S_{b4} , S_{b5} of Bridge-B are ON, Then the voltage across the load is $V_L = 2(V_1 + V_2) + V_2 = 6 V_{dc} + 1 V_{dc} = 7 V_{dc.}$

B.Proposed Switching Scheme

The proposed switching strategy comes under the level shift pulse width modulation technique (LS-PWM) family. According to the phase position of the carrier waveforms, LS-PWM strategies are categorized into three types [11]. Herein, the pro- posed topology is switched with the phase opposition disposition (POD) PWM technique. Basically, triangle and ramp signals are used as carrier waveforms in the entire carrier-based switching techniques. Furthermore, the carrier frequency (f_{cr}) normally kept high to curtail the lower order harmonics. How- ever, the switching and EMI issues severely affect the operation and control of the converter for higher f_{cr} value. To address aforementioned problems a new carrier is introduced. Here, the proposed carrier operates with lower f_{cr} to suppress the wide range of lower order harmonics than traditional carrier-based techniques. The present section demonstrates the proposed technique in detailed. Let assume carrier frequency is too higher, and then the sine reference signal (V_{ref}) seen by the carrier waveform is a constant dc signal . In fact, any multilevel voltage waveform is mathematically expressed in terms of dc offset, fundamental and its sideband harmonics, and carrier harmonics. Therefore, the carrier shape can decides the existence of the harmonics in the multilevel output waveform. The proposed carrier is discovered from the center aligned carrier so called triangular waveform without changing the peak-to-peak magnitude and frequency of the carrier wave.

The carrier and reference waveforms con- sider in can generate the positive 9th-level switching pulses S_9. Similarly, other carrier waveforms are compared with a reference waveform to produce pulses for remaining output levels. The positive slope of the carrier (first half-time period of the triangle) intersects the voltage

If the magnitude of δ varies, then the number of pulses and the width of the chops are altered accordingly. It can be demonstrated in Fig. 3(b)–(e). Primarily, the polarity of δ is negative, i.e., 0.3, and S_9 has only two pulses. In the second case, also, the polarity is negative (δ = 0.15), but the width of S_9 pulses is different. In the third stage, δ is a positive value (δ = +0.45) and the number of hitting instants with reference waveform is higher, which leads to getting more

number of chops without changing the carrier frequency (it is still $1/T_s$). Thus, it can be concluded that the number of chops per carrier period depends on the polarity of the delta. In other sense, S_9 can get more number of chopped pulses for positive δ values. Furthermore, the positive delta de- creases harmonic content as well as increases the fundamental magnitude of the output voltage.

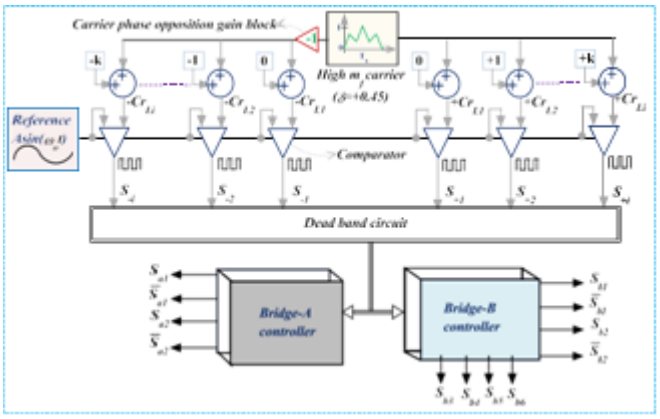

Fig 1.2: Proposed Control Technique Of 19 Level Inverter

The implementation of the proposed POD-PWM strategy to trigger Bridge-A and Bridge-B of the developed configuration is depicted in Fig. 4. To build the 19-level output wave- form through the LS-PWM strategy, 18 carrier waveforms are needed. Herein, positive nine carrier waveforms (from $+Cr_{L1}$ to $+Cr_{L9}$) are out of phase with negative nine carrier wave- forms (from Cr_{L1} to Cr_{L9}). As a matter of fact, all car- rier waveforms are established with only one carrier waveform. Initial driving pulses are delivered from the comparator that compares the fundamental sinusoidal reference waveform with the proposed carrier waveforms. Later, the dead band circuit is dedicated to avoiding the shoot through faults between the complementary switches. Finally, the actual gate pulses of the bridges (S_{a1} , S_{a2} , S_{b1}, S_{b2} , etc.) are developed by proper logi- cal combination among the initial driving pulses (from S_{-9} to S_{+9}). Actually, inverter constraints are varying with the magnitude of δ and three remarkable cases are observed at δ = 0.3, 0.45, and 1. This case is treated as conventional carrier-based PWM technique since the carrier shape a triangle. The fundamental peak of load voltage (V_p) is 327.7 V and the dominant harmonics are 21st and 19th orders at 1 kHz switching frequency. In this case, output waveform attains better THD than case-1 i.e., 5.29%. Moreover, the carrier frequency is still 1 kHz but the dominant harmonics are shifted to 61st, 59th order. Thereby, cost of the load side filter is drop down effectively.

Case 3 (δ = 1):

It also treated as a traditional carrier-based PWM technique since the carrier shape is a triangle. Even though the given carrier frequency is 1 kHz, the switching frequency becomes triple due to the delta magnitude is +1. Furthermore, the V_p is lesser compared with case-2 and switching stresses are high.

Thereby, the carrier waveform presented in case-2 has prominent features as follows: reduction in switching and conduction losses (P_{sw} and P_c); improves the FFT spectrum; rise in peak magnitude of the load voltage;

III. RESULTS AND DISCUSSION

To confirm the validity of the proposed topology with suggested switching technique, an experimental setup is constructed with SKM75GB123D half bridge IGBT modules, two linear cold rolled non-grain oriented (CRNGO) core transformers (Tr.1: 200VA, Tr.2: 100VA), and two channel Aplab dual dc power supply that provides two input dc sources (V_1 = 30 V and V_2 = 15 V), moreover, an appropriate gate driver circuits are built by TLP- 250 opto couplers. Further, the OP5142-RT simulator merely considered as a controller running with sim ulation time 50e-6 and the operating switching frequency is 1.5 KHz. The load parameters are considered as R = 36 Ω and L = 70 mH to evaluate the presented topology.

Bridge-A, Bridge-B output volt- ages, and load voltage when modulation index m_a changes. The Bridge-A starts to feed the load when m_a > 0.3. It is evident that, as m_a changes, the power sharing between the bridges will vary [3]. In the presented configuration, the power sharing of the transformer are distributed as 78% of the transformer-a, and 22% of the transformer-b at the rated load conditions. Further, important issues about transformers when fed with low frequency waveform create heating issues. This further effects efficiency of a converter. However, if winding currents are sinusoidal then extra losses can be minimized . On the other side, presence of the transformer in the proposed design ensures the following: less voltage and current rating switches; drastically minimizes voltage stresses; eliminates higher order harmonics; provides inbuilt isolation; and matches the voltages between source and line. Next, an experimental 19-level load voltage, load current, and corresponding bridge voltages. for m_a = 1 are shown in , where 180 V, 90 V, 270 V, and 7.3 A are the peak-peak magnitudes of V_a , V_b , V_L , and i_L , respectively.

IV. CONCLUSION

In the present paper, a novel hybrid multilevel inverter is recommended to verify the performance of the proposed carrier-based LSPWM technique. The recommended

topology is achieved 19-level PWM output waveform with only two bridges. The bridge outputs are connected to the line frequency transformers that provide isolation between the load and dc supply. The proposed topology is extremely suitable for active filters, var compensators, and grid connected systems. Addition- ally, the proposed switching technique plays a significant role to improve the FFT spectrum of the output waveform with less switching frequency. Moreover, it it can apply to all hybrid and asymmetrical topologies.

REFERENCES

[1] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57.8, pp. 2553–2580, Aug. 2010.

[2] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A review on symmet- ric, asymmetric, hybrid and single DC sources based multilevel inverter topologies," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 788–812, 2017.

[3] K. Feel-Soon *et al.*, "Multilevel PWM inverters suitable for the use of standalone photovoltaic power systems," *IEEE Trans Energy Convers.*, vol. 20, no. 4, pp. 906–15, Dec. 2005.

[4] B. M. Reza, H. Khounjahan, and E. Salary, "Single-source cascaded trans- formers multilevel inverter with reduced number of switches," in *Proc. Power Electr.*, 2012, pp. 1748–53.

[5] S. Behara, N. Sandeep, and R. Y. Udaykumar, "Transformer-based seven- level inverter with single-dc supply for renewable energy applications," in *Proc. IEEE 7th India Int. Conf. Power Electr.*, 2016, pp. 1–6.

[6] F. Kang *et al.*, "A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system," *Solar Energy*, vol. 78.6, pp. 727–738, 2005.

[7] R. S. Alishah *et al.*, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electr.*, vol. 7, no. 1, pp. 96–104, 2014.

[8] E. Babaei and S. H. Hosseini, "Charge balance control methods for asym- metrical cascade multilevel converters," in *Proc. Int. Conf. Electr. Mach. Syst.*, 2007, pp. 74–79.

[9] K. K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electr.*, vol. 5, no. 4, pp. 435–46, 2012.

[10] Colak,, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Convers. Manag.*, vol. 52.2, pp. 1114–1128, 2011.

[11] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM methods," in *Proc. IEEE 33rd Annu. Meet. Ind. Appl. Conf.*, vol. 2, 1998, pp. 1424–1431.

[12] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for mul- tilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49.4, pp. 858–867, Aug. 2002.