# Design of Multibit Flip-flop with Adaptive Clock Gating for Area Efficient Applications

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***Abstract-*** *Adaptive Clock-Gating (ACG) and Merging Flip-Flops in which several FFs are grouped and share a common clock driver are two effective low-power design techniques. Combining these techniques into a single grouping algorithm and design flow enables further power savings. We study MBFF multiplicity and its synergy with FF data-to-clock toggling probabilities. A probabilistic model is implemented to maximize the expected energy savings by grouping FFs in increasing order of their data-to-clock toggling probabilities. The clock signal driving a FF is disabled when the FFs state is not subject to change in the next clock cycle. Data-driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is presented to group several FFs to be driven by the same clock signal, generated by ORing the enabling signals of the individual FFs. By using pass transistor logic, we can reduce the count of transistors in the designs and thus can have better results in terms of area and delay. The total designs of proposed Multi-bit Flip flop is done in Tanner EDA tool*

***Keywords***- Clock gating (CG), clock network synthesis, low-power design, Pass Transistor Logic.

## I. INTRODUCTION

The data of digital systems are usually stored in flip-flops (FFs), each of which has its own internal clock driver. In an attempt to reduce the clock power, several FFs can be grouped into a module called a multi bit FF (MBFF) that houses the clock drivers of all the underlying FFs. We denote the grouping of kFFs into an MBFF by a k-MBFF. Kapoor et al. reported a 15% reduction of the total dynamic power processor design. Electronic design automation tools, such as Xilinx Liberate, support MBFF characterization. The benefits of MBFFs do not come for free. By sharing common drivers, the clock slew rate is degraded, thus causing a larger short-circuit current and a longer clock-to-Q propagation delay tpCQ. To remedy this, the MBFF internal drivers can be strengthened at the cost of some extra power. It is therefore recommended to apply the MBFF at the RTL design level to avoid the timing closure hurdles caused by the introduction of the MBFF at the backend design stage. Due to the fact that the average data-to-clock toggling ratio of FFs is very small, which usually ranges from 0.01 to 0.1, the clock power savings always outweigh the short-circuit power penalty of the data toggling.

An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio (also termed activity and data toggling probability).

One of the major dynamic power reduced by clock gating method in computing and consumer electronics products in the overall system's clock signal then reduce the 30%–70% of the total dynamic power consumption and then reduce the overall circuit power to reduce15- 20% of Grouping Flip Flop data driven clock gating method. Clock gating is major method of reducing clock signal. Generally, when a logic unit is clocked, it is based on the sequential elements receiving the clock signal, sequentially they will toggle in the next cycle whether it is required or not. The data driven clock gating circuit using clock enabling signals are manually added for every FF as a part of a design methodology.

In this paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs. The optimal fan out of a clock gate yielding maximal power savings is derived based on the average toggling statistics of the merging FFs, process technology, and cell library in use. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires, therefore, extensive simulations and statistical analysis of the FFs activity. Another grouping of FFs for clock switching power reduction, called Multi bit FF (MBFF). MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs. MBFFs the advantages are: 1) smaller

design area due to shared clock drivers and less routing resource 2) Less delay and less power of clock network due to fewer clock sinks 3) Controllable clock skew because of common clock and enable signals for the group of flip flops and reduced depth of a clock tree.

Recent methods aim at reducing the switching activity during scan shift cycles, whose test generator allows automatic selection of their parameters for LP pseudorandom test generation. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods, can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG). This is one of the major motivations of this paper. Most of the previous deterministic BIST approaches did not include LP concerns. We intend to present a new method that effectively combines an efficient LP PRPG and LP deterministic BIST. In order to reduce test power in deterministic BIST, we will propose a new LP reseeding scheme, since there is no other effective solution in this field.

## II. DATA DRIVEN CLOCK GATING

An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio.

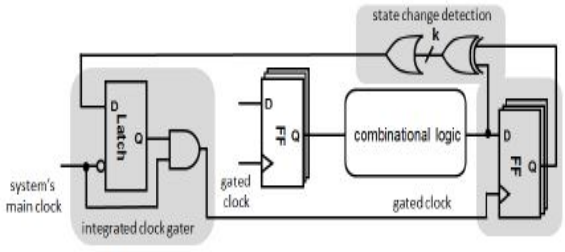


Fig. 1. DDCG integrated into a *k*-MBFF

Fig. 1 illustrates a DDCG integrated into a *k*-MBFF. The shaded circuits reside within a library cell. Given an activity *p*, the group size *k* that maximizes the energy savings solves the equation.

$$(1-p)^k \ ln(1-p) C_{FF} + \frac{C_{latch}}{k^2} = 0 \qquad (1)$$

where $C_{FF}$ and $C_{latch}$ are the clock input loads of an FF and a latch, respectively. The solution to (1) for various activities is shown in Table I for typical $C_{FF}$ and $C_{latch}$. The above optimization does not take into account the clock driver sharing, which also affects the optimal grouping as shown below. To grasp the power savings of a *k*-MBFF achievable by DDCG, Fig. 1 was simulated with SPICE for various activities *p* and *k* = 2, 4, 8.

Clearly, the best grouping of FFs that minimizes the energy consumption can be achieved for FFs whose toggling is highly correlated. Using toggling correlations for MBFF grouping has the drawback of requiring early knowledge of the value change dump vectors of a typical workload. Such data may not exist in the early design stage. More commonly available information is the average toggling bulk probability of each FF in the design, which can be estimated from earlier designs or the functional knowledge of modules. FFs' toggling probabilities are usually different from each other. An important question is therefore how they affect their grouping. We show below that data-to-clock toggling probabilities matter and should be considered for energy minimization.

In data driven clock gating methodology is used to reduce the power consumption and reduce the delay of the circuit. The data driven clock gating is power reducing using in merging flip flop and integrated clock gating circuit. The block diagram of merging flip flop using data driven clock gating circuit is shown in fig 2. The ICG is disable then the output of state change detector is input of the ICG circuit. State change detector is XORed output and k enabling signal of the Flip Flop, by ORed the input of ICG circuit. The arithmetic circuit is used by logic circuit of data driven clock gating circuit. The merging Flip-flop reduces the unwanted clock signal of circuit. The unwanted glitches are reduced in data driven clock gating circuit.

### A. ADAPTIVE CLOCK GATING

An adaptive clock gating circuit is shown in Fig. 3. By XORing gate its output with the present input of Integrated Clock Circuit that will appear at its output in the next clock cycle, an FF checks whether its state is subject to change, thus finding out whether its clock can be disabled in the next cycle. The outputs of k XOR gates are ORed and then latched to generate a joint gating signal for k FFs. The combination of a latch With AND gate is called Integrated Clock Gate (ICG), commonly used by industrial electronic design automation (EDA) tools. The practical Data Driven Clock Gating block

diagram is given above. The function of module list is given that State Change Detector, Merging Flip-Flops and Integrated Clock Gating.

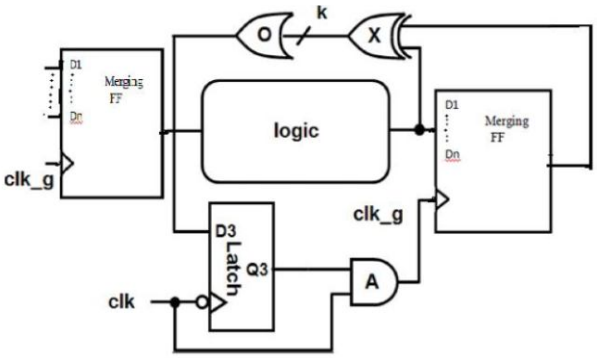


Fig. 2 Circuit diagram of practical Adaptive Driven Clock Gating

### *B.* CLOCK GATING

Clock gating circuit is power consumed by 50 % of dynamic power. The clock gating reduce dynamic power by combinational logic circuit and then the circuit reduce clock pulse and sharing the clock signal in merging flip-flops and reduce clock signal. The profitable EDA tools are supported clock gating technique. There are two types of clock gating technique. They are Latch-based clock gating and Latch-free clock gating. The latch-free clock gating technique uses a simple AND or OR . The latch-based clock gating technique is a level-sensitive. In this project using in latch based clock gating technique. The latch-based clock gating technique is called Integrated Clock Gate (ICG). The Integrated Clock will be disables in the next cycle by XORing the output of the present data input and it will reveal at the output in the next cycle. Then the output of the XOR gates are ORed for generating the gate signal for the FF's which is to be used to avoid the glitches. The Integrated clock gate (ICG) can be used by the environmental tools by the combination of LATCH with the AND gate. These latches could be used in ultra-low power applications for a digital filter. The data driven clock gating signal are being used as an enabling signals in this applications. There will be a trade-off for ICG is the number of clock pulses could be disabled. The pulses could also be a trade-off for the hardware over-head. While increase the number of flip-flops the hardware overhead decreases to obtain by ORing the enable signals. The level of this high and the low state of signals could be processed in the same versa to give the proper output.

### *C.* PROPOSED MULTIBIT FLIPFLOP

A popular and widely used alternative to complementary CMOS is pass-transistor logic. Pass-transistor logic attempts to decrease the quantity of transistors necessary to realize the logic by allowing the principal inputs to drive gate terminals (Radha krishnan 1985) as well as drain/source terminals as shown in Figures 3.1 and 3.2 It is also observed from Figures 3.1 and 3.2, that, when the device is getting used as a pass-transistor may conduct current in either direction.

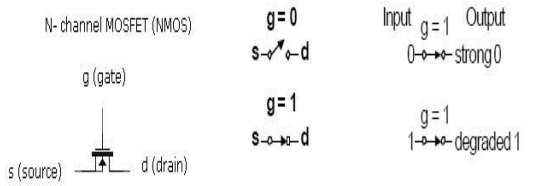


Fig 3.1 NMOS - Pass transistor logic

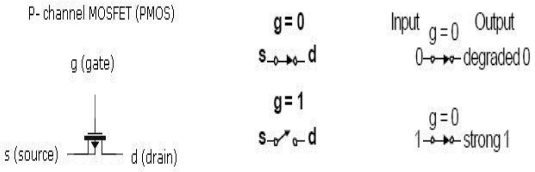


Fig 3.2 PMOS - Pass transistor logic

The NMOS transistors pass a strong logic 0 but a weak logic 1(threshold voltage drop. $High = VDD - V_{thn}$) and PMOS transistors pass a strong logic 1 but a weak logic 0(threshold voltage drop. $Low = V_{thp}$). Thus, NMOS switches are best for pull-down network and the PMOS switches are best for pull-up network. Keeping these in view, the study adopted a quasi-experimental research method.

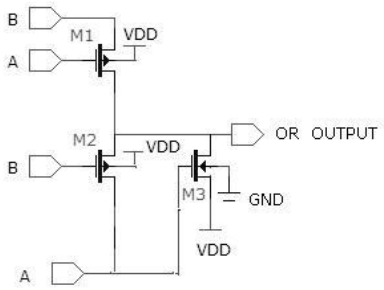


Fig.4 Three transistors based OR gate with PTL

When input A = input B= 0, the two PMOS M1 and M2 are ON and NMOS M3 is OFF. The transistors M1 and M2 functions as a pass transistor (Transistor M1 is more stronger than other transistor M2 and passes B ) giving an output logic zero.

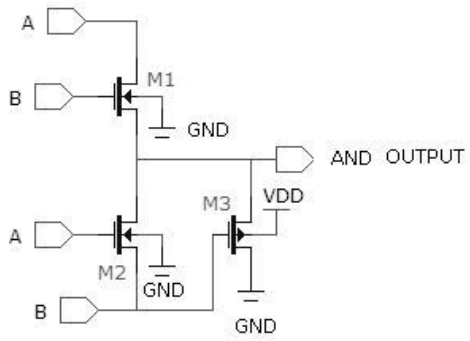


Fig.5 Three transistors based AND gate with PTL

When input A =0 input B= 0, the two NMOS M1 and M2 are OFF and PMOS M3 is ON. The transistors M3 connects the output line to ground giving an output logic zero.

Equivalent of XOR gate design it consist of 2 transistors Q1 and Q2 with A, B as inputs, when inputs A and B both are logic low then Q1 is in ON state and Q2 is in OFF state so that the output is low, when inputs A is low and B is high then Q1 is in OFF state and Q2 is in ON state so that the output is at high in the same way if the input A is high and B is low then Q1 is in ON state and Q2 is in OFF state so that the output is at high, but when both the inputs are at high then output is at low hence the above circuit acts as XOR gate.

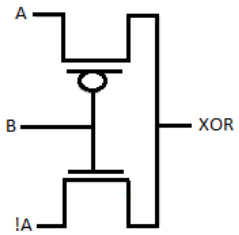


Fig.6 Two transistors based XOR gate with PTL

It reduces the delay and size of the devices compared to single bit flip flop. Generally, the adder libraries consists AND, XOR and OR as majority gates. The register banks are used to store the bit when it is enabled. The proposed designs are done and implemented with better area and delay when compared to conventional designs by using pass transistor logic where we have less number of transistors compared to CMOS based Logic design.

## III. RESULT AND DISCUSSION

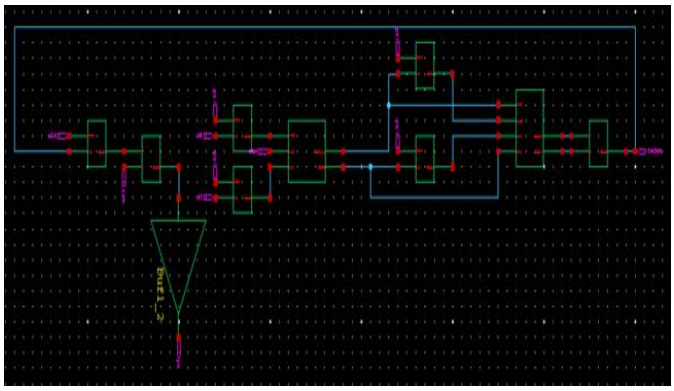

Figure 7. Schematic Diagram for the proposed 2 bit FF

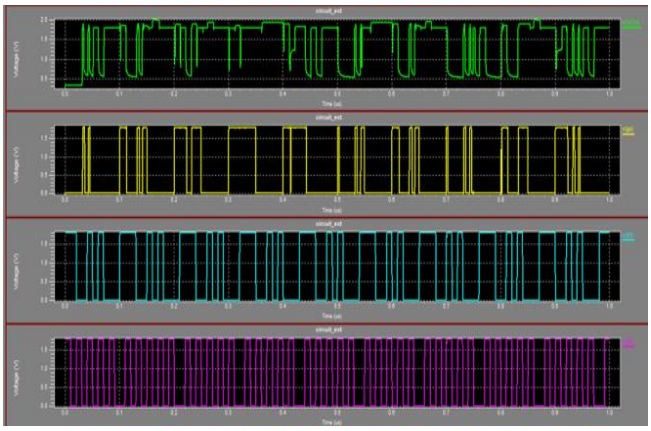

Figure 8. Simulation Diagram for the proposed 2 bit FF

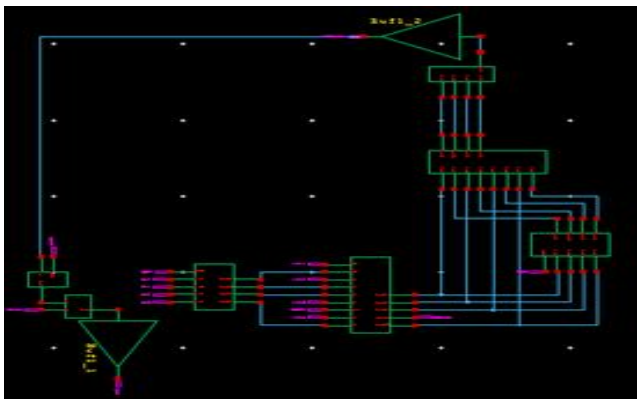

Figure 9. Schematic Diagram for the proposed 4 bit FF

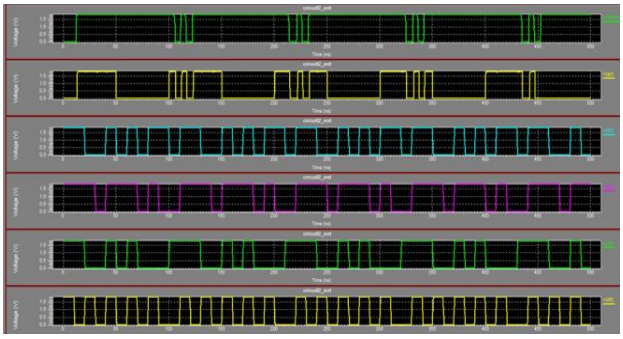

Figure 10. Simulation Diagram for the proposed 4 bit FF

### D. COMPARISON TABLE:

| Design | Area (TC) | Delay(ns) |
|---|---|---|
| 2 bit flip flop existing | 123 | 24.4ns |
| 2 bit flip flop implemented | 89 | 14.83ns |
| 4 bit flip flop existing | 261 | 95.12ns |
| 4 bit flip flop implemented | 189 | 85.93ns |

## IV. CONCLUSION

The objective of the system is to reduce the area, delay & power of data driven clock-gating technique. In proposed method using merging FFs for combined clocking by a shared gate to yield highest dynamic power savings. Analyzed, the results of grouping and merging FFs architectures, simulation and synthesis. As the result of the area, delay parameters, grouping FF using data driven clock gating is more effective than the merging FF using data driven clock gating. In case of grouping FFs using data driven clock gating is extraordinary power saving for merging FFs using data driven clock gating. In this paper, analysis between grouping FFs using data driven clock gating and merging FFs using data driven clock gating and to enhance the performance of the this Multi bit Flip flops we use pass transistor logic which can reduce the transistor count of the circuit so that can have less area and delay of the circuit.

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