Schmitt Trigger Based 4t Sram Cell

R Manishankari[1], DK Nivetha[2], T Pavithra[3], Mr. P F Khaleeleur Rahiman[4]
[1] Dept of Electronics and Communication Engineering
[2]Asst. Professor, Dept of Electronics and Communication Engineering
[1, 2, 3, 4] Hindusthan College of Engineering and Technology, Otthakalnmandapam, Coimbatore, India.

Abstract- *Due to wide-spread use of electronic devices, embedded memories play a significant role in modern era. Due to fast and random access, SRAM is mainly used as a cache memory. But in low power VLSI, Stability degrades due to technology scaling and fluctuations in process parameters that is oxide thickness, diffusion depth and density of impurity concentration etc. Thus to measure stability, static noise margin is the main performance parameter in SRAM cell. This paper presesnts SRAM topologies, conventional 4t and Schmitt Trigger based SRAM bit cell. These two topologies are characterized and compared on the basis of their Read and Write SNM with dynamic power supply.*

Keywords- SRAM, Schmitt Trigger, Topologies, SNM, Dynamic power supply.

I. INTRODUCTION

Fast memory access times are essential to cater the heavy workload needs imposed on PCs and work stations. Many researchers and companies all over the world have been tackling the various problems that accompany the scaling. Static Noise Margin (SNM) is useful performance parameter to measure the stability of a system. Today everyone wants low power, stable and fast accessible device. Though, the high speed devices use SRAM as a cache memory. The main and biggest role of low power SRAM in most of the digital devices is due to their battery life and good stability of portable devices.

II. EXISTING SYSTEM

The conventional 6T SRAM cell is shown in the below diagram.The conventional 6T SRAM cell comprises of two cross coupled inverter. The output of one inverter is connected to input of other and vice-versa. The complementary output of these two inverters is connected to the two access transistors (M5 and M6) which connect the bit and bit-bar lines to the cell. These two access transistors are accessed through word line. A SRAM Cell mainly performs three operations: Hold, Read and Write operations.

III. PROPOSED SYSTEM

The proposed Schmitt Trigger 4T SRAM cell which improves the power and stability of write operation. Much of on-chip storage is devoted to transient, often short lived data. Despite this, virtually all on-chip array structures use Schmitt trigger 4T static RAM cells that store data indefinitely. This makes 4T cells uniquely well-suited for predictive structures like branch predictors and BTBs where data integrity. In the four– transistor (4T) loadless bit cell, pMOS devices act as access transistors. The design requirement is such that pMOS OFF state current should be more than the pull-down nMOS transistor leakage current for maintaining data reliably. With increasing process variations and exponential dependence of the sub-threshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging.

The step by step procedure of the proposed system

- SRAM Read,
- SRAM Write,
- SRAM Sizing.

IV. EXISTING SCHMITT TRIGGER

Schmitt Trigger In the previously reported SRAM cell, the basic element for the data storage is a cross coupled inverter pair. Extra transistors are added to decouple the read and write operations. The cross coupled inverter pair of an SRAM cell operating at low supply voltage consumes high power. So to improve the inverter characteristics, Schmitt Trigger configuration is used. Schmitt trigger is like a comparator which includes positive feedback. The output is high for an input is higher than a chosen threshold value. On the other hand the output is low for an input is higher than a chosen threshold value.

The output retains the value if the input between these two. The Schmitt circuit is a general inverter circuitry (double transistor inverter) with two extra transistors for providing the hysteresis .The Schmitt trigger circuit is shown in Figure 2 .The double transistor inverter is used because the transistors (M2 and M5) have some higher threshold voltage

than M1 and M4 due to body bias effect and due to which the output switches to high from low or low from high when after the ON condition of M2 or M4 respectively. The addition of two more transistors M6 and M3 the circuit is capable to provide hysteresis. When 0 input voltage is applied at the input, both M1 andM2 are in OFF condition while M4 and M5 are in ON condition and output is at high logic level. When the input reaches to threshold voltage of M1 transistor then M1 will be on , while M2 remains OFF and at this time output will be high M3 will be on , so M1 Try to pull down the node between M1 and M2 while M3 try to pulls up this node to voltage VDD-VT , so transistor M2 stays the output to HIGH logic level , now when the input rises up to the threshold voltage of M2 then output switches to low logic level, so effectively our switching point shifted to higher voltage referred as VIH.A Schmitt trigger increases or decreases the switching threshold of the inverter depending upon the direction of input transition .This adaptation is achieved with the help of feedback mechanism.

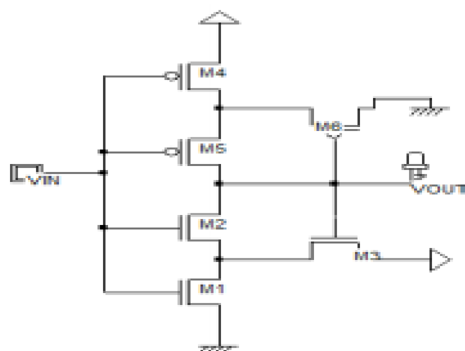

Fig 4.1. 6T Schmitt Trigger

V. PROPOSED SCHMITT TRIGGER

This structure is used to form the inverter of our memory bit cell. The basic Schmitt trigger requires six transistors instead of two transistors to form an inverter. Thus, it would need 14 transistors in total to form an SRAM cell, which would result in large area penalty. Since PMOS transistors are used as weak pull-ups to hold the “1” state, a feedback mechanism in the PMOS pull-up branch is not used. Feedback mechanism is used only in the pull-down path. The modified Schmitt trigger schematic is shown in Figure 3.In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in Figure . During 0 ->1 input transition, the feedback transistor (NF) tries to preserve the logic “1” at output (Vout) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a 0->1 input transition for the inverter storing logic “1,” higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. For the 1->0 input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input dependent transfer characteristics of the Schmitt trigger improves both read stability as well as write ability of the SRAM bit cell.

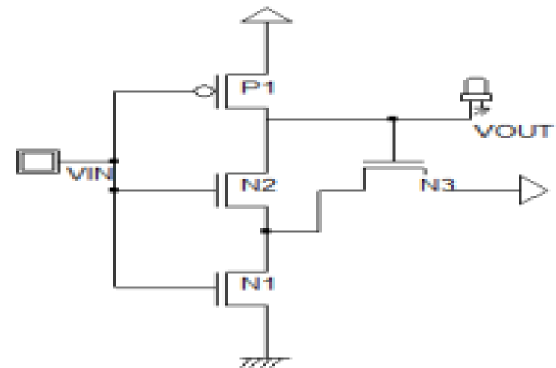

Fig 5.1. 4T Schmitt Trigger

VI. SRAM OPERATION

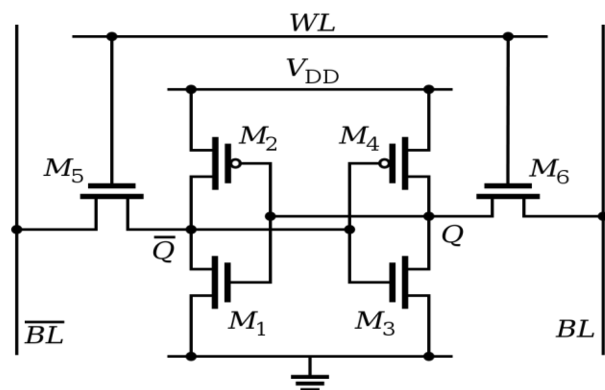

Fig 6.1 SRAM Opration

An SRAM cell has three different states it can be in: *standby* (the circuit is idle), *reading* (the data has been requested) and *writing* (updating the contents). The SRAM to operate in read mode and write mode should have "readeability" and "write stability" respectively. The three different states work as follows:

6.1 Standby

If the word line is not asserted, the *access* transistors M_5 and M_6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M_1 – M_4 will continue to reinforce each other as long as they are connected to the supply.

6.2 Reading

Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by precharging both the bit lines to a logical **1**, then asserting the word line WL, enabling both the *access* transistors. The second step occurs when the values stored in Q and Q are transferred to the bit lines by leaving BL at its precharged value and discharging BL through M_1 and M_5 to a logical **0** (i. e. eventually discharging through the transistor M_1 as it is turned on because the Q is logically set to **1**). On the BL side, the transistors M_4 and M_6 pull the bit line toward V_{DD}, a logical **1** (i. e. eventually being charged by the transistor M_4 as it is turned on because Q is logically set to **0**). If the content of the memory was a **0**, the opposite would happen and BL would be pulled toward **1** and BL toward **0**. Then these BL and BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was **1** stored or **0**. The higher the sensitivity of sense amplifier, the faster the speed of read operation is.

6.3 Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, we would apply a **0** to the bit lines, i.e. setting BL to **1** and BL to **0**. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A **1** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

6.4 Bus behavior

A RAM memory with an access time of 70 ns will output valid data within 70 ns from the time that the address lines are valid. But the data will remain for a hold time as well (5-10 ns). Rise and fall times also influence valid timeslots with approximately ~5 ns. By reading the lower part of an address range bits in sequence (page cycle) one can read with significantly shorter access time (30 ns).

VII. CHARACTERISTICS

SRAM is more expensive, but faster and significantly less power hungry (especially idle) than DRAM. It is therefore used where either bandwidth or low power, or both, are principal considerations. SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM. Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

VIII. APPLICATIONS

Clock rate and power

The power consumption of SRAM varies widely depending on how frequently it is accessed; it **can** be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draw very little power and can have a nearly negligible power consumption when sitting idle — in the region of a few micro-watts.

Static RAM exists primarily as:

- general purpose products
- with *asynchronous* interface, such as the 28 pin 32Kx8 chips (usually named XXC256), and similar products up to 16 Mbit per chip.
- with *synchronous* interface, usually used for caches and other applications requiring burst transfers, up to 18 Mbit (256Kx72) per chip.
- integrated on chip
  - as RAM or cache memory in micro-controllers (usually from around 32 bytes up to 128 kilobytes)
  - as the primary caches in powerful microprocessors, such as the x86 family, and many others (from 8 kB, up to several megabytes)
  - to store the registers and parts of the state-machines used in some microprocessors (see register file)
  - on application specific ICs, or ASICs (usually in the order of kilobytes)
  - in FPGAs and CPLDs.

IX. ADVANTAGES

- Eliminates the errors During the read operation
- The noises in the circuit is decreased
- No of transistor can be reduced than the sense amplifier circuit.
- Consumes low power.

X. CONCLUSION

The Schmitt trigger based single-ended, robust, 6-transistor SRAM bitcell suitable for subthreshold operation. The ST based 6t bitcell achieves higher read SNM (1.6×) compared to the conventional 6T cell.The higher SNM can be achieved by modifying the device parameters of ST based 4T SRAM.

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