Design And Implementation of Low Power Sequential Circuits Using GDI Technique

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Abstract- *GDI (Gate Diffusion Input) - a new technique of low power digital circuit design is described. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various PTL design techniques is presented, with respect to the layout area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI as compared to other methods. AND and NAND logic gates have been implemented in 250nm technology to compare the GDI technique with CMOS and PTL. Showing up to 45% reduction in power-consumption in GDI. Properties of D Flip flop using GDI are discussed, simulation results are reported and measurements are presented.*

Keywords- CMOS technology, PTL, Gate Diffusion Input Technique, low power design Flip-flop

I. INTRODUCTION

With rapid development of portable digital applications, the demand for increasing speed, compact implementation and low power dissipation triggers numerous research efforts [2,3]. The wish to improve the performance of logic circuits, once based on traditional CMOS technology, results in developing of many logic design techniques during the last two decades. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Formal methods for deriving pass-transistor logic have been presented for NMOS. They are based on the model, where a set of control signals is applied to the gates of n-transistors. Another set of data signals are applied to the sources of the n-transistors [2]. Many PTL circuit implementations have been proposed in the literature [2,3,4,5,8]. Some of the main advantages of PTL over standard CMOS design are: (1) High speed - due to the small node capacitances, (2) Low power dissipation - as a result of the reduced number of transistors, (3) Lower interconnection effects [6,7] - due to a small area. However, most of the PTL implementations have two basic problems. First, the threshold drop across the single-channel pass transistors results in reduced current drive and hence slower operation at reduced supply voltages; this is particularly important for low power design since it is desirable to operate at the lowest possible voltage level. Second, since the "high" input voltage level at the regenerative inverters is not Vdd, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant [4]. An additional problem of existing PTL is top-down logic design complexity, which prevents from the pass-transistors capturing a major role in real logic LSl's. One of the main reasons for this is that no simple and universal cell library is available for PTL based design. GDI (Gate Diffusion Input technique) - a new low power design technique, which allows solving most of the problems mentioned above was presented in [10]. GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low power circuits, using reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving power characteristics and allowing simple Shannon's theorem-based design [10] by using small cell library.

The aim of this work is to design a D flip flop using GDI technique

Section II presents the operation of AND gate using GDI technique the comparison of conventional AND gate and AND gate using GDI technique. Section III shows the NAND gate using GDI technique and its output. Section IV layout and its rules. Section V shows the convention D flip flop with the power results. Section VI D flip flop using GDI technique with power results. Section VII future scope has been mentioned

II. AND GATE USING GDI TECHNIQUE

Conventional and gate: conventional AND gate requires 4 transistors as shown below

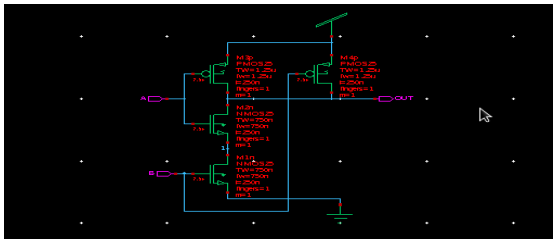

Fig1:Schematic of Conventional AND gate

AND GATE USING GDI TECHNIQUE:

Generally we require 4 transistors (2 PMOS, 2NMOS) for the design of AND gate but by using GDI technique we reduced to 2 transistors as shown in below fig...

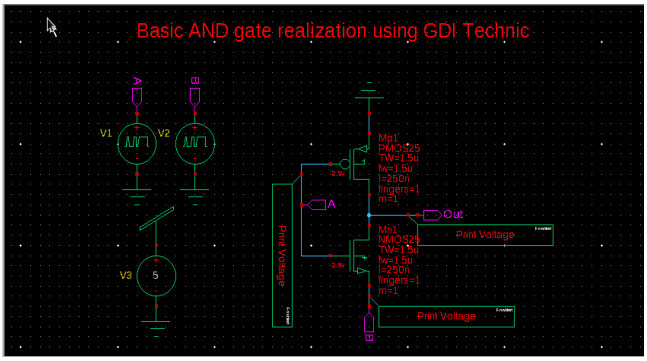

Fig 2: schematic of AND gate using GDI technique

The AND gate consists of two inputs A , B and one output named as OUT. The truth table of AND gate is shown below..

OUT=A . B

Table 1: AND gate truth table

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Now the truth table is divided into two parts such as the inputs (00, 01) as part1 and the inputs (10, 11) as part 2.
In part 1 from the truth table by observing the inputs and output the output follows the input A irrespective of input B. By using the same logic the input A is taken as selection input.

input A = 0 (PMOS transistor will be on and NMOS will be off even though the PMOS transistor is on however it is connected to ground then the output will be 0)

In part 2 from the truth table by observing the inputs and output the output follows the input B irrespective of input A. Here the input A =1 (PMOS will be off NMOS will be on so that

Input B=0, output = 0
Input B=1, output = 1
Hence the AND gate using GDI technique satisfy the truth table of conventional AND gate.

OUTPUT OF AND GATE:

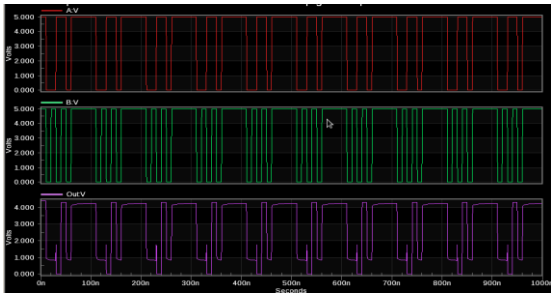

Fig 3: Output of AND gate using GDI technique

III. NAND GATE USING GDI TECHNIQUE

As we reduced AND gate to two transistors by connecting an inverter to the optimized AND gate we will obtain a NAND gate. The schematic of NAND gate using GDI technique is shown below.....

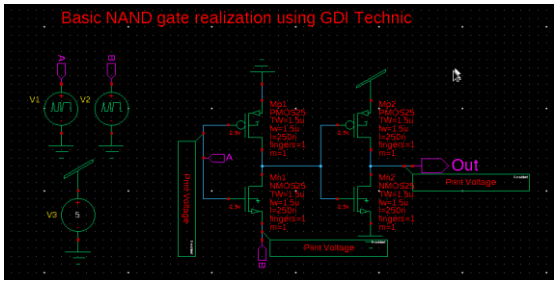

Fig 4: Schematic of NAND gate using GDI technique

As we know that the output of NAND gate is complementary to AND gate so that we connected an inverter to the optimized AND gate this inverter complements the output of And gate and gives the output of NAND gate using gdi technique

OUT = (A.B)'

The truth table of NAND gate is shown below.

Table 2: NAND gate truth table

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

OUTPUT OF NAND GATE:

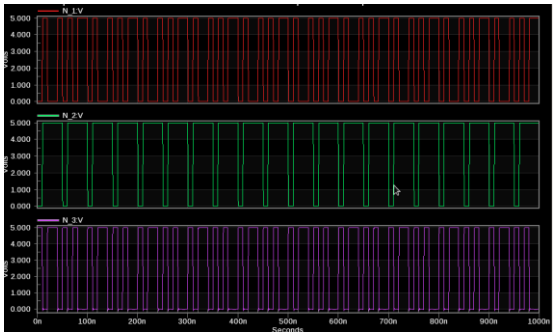

Fig 5: Output of NAND gate using GDI technique

IV. RULES OF LAYOUT

LAYOUT OF AND GATE: The layout of the schematic of AND gate using GDI technique is shown below.

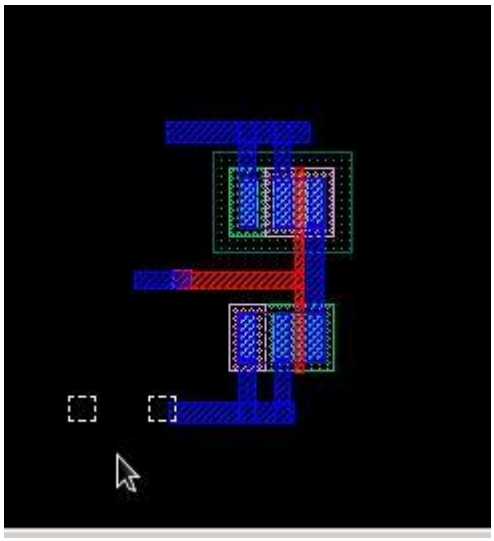

Fig 6: AND gate layout

PMOS LAYOUT: As the length between the source and drain is 250nm we are using 250nm Technology

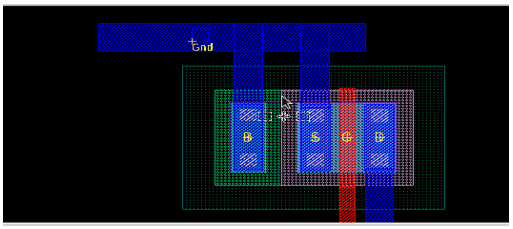

Fig 7:PMOS layout

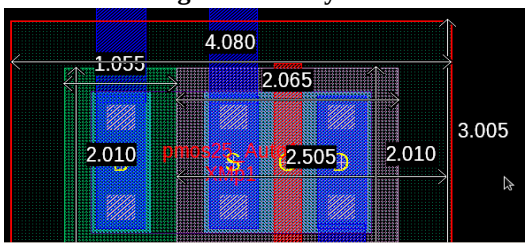

Fig 8: Measures of PMOS layout

These are the minimum lengths and widths used but we can use up to maximum extent as per our requirement.

Table 3: Measures of PMOS layout

PMOS			
S. NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	N-WELL	2.995 micrometer	4.110 micrometer
2.	SUBSTRATE	1.050 micrometer	1.050 micrometer
3.	PIMPLANT	2.005 micrometer	2.065 micrometer
4.	GATE	2.100 micrometer	0.250 micrometer
5.	METAL	1.140 micrometer	0.545 micrometer
6.	GROUND	4.170 micrometer	0.645 micrometer

NMOS LAYOUT:

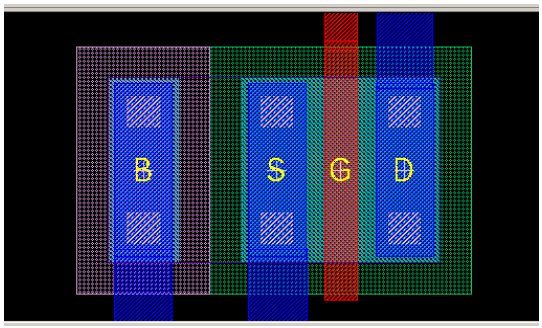

Fig 9: NMOS layout

Table 4: Measures of NMOS layout

NMOS			
S. NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	P-WELL	2.045 micrometer	2.000 micrometer
2.	SUBSTRATE	1.990 micrometer	1.010 micrometer
3.	N IMPLANT	1.550 micrometer	1.495 micrometer
4.	GATE	2.095 micrometer	0.250 micrometer
5.	METAL	3.710 micrometer	0.625 micrometer

V. CONVENTIONAL D FLIP FLOP

The schematic of conventional D flip flop is shown below.

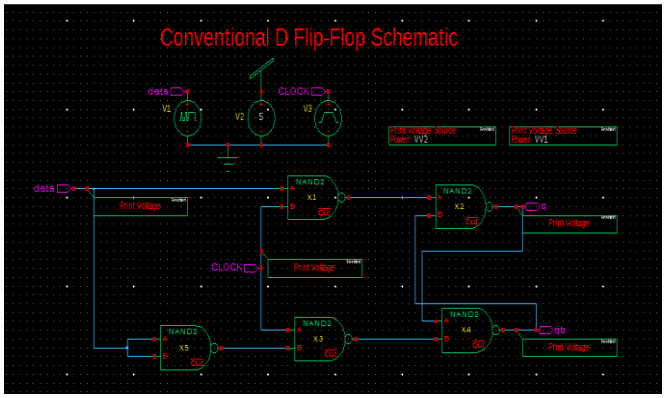

Fig 10: Schematic of conventional D flip flop

For this D flip flop we analyzed the power consumption and power delivered

There are two types of power
1.Static power
2.Dynamic power

Static power: Static power is power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input have active inputs (i.e., all inputs are "static" because they are at fixed dc levels).

Dynamic power: Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

We use **T-spice** commands to get the results of dynamic power

.power voltage source or resistor through which to compute power dissipated start time end time

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Power Results

VV2 from time 1e-10 to 1e-06
Average power consumed -> 1.254913e-04 watts
Max power 8.003834e-03 at time 1.00521e-07
Min power 8.901370e-09 at time 3.06e-07

VV1 from time 1e-10 to 1e-06
Average power consumed -> 2.321915e-06 watts
Max power 5.363479e-04 at time 8.60776e-07
Min power 0.000000e+00 at time 1e-10
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VI. D FLIP FLOP USING GDI TECHNIQUE

The D flip flop is designed by using 5 NAND gates. The schematic of D flip flop using GDI technique is shown below.

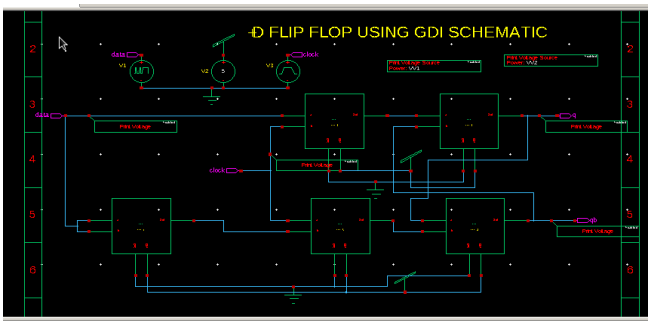

Fig 11: Schematic of D flip flop using GDI technique

For this D flip flop using GDI technique we analyzed the power consumption and power delivered

Power Results

VV1 from time 1e-10 to 1e-06
Average power consumed -> 1.047242e-05 watts
Max power 8.278281e-04 at time 7.11e-07
Min power 0.000000e+00 at time 1e-10

VV2 from time 1e-10 to 1e-06
Average power consumed -> 2.597747e-04 watts
Max power 1.157815e-02 at time 8.60682e-07
Min power 2.426567e-08 at time 6.62916e-07

By comparing the power consumption and power delivered values in conventional D flip flop and D flip flop using GDI technique we can observe that

1. Power consumption in D flip flop using GDI technique is (1.2746734e-01) less than the power consumption in conventional D flip flop
2. Power delivered in D flip flop using GDI technique is (1.342835) greater than the power delivered in conventional D flip flop.

Table 5: Comparison of power consumed and power delivered in GDI technique and conventionally

S. NO	TECHNIQUE	VV1 (power consumption)	VV2 (power delivered)
1	Conventional D flip flop	2.321915e-06watts	1.254913e-04watts
2	D flip flop using GDI	1.047242e-05watts	2.597747e-04watts

Output of D Flip Flop Using GDI Technique:

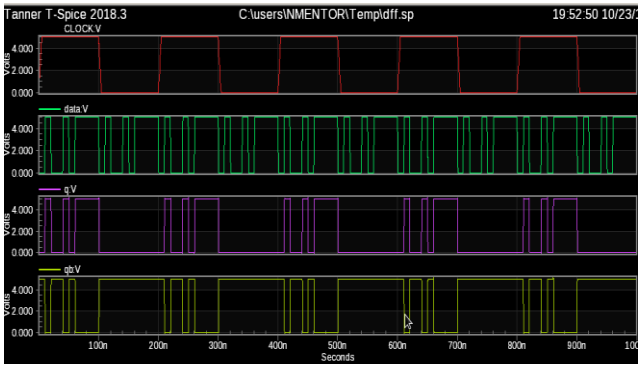

Fig 12: Output of D flip flop using GDI technique

By observing the waveform when clock is equal to 1 then the output (q) will same as data. The output (qb) is complement to the output (q).

VII. FUTURE SCOPE

The main focus of this paper is to design low power D Flip-flop circuit. This paper proposes the gate diffusion input technique to design the Flip-flop for achieving high speed operation in DSP applications. This is a better style when compared with the existing CMOS design in terms of area, Speed and power dissipation. The total transistor count is reduced to 24 in comparison with CMOS style that has total number of transistors as 96 and also the power has been reduced in the great amount of around 50%. Thus this logic style has created a better platform for the design of the sequential circuits. These results were obtained with spice simulation in Mentor graphics tool

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