Design Of Low Power Voltage Doubler Circuit For Power Harvesting Applications

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Abstract- *Implementation of power efficient and reliable device requires high end batteries and sustainable energy's. The major drawback of this sustainable energy is that, the low voltage generation makes it difficult to drive the device. To overcome this side-effect we make use of voltage doubler (DC-DC converter) circuit to convert low voltage to high voltage where it can able to drive the circuit and used in energy/power harvesting applications. Considering the ideal voltage doubler circuit in cmos circuit design and analyse the performance in terms of power and delay. Instead of using capacitor in the ideal voltage doubler circuit we make use of MOS capacitor which has less delay and less power dissipation than the ideal voltage doubler circuit. Later we modified the cmos inverter in the ideal voltage doubler circuit using FinFet inverter where the power dissipation of the FinFet inverter based voltage doubler (in uW) reduces futhermore than the ideal voltage doubler and the MOS capacitance voltage doubler (in mW) which can be utilized in the energy harvesting application.*

I. INTRODUCTION

In the modern era progress in the innovation of wired gadgets and small scale remote wearable frameworks is important to build up a low power consuming frameworks. To do so we require high end petroleum products, batteries and supportable vitality. Because of rising energy cost and decrease of assets we move to very good quality batteries, though in batteries it requires high supply to work the gadgets which makes the gadget more power subordinate. So we utilize feasible energy sources for example, piezoelectric, photovoltaic and thermoelectric [1].The principle disadvantage of utilizing this manageable vitality is their low voltage generation, which is the fundamental pleat of utilizing this gadgets. Thus, in the ongoing year, part of research has been occurred to create a proficient DC-DC converter, which is equipped for changing over low voltage level to higher voltage level with high productivity and low power utilization. Self-one-sided exchanging controller is utilized for efficient DC-DC converters. Considering the fundamental block of DC-DC boost converteras described in figure 1[1]

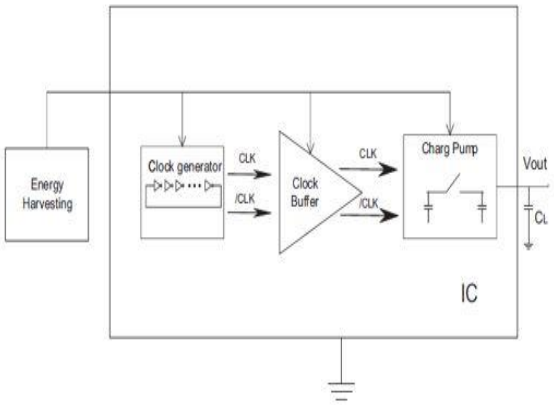


Figure 1: Integrated DC-DC converter [1]

A completely coordinated capacitive DC-DC voltage converter which essentially comprises of three area clock generator, clock buffer and charge pump.

The clock generator is utilized produce the necessary clock sign and equivalent timing of the voltage doubler circuitry for minimum DC input voltage. Clock buffer are used for high drive and to produce exact square wave. The charge pump of exchanged capacitor circuit convert low DC input voltage to high DC yield voltage. The charge siphons are various sorts and can incorporate different advance or multi-stage structures. These three area in the incorporated circuit are provided by the TEG energy harvester utilized in biomedical applications and furthermore can be utilized in low power applications.

1.2 THE CHARGE PUMP

A circuit of single stage voltage doubler is considered in the figure 2[12] .where as vck1 and vck2 are two inputs given to the circuit. Process of the circuit is given in two steps

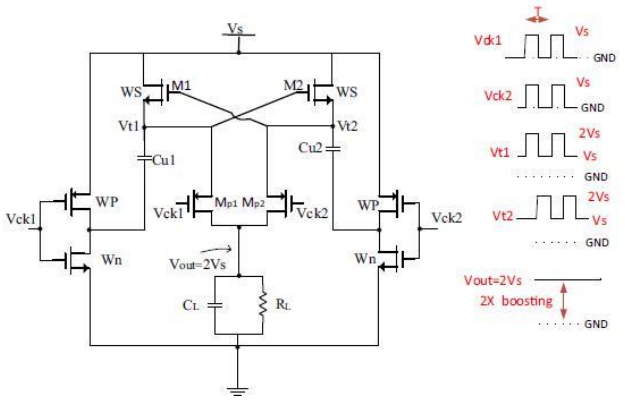


Figure 2: Voltage Doubler Circuit [12]

1) When clock1=0 and clock2=1:

Wp turns ON and Wn turns OFF.M2 turns ON where vt2= VS. Due to this the capacitor is charged to VS [cu2=VS].Because of the previous clock input the capacitor cu1 is charged to VS, so the output of the circuit becomes 2 VS [Vout=2VS]

2) When clock1=1 and clock2=0:

Wp turns ON and Wn turns OFF.M1 turns ON where vt1= VS. Due to this the capacitor is charged to VS [cu1=VS].Because of the previous clock input the capacitor cu2 is charged to VS, so the output of the circuit becomes 2 VS [Vout=2VS]

II. VOLTAGE DOUBLER USING MOS CAPACITOR

In order to reduce the power consumption and delay in the circuit, we make use of the MOS capacitor instead of normal capacitor in the ideal voltage doubler circuit. The main advantage is that it reduces the capacitor effect in the circuit. By using a MOS capacitor it reduces the complexity of the circuit during the fabrication process. MOS capacitor is nothing but metal oxide semiconductor capacitor where it has three terminals gate, drain and source. By shorting source and drain we make it as a MOS capacitor. The output of the circuit Vout is 3.045V.

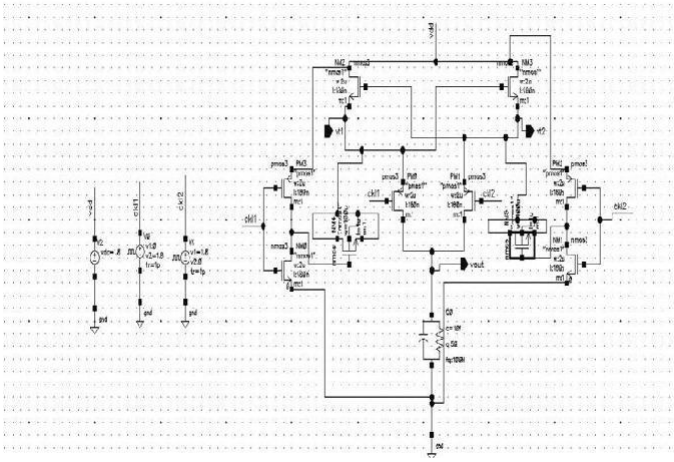


Figure 3: MOS Capacitor Voltage Doubler

2.1 IDEAL VOLTAGE DOUBLER WITH FINFETINVERTER

So as to lessen the power utilization in the circuit, we utilize FINFET inverter rather than typical inverter in the perfect voltage-doubler circuit. The main advantage is to reduce the second-order effect in the circuit. By using FINFET inverter it reduces the complexity of the circuit during the fabrication process and also consumes less area. FINFET is nothing but fin field-effect transistor, here the directing Channel is wrapped by a dainty silicon "fin" which frames the gate of the gadget. The output of the voltage doubler with FINFET inverter Vout is 3.32V.

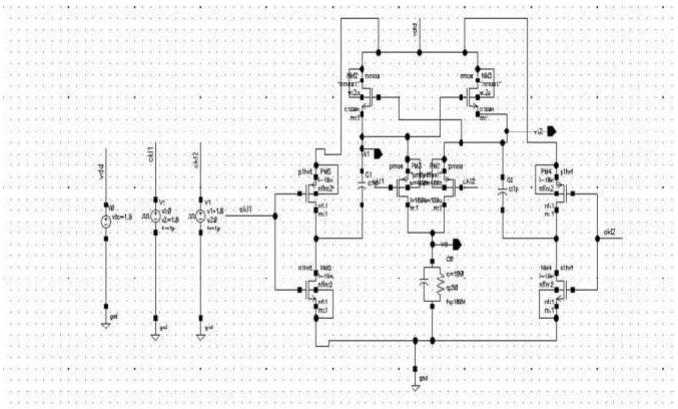


Figure 4: Voltage Doubler with FINFET inverter

2.2 VOLATGE DOUBLER CIRCUIT WITH FINFET INVERTER USING MOS CAPACITANCE

So as to lessen the power utilization and delay in the circuit, we make use of the MOS capacitor instead of a normal capacitor in the ideal voltage doubler circuit with FINFET inverter. The main advantage is that it reduces the capacitor effect in the circuit. By using a MOS capacitor it reduces the complexity of the circuit during the fabrication process. MOS

capacitor is nothing but metal oxide semiconductor capacitor where it has three terminals gate, drain and source. By shorting source and drain we make it as an MOS capacitor. Output of the circuit Vout is 3.3V

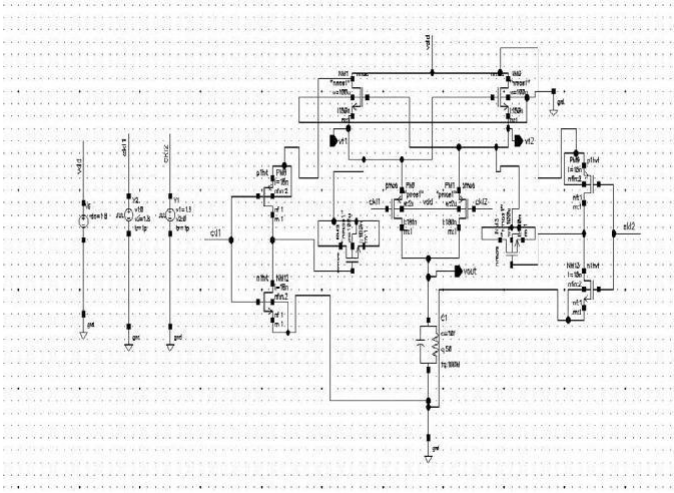
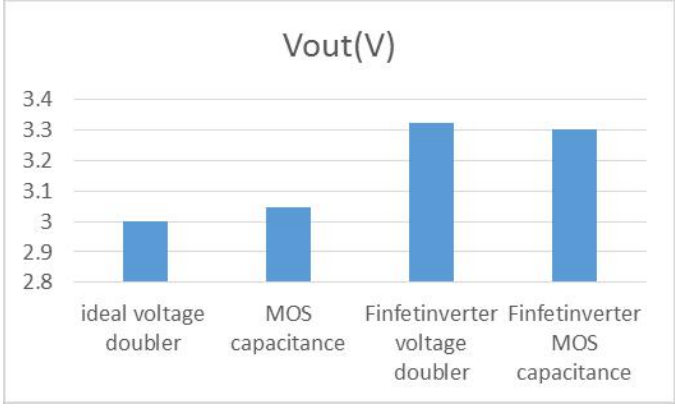
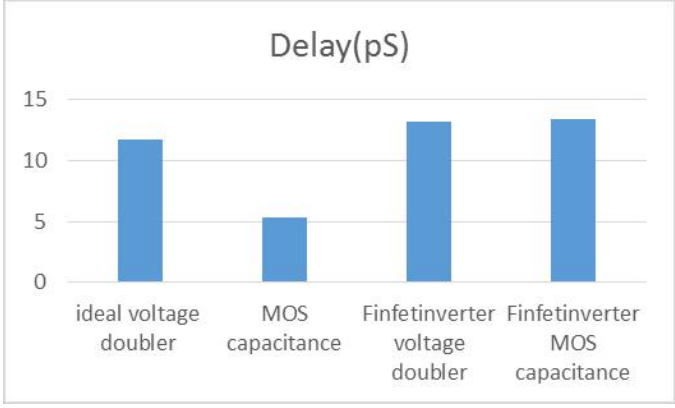


Figure 5: Voltage Doubler with FINFET inverter using MOS Capacitance

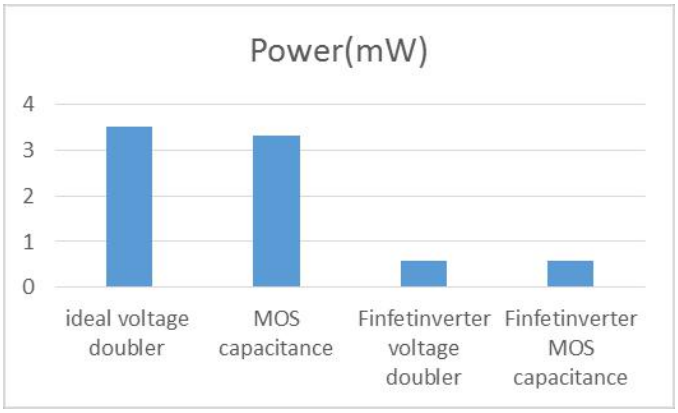
III. RESULTS



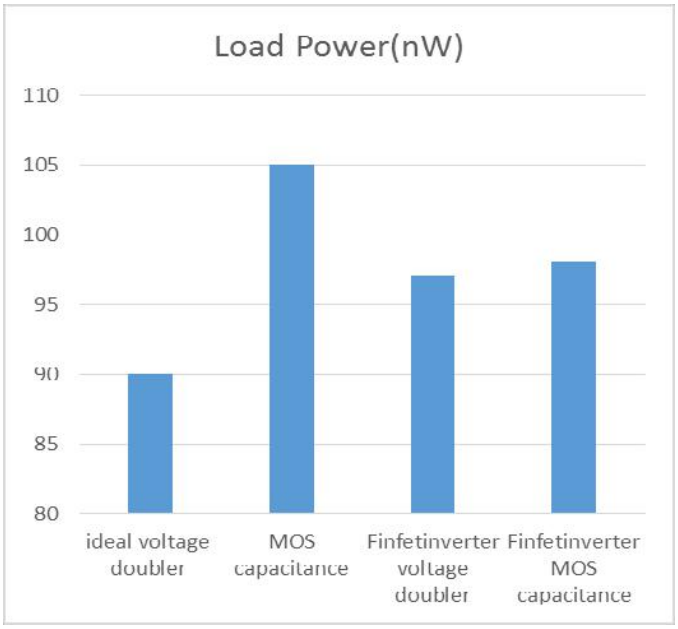
(a)



(b)



(c)



(d)

Figure 6: Comparison of four circuits: (a) output voltage, (b) delay, (c) power dissipation, (d) load Power

IV. CONCLUSION

This paper presents a low-power, fully integrated DC-DC converter for energy harvesting application based on different voltage doubler structure. Initially capacitor in the ideal voltage doubler is replaced by the MOS capacitance which improves the performance of the circuit in terms of delay 6.113 X E-12 seconds and power dissipation is 3.588mW and load power 85.01nW when compared to the ideal voltage doubler circuit. Also, the cmos inverter circuit at the input stage is modified with the FINFET inverter to further improve the performance of the circuit. Whereas the power dissipation reduces to 570uW for MOS capacitance voltage doubler with FINFET inverter circuit which is less when compared to the other voltage doubler circuits. Load power of the MOS capacitance voltage doubler with FINFET inverter circuit is 96nW which is less when compared to ideal voltage

doubler circuit, MOS capacitance voltage doubler and voltage doubler using FinFet inverter.

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