Design Of Dc-Dc (Vmc) Converter For Solar Energy System

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Abstract- *This paper introduces the use of the voltage multipliertechniqueappliedtotheclassicalnonisolatedDcDcconverters. The major benefits obtained with the integrationof voltage multipliers with classical converters are the operation withhighstaticgain,reductionofthemaximumswitchvoltage, zero current switch turn-on and minimization of the effects of thereverserecoverycurrentofalldiodeswiththeinclusionofasmall inductance. The voltage multiplier also operates as a regenerative clamping circuit, reducing problems with lay-out andtheEMIgeneration.Thesecharacteristicsallowstooperatewith high static again, high efficiency and to obtain a compact circuit for applications where the isolation is not required.The principle of operation, the design procedure and practical results obtained from the prototype arepresented.*

I. INTRODUCTION

There are several applications powered by batteries or others low voltage storage elements, as embedded systems, renewable energy systems, fuel cells and interruptible power supply (UPS). These applications demand the development of high performance and high step-up Dc-Dc converters. Some classical converters with magnetic coupling as fly back or current-fed push-pull converters can easily achieve high step-up voltage gain. However the transformer leakage energy can cause high voltage stress, large switching losses, EMI problems and power losses in dissipative clamping circuits, reducing the converter efficiency. Some topologies as the active clamping current-fed push-pull converter can use the leakage energy to obtain soft-commutation, reducing the losses and minimizing the EMI generation. However the voltage stress is higher than in the hard-switching structures and the cost and circuit complexity are increased.

The weight, volume and losses of the power transformeris also a limitation of the isolated Dc-Dc converters for embedded applications. Some non-isolated Dc–Dc converters, as the classical boost, can provide high stepupvoltagegain,butwiththepenaltyofhighvoltageandcurrent stress, high duty-cycle operation and limited dynamic response [1,2,3]. The diode reverse recovery current also can reduce the efficiency when the converter operates with high current and voltagelevels.

There are others non isolated topologies that can operate with large conversion ratios as the quadratic boost and with auxiliary circuits can obtain soft-switching, but the switch voltage is equal to the output voltage, increasing the losses. The use of voltage multiplier in low frequency rectifiers is a classical solution to increase the Dc output voltage. This technique is also used in high-frequency isolated Dc-Dc converters, mainly for high output voltage (kV) applications as in Travelling Wave Tube Amplifiers (TWTA), reducing the problems presented by high frequency and high-voltage power transformer[4].

However, the voltage multiplier technique can be also integrated with non-isolated Dc-Dc converters, obtaining new operation characteristics. The major benefits obtained are the operation with high static gain, reduction of the maximum switch voltage, zero current switch turn-on and minimization of the effects of the reverse recovery current of all diodes with the inclusion of a small inductance. The voltage multiplier also operates as a regenerative clamping circuit, reducing problems with lay-out and the EMI generation.Thesecharacteristicsallowstooperatewithhigh static again, high efficiency and to obtain a compact circuit for applications where the isolation is notrequired.

II. PROPOSEDSTRUCTURE

The proposed topology is presented in Fig. 1. The voltage multiplier cell, composed by the diodes D_{M1}-D_{M2}, the capacitors C_{M1}-C_{M2} and the resonant inductor L_r, is associated with a classic boost converter, composed by the switch S, input inductor L_{in}, output diode D_o and capacitor filter C_o.

When the power switch is turned-off, the capacitor C_{M1} is charged with a voltage equal to the classical boost output voltage. When the power switch is turned-on, the energy stored in the capacitor C_{M1} is partially transferred to the capacitor C_{M2} and the voltage in this capacitor is approximately equal to the C_{M1} voltage. Therefore, the output voltage of the boost converter integrated with the voltage multiplier is twice the output voltage of the classical boost converter. However, in both structures the switch voltages are equals. Thus it is possible to obtain high static gain without increase the switch voltage. This characteristic allows using low drain-source voltage and low R_{DSon} MOSFETs, reducing the switch conduction losses.

As in the classical voltage multipliers, the number of multiplier stages connected in series can be increased in order to obtain higher static gain.

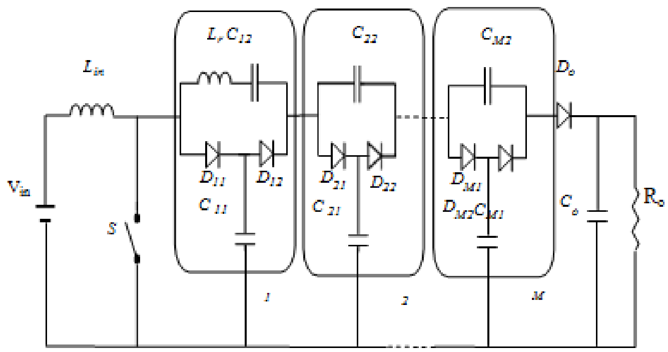

Fig. 2. Boost converter with "M" voltage multiplier cells.

The proposed topology with M multiplier stages is presentedinFig.2.Inthiscase,onlyoneresonantinductorin the first multiplier stage is necessary to ensure the adequate operationcharacteristics.

The voltage multiplier cell increases the static gain of the classical boost by a factor (M+1), where M is the number of multiplier cells. Therefore, the output voltage is (M+1) times higher than the maximum switch voltage.

The voltage multiplier cell also can operate without the resonant inductor L_r. However, the inclusion of this small inductance allows to obtain zero-current-switching (ZCS) turn-on and the negative effects of the reverse recovery current of all diodes is minimized. Thus the current transitions in all components occur in a resonant way, with low di/dt. This characteristic reduces the converter commutation losses, allowing the operation with high switching frequency, maintaining high efficiency.

The multiplier capacitors connected with the negative terminal of the input voltage can be also integrated with the output capacitance, as presented in Fig. 3. With this configuration, the voltage in each output capacitor is half of the output voltage. A symmetrical output voltage can be obtained even for asymmetric loads, considering the reference in the capacitor center point.

The voltage multiplier cell can be integrated with the others basics Dc-Dc converters, as presented in Fig. 4. However, as the boost converter presents the highest static gain of the basic structures, only the analysis of the boost converter integrated with the voltage multiplier is studied in this paper. But the operation characteristic presented for the boost converter is similar for the others structures.

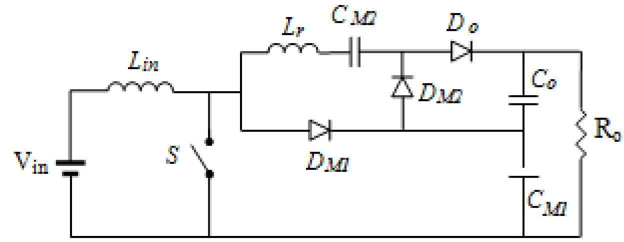

Fig. 3.Integration of the voltage multiplier capacitor with the output.

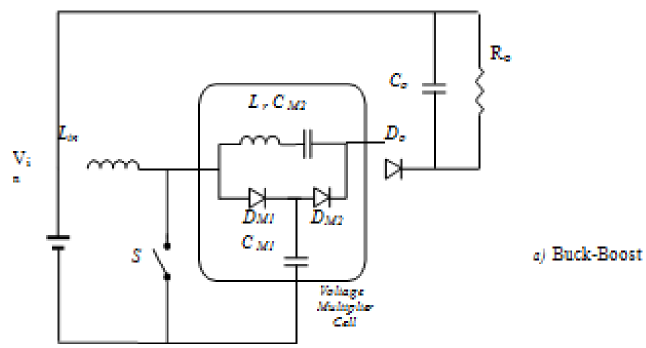

Fig. 4. Voltage Multiplier cell integrated with others classical Dc-Dc converters.

III. OPERATIONANALYSIS

The operation of the proposed converter can be presented in four operation stages. Better operation characteristicsare obtained when the converter operates in continuous conduction mode (CCM). Thus, the operation stages (Figs 5 to 8) and the theoretical waveforms (Fig. 9), are presented for the CCMoperation.

1) First Stage ([t_o, t_1] Fig.5)

At the instant t_0, switch S is turned-off and the energy stored in the input inductor L_{in} is initially transferred to the multiplier capacitor C_{M1} through the diode D_{M1}.

The resonant inductor current (i_{Lr}) rise linearly from zero untiltoreachthevalueoftheinputinductorcurrent(i_{Lin})and thecurrentinthediodeD_{M1}isreducedatsameproportion. Theresonantinductorcurrentchargestheoutputcapacitor C_o through the diodeD_o.

2) Second Stage ([t_1, t_2] Fig.6)

At the instant (t_1), the current in the diode D_{M1} is zero and this diode is blocked with low di/dt, minimizing the diode reverse recovery current. The resonant inductor current is equal to the input inductor current during this stage and the energy of the input inductor is transferred to the load through the diode D_o.

3) Third Stage ([t_2, t_3] Fig.7)

At the instant (t_2), the switch S is turned-on with ZCS commutation and the current in the resonant inductor L_r and in the output diode D_o reduce linearly until zero, at the instant (t_3). Thus the reverse recovery current of the output diode is also minimized.

4) Fourth Stage ([t_3, t_3]Fig.8)

When output diode is blocked, D_{M2} conducts transferring part of the energy stored in the capacitor C_{M1} to the capacitor C_{M2}, in a resonant way. When there is a balanceof energy between the multiplier capacitors, the diode $D_{M2}$is blocked (t_4) also with low di/dt. During the switch turn-on the input inductor stores energy as the classical boost.

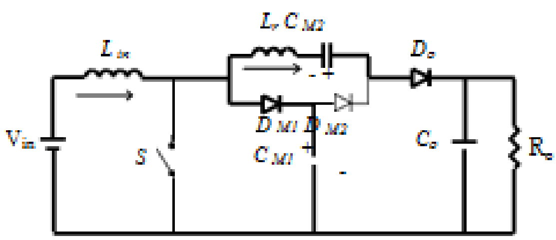

Fig. 5. First Stage (t_0, t_1)

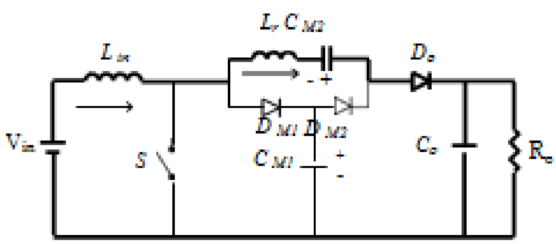

Fig. 6. Second Stage (t_1, t_2)

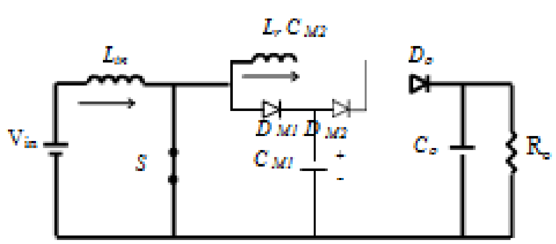

Fig. 7. Third Stage (t_2, t_3)

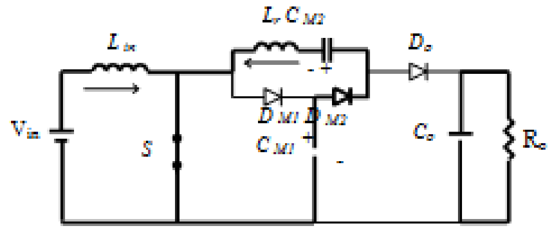

Fig. 8. Fourth Stage (t_3, t_4)

IV. EXPERIMENTALRESULT

The practical aspects of the proposed converter and the design procedure developed are verified with the implementation of two laboratory prototypes. The power circuits implemented and the components used are shown in Figs. 10 and 11.

The specifications of the prototype of Fig. 10 are presented in design procedure and the specification of the prototype of Fig. 11 are presented below.Output power:100W Input Voltage: 12V Output Voltage: 100VSwitching Frequency: 40kHzApproximately by (7), where the current ripple in the input inductance (i_{Lin}) is not considered.

The main waveforms obtained from the prototype of Fig. 10 are presented in Figs. 12, 13, 14, 15 and 16.

Thevoltageandcurrentofthepowerswitchareshownin Fig12.Themaximumswitchvoltageisequalto55Vforan output voltage equal to100V.

The detail of the turn-on commutation can be observed in Fig.13. The turn-on commutation occurs with zero current and the commutation loss is reduced.

The multiplier capacitor C_{M1} also operates as a clamping capacitor, eliminating the switch overvoltage due to the lay problems. As presented in the theoretical analysis, this inductancereduces the di/dt in all diodes, minimizing the effects of the diodes reverse recoverycurrent.

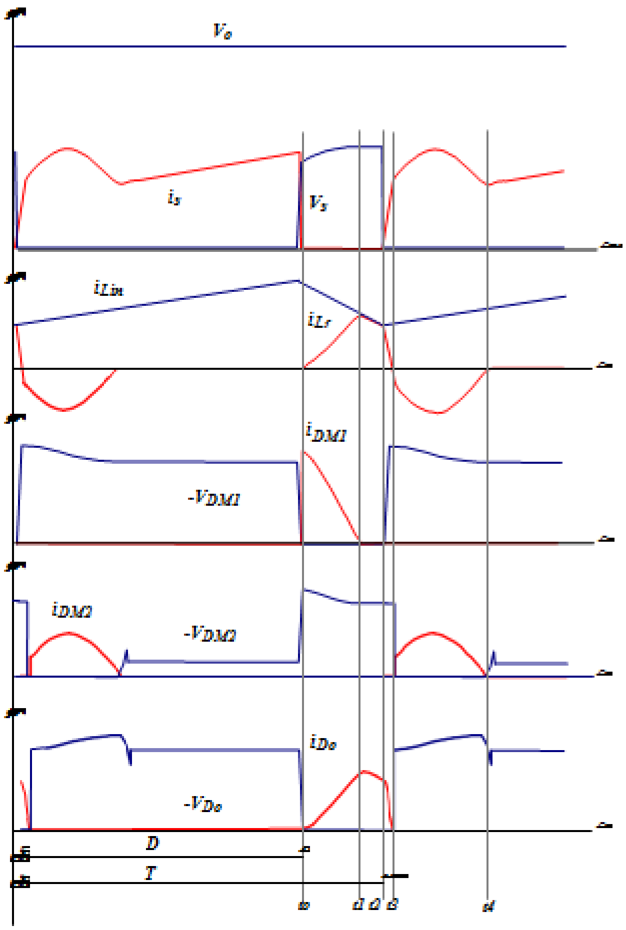

Fig. 9. Main theoretical waveforms

Output power: 100W
Input Voltage: 12V
Output Voltage: 100V
Switching Frequency: 40kHz

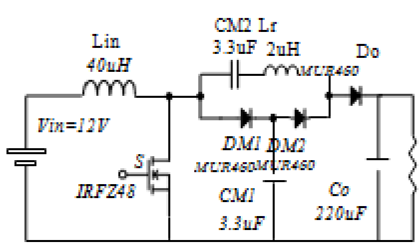

Fig. 10. Power circuit of the prototype implemented (M=1

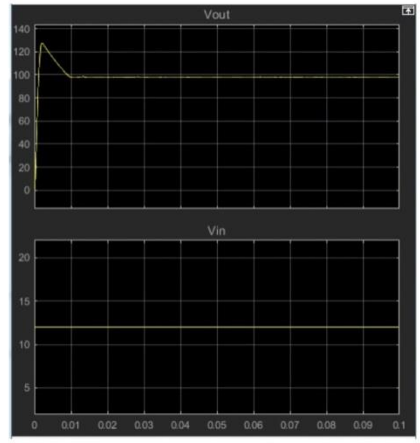

Fig.11. input and output voltage.

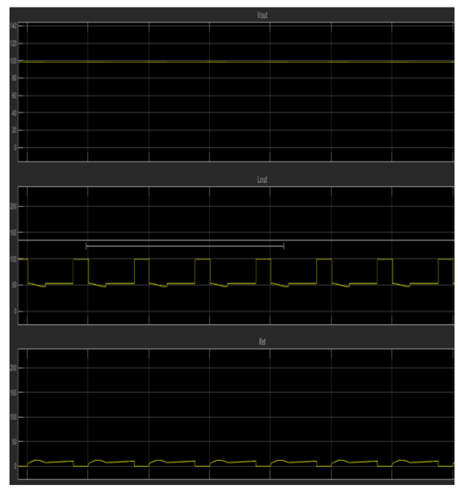

Fig.12.outpt voltage and inductance output and mosfet current

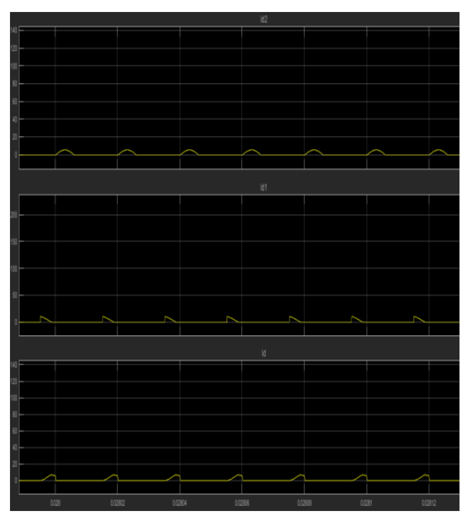

Fig.13.DIODE current

Themaximumswitchvoltageisequalto55Vforan output voltage equal to100V.

The detail of the turn-on commutation can be observed in Fig.13. The turn-on commutation occurs with zero current and the commutation loss is reduced.

The multiplier capacitor C_{M1} also operates as a clamping capacitor, eliminating the switch overvoltage due to lay-out problems.

Fig 14 presents the current in the resonant inductor. As presented in the theoretical analysis, this inductancereduces the di/dt in all diodes, minimizing the effects of the diodes reverse recoverycurrent.

Fig. 15 shows the current in the input inductance. The input characteristic is the same of the classical boost converter.

V. CONCLUSIONS

A simple non isolated topology of a high static gain step-upDc-Dc converter is presented in this paper. The mainoperation characteristics of the proposed structure are highstatic gain without the use of a transformer, low voltagestress, ZCS switch turn-on commutation and elimination ofthe reverse recovery current of all diodes. These operationcharacteristics allow to obtain high-efficiency and compactequipment.

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