Estimation of Crosstalk Noise With Mutually Coupled RLC Interconnects In VLSI Design

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Abstract- *Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The rapid advances in VLSI technology has resulted in the reduction of minimum feature size to sub-quarter microns and switching time in terms of Pico seconds or even less. As a result, the degradation of high-speed digital circuits due to crosstalk. Crosstalk is a phenomenon, by which a logic transmitted in VLSI circuit or a net/wire creates undesired effect on the neighboring circuit or nets/wires, due to capacitive coupling. Reduction of crosstalk noise in VLSI interconnect has become more important for high-speed digital circuits. In this project estimation of crosstalk noise analysis with mutually connected RLC interconnect in VLSI circuits is implemented with simulations results in CADENCE TOOLS. And also investigated the crosstalk reduction of mutually coupled RLC interconnects through shield insertion technique.*

Keywords- Crosstalk, FEXT, Interconnects, NEXT, Shielding, Signal Integrity, and VLSI.

I. INTRODUCTION

THE changes of scaling in VLSI technology result in the reduction of minimum feature size to sub-quarter microns and switching time in terms of Pico seconds level or even less. Because of this, the digital circuits today face a lot of problems like noise occurrence in the circuit due to smaller in the size and also smaller spaces between the lines. The advances in high-speed digital circuit design and Internet access for broadband signals require high-speed data signals [1]. In this constrain the design of interconnects is degrading the Signal Integrity to some very high levels to support quick varying and broadband signals. SI is defined in terms of as any deviation from ideal waveform at the receiver ends [2]. It becomes a problem for high performance of digital circuits when the effects of capacitance and an inductance also power, and ground bounce significantly degrade the performance and reliability of high-speed digital circuits[3]. Capacitive and inductively coupling effects are the major concern between two adjacent wires in DSM and UDSM technology because the spacing between two wires is too small[4].

This mutual coupled inductance and capacitance causes Near End Crosstalk (NEXT) at near to the transmitter end and Far End Crosstalk (FEXT) at the receiver end on the victim line when source applied to an aggressor line. The noise signature will be different on the far end and near end on victim line adjacent to an aggressor line. The FEXT noise is related to the difference between the inductively and capacitive coupled currents. The NEXT noise is related to the sum of the inductively and capacitive coupled currents. Coupling effect may be a short-range effect and which exists only between two adjacent signal lines[5]. Because of capacitive and inductively coupling sensitive with the coupling effects of the MOS drivers and therefore the conducting elements adjacent to the first originalsignal[6].

There are two techniques to scale back cross talk noise that to Coupling effects. Increasing spacing between two lines is one of the methods to reduce the crosstalk noise[7]. The crosstalk noise is inversely proportional to the distance between an aggressor and victim lines at the sense node. And another method is inserting a shield line(Shielding) between aggressor and victim line. The shielding technique can avoid the undesirable increase in coupling Effects[8].

The undesired capacitive or resistive or conductive couplings from one circuit or channel to the other are responsible for generating a typical noise called Crosstalk. Hence the crosstalk has become significant parameter in micro-circuits or in small chips that are designed to operate for communication.

In this paper estimation of crosstalk noise analysis with mutually connected RLC interconnects in VLSI circuits is implemented with simulations results in CANDENCE TOOLS.

VLSI design reduces the area of circuit also with less expensive and having less power dissipation line regulation factor of both analog and digital circuits,

Where Len is that the length of the coupled region between the first and second line, RT is Rise time, V is that the speed of the signal on the wire, C_{mL} is that the mutual capacitance, L_{mL} is coefficient of mutual inductance, C_L the capacitance per length of the signal trace and, L_L is that the inductance per length of the signal trace.Further, the paper is organized as follows, the Implementation of RLC model circuits in II. In Section III, the characterizing the interconnect model with shielding technique to attenuate of crosstalk noise on victim line are investigated. Finally, this paper is concluded in SectionIV.

II. ANALYSIS OF RLC CIRCUITS IN CADENCE TOOLS

Fig. 1. Coupled RLC aggressor and Victim line Interconnect model.

A step input is applied to the RLC coupled circuit shown in Fig. 1. and having the rise time of $T_r=1$ ns. During this circuit considered the consequences of coupling capacitance and mutually coupled inductance of aggressor and victim lines. The FEXT noise occurs at the receiver end and NEXT noise occurs at Transmitter endways the victim line that to aggressor line when switches the signal is ON.

In Fig. 2 shown, an input and an output response of the mutual inductance and coupling capacitance of the RLC
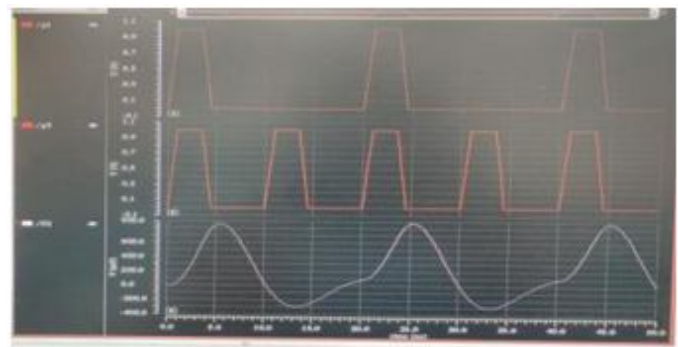

Fig 2.An input , output response showing the deviation in the output (due to crosstalk).

interconnect model circuit. The maximum over damped voltage on victim line at node FEXT is 0.159 mV and at node NEXT is 0.056 mV when applied 1V step input. These voltages are considered as FEXT and NEXT noise voltages on victimline.
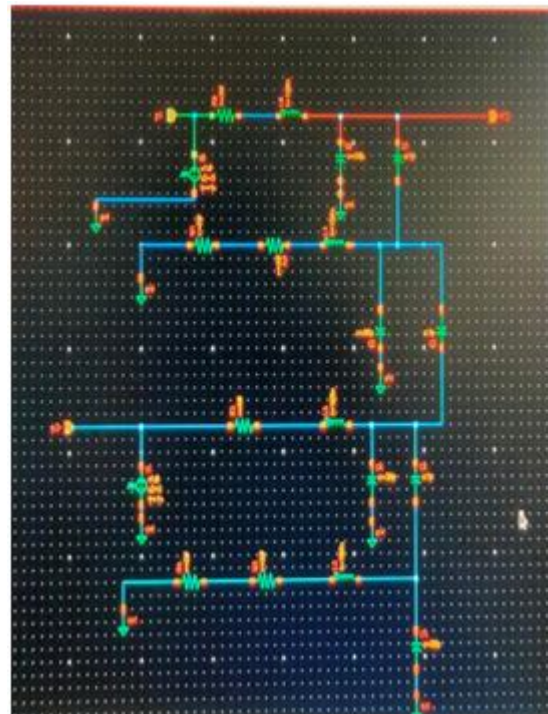

Fig. 3. Four lines of RLC interconnect model with alternative input signal

In Fig. 3. there is an alternate source of the signal is applied as an input and simulated the result for FEXT noise voltage on victim linesand NEXT noise voltage on victim lines respectively.
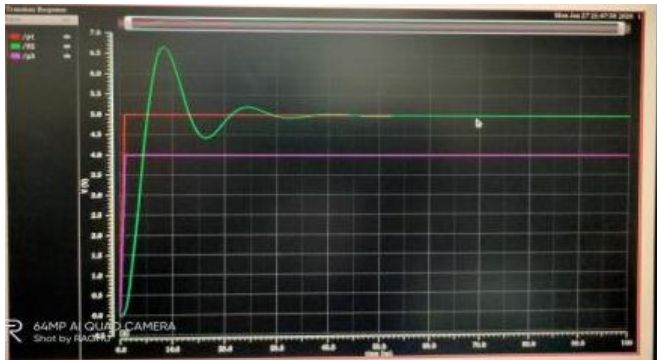
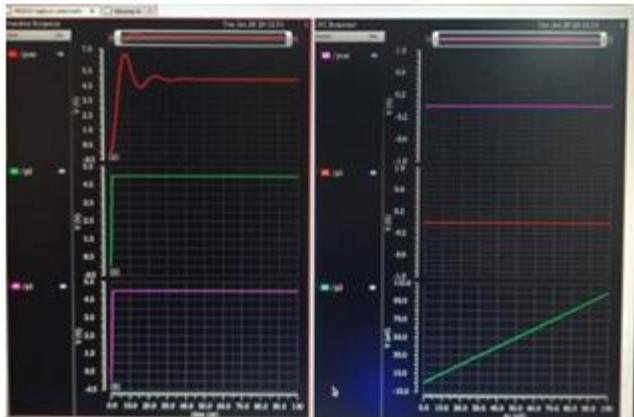Fig. 4(a). Input and output response at Vout1and Vout2

Fig. 4(b). FEXT and NEXT noise voltages on Victim lines

The maximum output response from Fig. 4(a). at node Vout1 and at node Vout2 is 1.252 V and 1.189 V respectively. The maximum over damped voltage on victim lines from Fig. 4(b). at FEXT1 is 0.205 mV, FEXT2 is 0.097mV and at NEXT1 is 0.221 mV, NEXT2 is 0.118 mV when 1V an input is applied alternatively. At FEXT1 and NEXT1, crosstalk voltage is higher compare to FEXT2 and NEXT2 because the victim line one is in-between the two aggressor lines and effects more compare to victim linetwo.

III. CROSSTALK REDUCTION BY USING SHIELDINGTECHNIQUE

In Fig. 5. shows the RLC model circuit with shielding technique. Guard (Shield) line inserted in-between the aggressor and victim line with grounded two sides of shield line. The simulation results show the FEXT and NEXT noise voltage on victim line at FEXT node and NEXT node. Here, a 1V input is applied at aggressor node same as RLC Coupled circuit(without shielding).
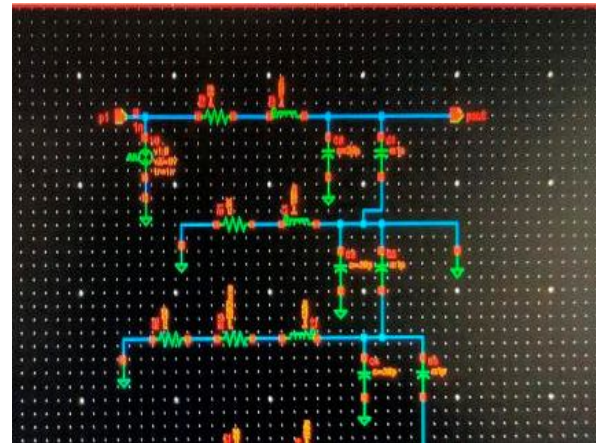

Fig. 5. RLC circuit model with shield insertion technique.

The simulation results are shown in Fig. 6. The out response at V_{out} is 1.326V and the maximum over damped voltages on victim node at FEXT is 0.022 mV and at NEXT is 0.014 mV. The crosstalk voltage is reduced with compare to without shielding RLC coupled model circuit.
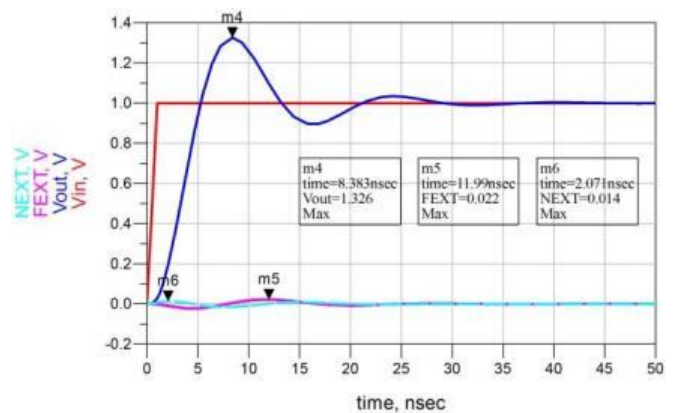

Fig. 6. The simulation result of an input, an output response, FEXT and NEXT of RLC Interconnect with shielding technique.

Shield line grounded with two sides is inserted in between the aggressor and victim line alternatively and shown in Fig. 7

Fig. 7. Four lines of RLC interconnect model with alternative an input.

In Fig. 8(a) and 8(b), the simulated results of FEXT noise voltage on victim lines at node FEXT21, node FEXT22 and NEXT noise voltage at node NEXT21, node NEXT22. The maximum over damped voltage of FEXT and NEXT noise on victim line at FEXT21, FEXT22, NEXT21, and NEXT22is0.112mV,0.016mV,0.188mVand0.007mV respectively.
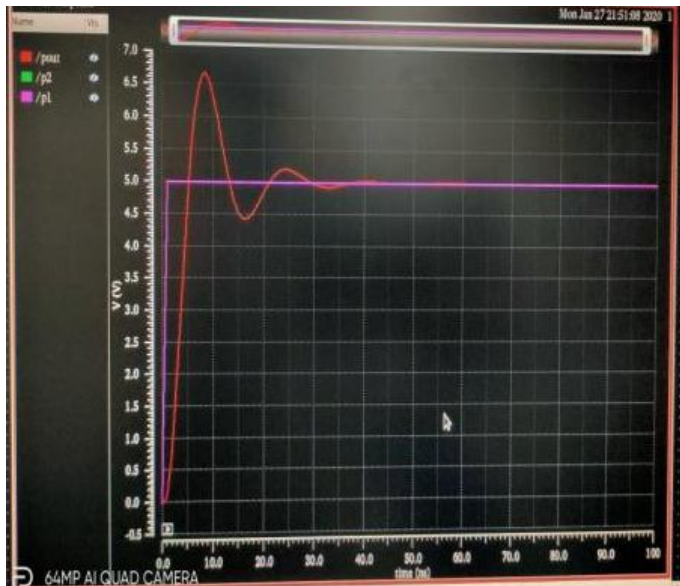

Fig. 8(a). Input and Output response of Four lines of RLC interconnect model with alternative input signal with shielding technique.

IV. CONCLUSION

In this paper, investigated the cross talk noise voltage for RLC model with and without shielding technique and performed the simulation of the model circuits. It's clear that the extent of crosstalk voltage decreases with the insertion of shield between the aggressor and victim line. The bottom connection during a shield line divides the interconnect structure into smaller interconnect structures thereby, further reducing the crosstalk voltage. The simulation results of RLC model circuit shown that the minimization of far end cross talk noise voltage. In future got to develop more accurate RLC interconnect model to research and make new shielding methodologies.

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