Design and Implementation of FMO/Manchester Encoding By Using SOLS Technique

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Abstract- *The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FMO/Manchester/Miller codes to reach Dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FMO, Manchester, Miller codes seriously limits the potential to design a fully reused VLSI architecture for both. In this project, the similarity oriented logic simplification (SOLS) techniques is proposed to overcome this limitation and also used to improve the hardware utilization rate. By using two code power, delay and area can be reduced. The proposed architecture will have less delay, area as compared to existing architecture. In this paper the architecture analyzed to reduced the num of components. Using SOLS technique to reduced the area, delay and power.*

Keywords- FMO, Manchester, Miller and SOLS technique.

I. INTRODUCTION

The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: Automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobile. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC).

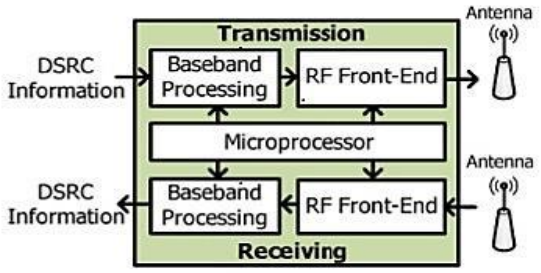

Fig 1. DSRC Transceiver.

The DSRC architecture having the transceiver. The transceiver having the baseband processing, RF front end and microprocessor. The microprocessor is used to transfer the instruction to the baseband processing and RF front end. The RF front end is used to transmit and receive the wireless signals using the antenna. The baseband processing is responsible for modulation, error correction, encoding and synchronization. The Similarity Oriented Logic Simplification having the two methods: Area Compact Retiming and Balance Logic Operation Sharing. The area compact retiming used to reduce the transistor counts and the balance logic operation sharing used to combine FMO and Manchester encoding.

II. FMO ENCODING

Flexible Macroblock Ordering or FMO is one of several error resilience tools defined in the Baseline profile of the H.264/MPEG - 4 AVC video compression standards. This way, FMO allows more flexibly deciding what slice macroblocks belong to, in order to spread out errors and keep errors in one part of the frame from compromising another part of the frame. Certain advanced encoding techniques can simulate some of FMO's benefits. In H.264/AVC, P (predicted) and B (bipredicted) frames may contain I (intra) blocks, which store independent picture. Rather than create a slice in order to periodically refresh entirely with I or IDR frames I-blocks can be sent in any desired pattern while predicted blocks make up the rest of the picture.

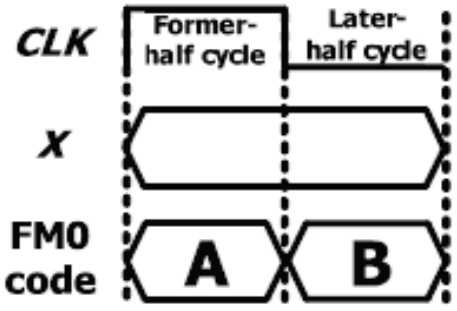

Fig 2. Code Word Structure of FMO

The coding principles of FMO is listed as the following three rules.

1) If X is the logic-0, the FMO code must exhibit a transition between A and *B*.
2) If X is the logic-1, no transition is allowed between A and B.
3) The transition is allocated among each FMO code no matter what the X.

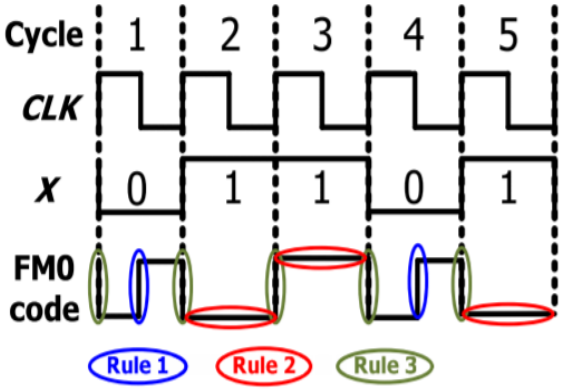

Fig 3. FMO Encoding

III. SOLS TECHNIQUE

The SOLS technique which is used to eliminates the coding diversity between Manchester and FMO encoding. The SOLS technique is eliminate the limitation on hardware utilization by two important techniques. Using compact retiming the number of transistor is reduced as 22. Using logic operation sharing, HUR was achieved as 100%. The maximum operation frequency of both Manchester and FMO encoding are 2GHz, 900MHz. The power consumption of Manchester and FMO encodings are 1.58mW, 1.14mW. The intention of SOLS scheme is to design a fully salvaged VLSI architecture for Manchester and FMO encodings. The SOLS technique is divided into two categories:

1) Area Compact Retiming.
2) Balance logic operation sharing.

IV. MILLER AND FMO ENCODING

An Miller encoding is also known as delay encoding. It can be used for higher operating frequency and it is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is 1. While using the Miller delay, noise interference can be reduced. The block diagram has a d flip flop, t flip flop, NOT gate, and XOR gate. Where the input is A_in and CLK, then the output is a Miller output. For example, if the input is 0 and the clock, given the XOR operation has done that, is A_in CLK, therefore 0 plus a positive edge clock produces the output as 0. Given to d flip flop, the clock has inverted, and after that output is given to t flip flop it inputs as d flip flop output, which is 0. Then the TFF is toggle FF, which produces the Miller output as 1.

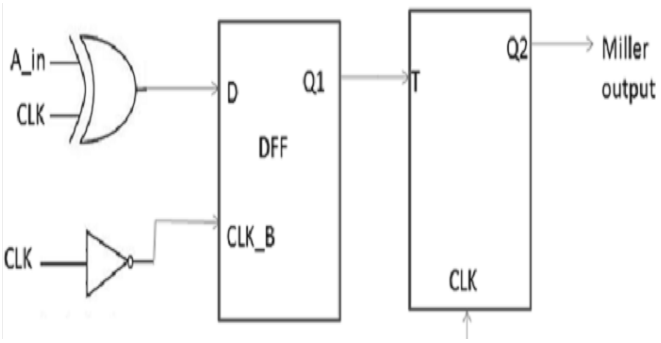

Fig 4. Block diagram for Miller encoder

The four states available are 00, 01, 10, 11. There is also RST. Transition is obtained based on 1 and 0. In the initial state, reset is 1. Then the next state will be 00, and after this reset it will always be 0. When the input is 0, and the current state is 00, the next state is 10. If the input is 1, and the current state is 00, the next state is 01. If the input is 0, and the current state is 01, the next state is 10. And if the input is 1, and the current state is 01, the next state is 01. If the input is 0, and the current state is 10, the next state will be 11. If the input is 1, and the current state 10, the next state is 00. If the input is 0, and the current state is 11, the next state will be 01. And if the input is 1, and the current state is 11, the next state is 10.

Table 1. State machine diagram for miller encoder

Reset	Input	Current State	Next State
1	-	-	00
0	0	00	10
0	1	00	01
0	0	01	10
0	1	01	01
0	0	10	11
0	1	10	00
0	0	11	01
0	1	11	10

In Area compact retiming for miller is same as a area compact retiming of FM0 encoder. To reduce the component in the logical circuit so the area is reduced.

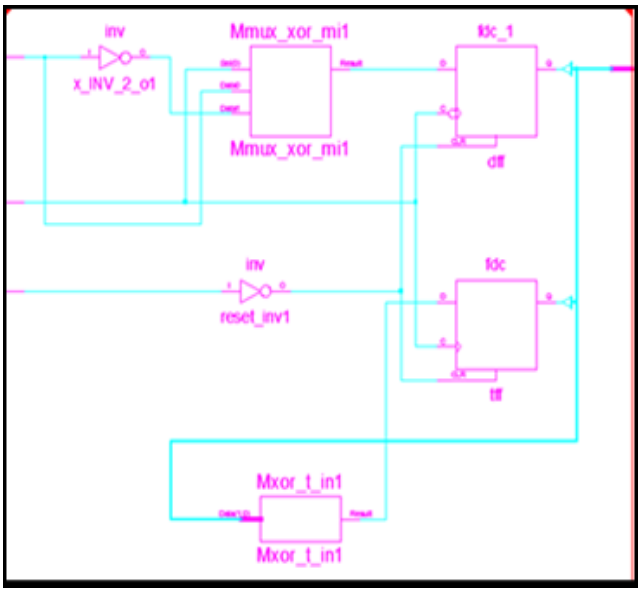

Fig 5. Illustration of area-compact retiming on Miller encoding architecture

To replace the Manchester encoder by miller encoder to the figure 8. And to rearrange and remove the some element based on the sharing the logic or component. After this operation to get the prepare balanced logic-operation sharing circuit.

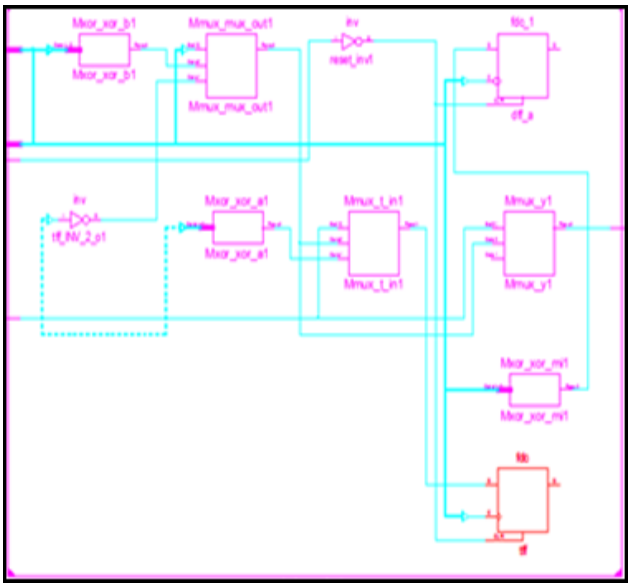

Fig 6. Architecture of FM0 and Miller encodings using SOLS technique

Table 2. Comparison Table

	FM0 Man	FM0 Miller	Area Compact	UBC	BC
LUT	3	4	1	2	2
Slice Reg	2	4	1	1	1
OC	3	3	1	2	2
IOB	5	5	4	6	6
Delay	2.498	1.535	1.943	1.914	1.914
Power	23	23	23	23	23

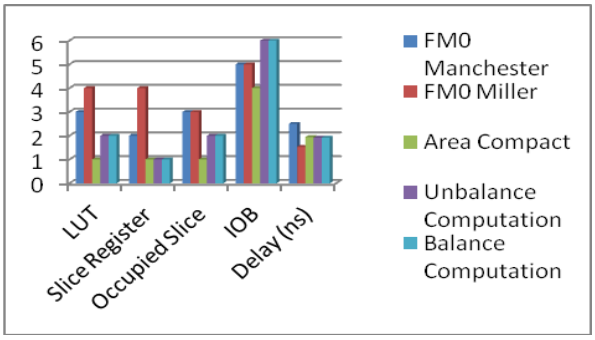

Chart 1. Simulation Result

V. SIMULATION

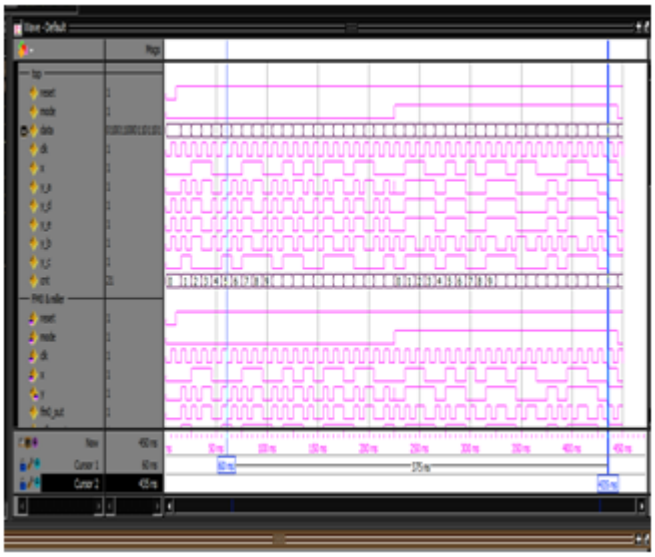

Fig 7. Simulation of Proposed Encoder

VI. CONCLUSION

In this paper, we have designed the architecture of a New Proposed Encoder which integrates the FMO, Manchester and Miller Encoding using SOLS techniques. In the first part we have integrated the FMO/Manchester encoding applied SOLS technique is proposed to overcome this limitation and also used to improve the hardware utilization rate. By using two code power, delay and area can be reduced. The proposed architecture will have less delay, area as compared to existing architecture. In this paper the

architecture analyzed to reduced the number of components. Using SOLS technique to reduced the area, delay and power.

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