Seven-Level Inverter Using Solar Power Generation

Ashwini S Khaire[1], Vrushali V Chitte[2], Pooja R Waghmare[3]
[1, 2, 3] Dept of Electrical Engineering
[1, 2, 3] Sandip Institute Of Engineering And Management, Nashik

Abstract- *This paper proposes another sunlight based force era framework, which is made out of a dc/dc power converter and another seven-level inverter. The dc/dc power converter coordinates a dc–dc support converter and a transformer to change over the yield voltage of the sun powered cell cluster into two autonomous voltage sources with various relationships. This new seven-level inverter is arranged utilizing a capacitor determination circuit and a full-connect power converter, associated in course. The capacitor choice circuit changes over the two yield voltage wellsprings of dc–dc force converter into a three-level dc voltage, and the full-connect power converter further changes over this three-level dc voltage into a seven-level air conditioning voltage. Along these lines, the proposed sun oriented force era framework produces a sinusoidal yield current that is in stage with the utility voltage and is nourished into the utility. The remarkable elements of the proposed seven-level inverter are that just six force electronic switches are utilized, and stand out force electronic switch is exchanged at high recurrence whenever. A model is produced and tried to check the execution of this proposed sun oriented force era framework.*

Keywords- Grid-connected, multilevel inverter, pulse-width modulated (PWM) inverter

I. INTRODUCTION

The extensive use of fossil fuels has resulted in the global problem of greenhouse emissions. Moreover, as the supplies of fossil fuels are depleted in the future, they will become increasingly expensive. In particular, small-capacity distributed power generation systems using solar energy may be widely used in residential applications in the near future. The power conversion interface is important to grid connected solar power generation systems because it converts the dc power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the dc power to ac power. Since the output voltage of a solar cell array is low, a dc–dc power converter is used in a small-capacity solar power generation system to boost the output voltage, so it can match the dc bus voltage of the inverter. The power conversion efficiency of the power conversion interface is important to insure that there is no waste of the energy generated by the solar cell array. The active devices and passive devices in the inverter produce a power loss. The power losses due to active devices include both conduction losses and switching losses Conduction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. A filter inductor is used to process the switching harmonics of an inverter, so the power loss is proportional to the amount of switching harmonics. The voltage change in each switching operation for a multilevel inverter is reduced in order to improve its power conversion efficiency and the switching stress of the active devices. The amount of switching harmonics is also attenuated, so the power loss caused by the filter inductor is also reduced. Therefore, multilevel inverter technology has been the subject of much research over the past few years. In theory, multilevel inverters should be designed with higher voltage levels in order to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI). Conventional multilevel inverter topologies include the diode clamped the flying-capacitor and the cascade H-bridge types. Diode-clamped and flying capacitor multilevel inverters use capacitors to develop several voltage levels. But it is difficult to regulate the voltage of these capacitors. Since it is difficult to create an asymmetric voltage technology in both the diode clamped and the flying capacitor topologies, the power circuit is complicated by the increase in the voltage levels that is necessary for a multilevel inverter. For a single-phase seven level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Asymmetric voltage technology is used in the cascade H bridge multilevel inverter to allow more levels of output voltage, so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a dc bus voltage of multiple relationships can be connected in cascade to produce a single phase seven-level inverter and eight power electronic switches are used. More recently, various novel topologies for seven level inverters have been proposed. For example, a single-phase seven-level grid-connected inverter has been developed for a photovoltaic system. This seven-level grid-connected inverter contains six power electronic switches. However, three dc capacitors are used to construct the three voltage levels, which results in that balancing the voltages of the capacitors is more complex. This paper proposes a new solar power generation system.The proposed solar power generation system is composed of a dc/dc power

converter and a seven-level inverter. The seven level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascade. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Since only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage, the switching power loss is reduced, and the power efficiency is improved. The inductance of the filter inductor is also reduced because there is a seven level output voltage. In this study, a prototype is developed and tested to verify the performance of the proposed solar power generation system.

II. CASCADED H-BRIDGES INVERTER

Cascaded H-Bridge configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units. Each H-bridge unit has its own dc source. Each SDC (separate D.C. source) is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Fig. 1 shows a single phase structure of a cascaded H-bridge inverter with separate D.C. sources. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, +Vdc, -Vdc and zero. To obtain +Vdc switches S1 and S4 are turned on. On turning on S2 and S3 together we get the output –Vdc. On turning the switches S1 and S2 together or S3 and S4 together or S1, S2, S3, S4 simultaneously we get the output 0. The AC outputs of different full-bridge converters are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. In this topology, the number of output-phase voltage levels is defined by M=2N+1, where 'M' is the no of levels and 'N' is the number of DC sources.

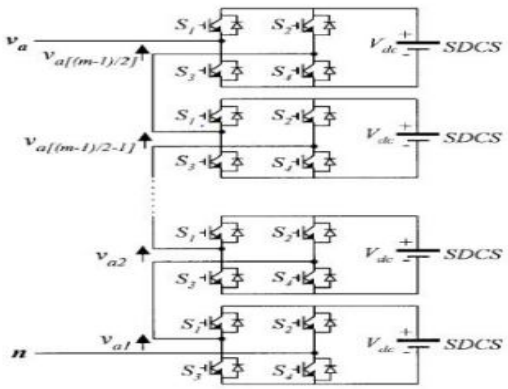

Fig.No 1 Single phase structure of a cascaded H-bridge inverter.

From the single phase structure of a cascaded H-bridge inverter as shown in Fig. 1 above, we can make the three level, five level, seven level inverters without using any type of modulation technique, and by using the same mathematical relation M=2n+1.

2.1 5- Level Diode Clamped Inverter

The topology proposed concept for the single phase is named as active-neutral-point-clamped five-level (ANPC5L) inverter. The most commonly used multilevel inverter among the three types is the diode-clamped multilevel inverter. In these inverters, the voltage across the semiconductor switches are limited by diodes connected to various DC levels as such it is called Diode Clamped Multilevel inverter. It provides a significant advantage that it can be extended to any number of levels by increasing the number of capacitors connected across the dc source. Each leg composed of four upper and four lower switches with anti-parallel diodes across them. Four series dc-link capacitors split the dc-bus voltage into 114, and clamping diodes will confine the voltage across the switches within the voltage of the capacitors. All diodes are rated for Vdc 14(Vdc/m-1 in general) and the 01" diodes need to block 3Vdc/4 and therefore there are six diodes need to be in series. However, for low voltage applications of multilevel inverter there is no need to connect the components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. The number of switches required for the five level diode clamped inverter is described in the table I. where m represents the number of levels of the inverter.

2.2 7-level Inverter

The topology of 7-level inverter is similar to 5-level topology, only the auxiliary circuit now was added with an additional circuit. In general, 7-level inverter consists of a full bridge inverter, two bidirectional switches (the auxiliary circuit), and three capacitors as voltage divider illustrated in Figure 1. To ensure that the power flows from the PV arrays to the grid, high dc bus voltages are necessary. Seven output voltage level can be achieved when the switching signal for the IGBTs in the topology were done properly. Diode-clamped and flying-capacitor multilevel inverters use capacitors to develop several voltage levels. But it is difficult to regulate the voltage of these capacitors. Since it is difficult to create an asymmetric voltage technology in both the diode clamped and the flying-capacitor topologies, the power circuit is complicated by the increase in the voltage levels that is necessary for a multilevel inverter.. Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage , so the cascade H-

bridge multilevel inverter to allow more levels of output voltage, so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a dc bus voltage of multiple relationships can be connected in cascade to produce a single-phase seven-level inverter. For example, a single-phase seven-level grid-connected inverter has been developed for a photovoltaic system. This seven-level grid-connected inverter contains six power electronic switches. However, three dc capacitors are used to construct the three voltage levels, which results in that balancing the voltages of the capacitors is more complex. Seven-level inverter topology, con-figured by level generation part and a polarity generation.

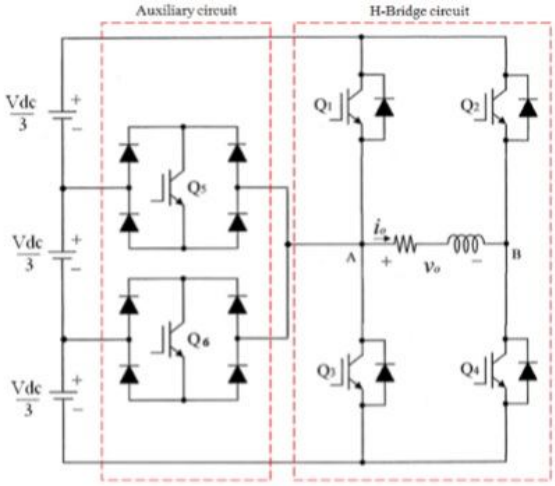

Fig.No 2 Topology of 7- Seven inverter

Table No 1 . The Switches On-Off Condition For 7-Level Multilevel Inverter.

Output Voltage	Q1	Q2	Q3	Q4	Q5	Q6
+Vdc	1	0	0	1	0	0
+2Vdc/3	0	0	0	1	1	0
+Vdc/3	0	0	0	1	0	1
0	0	0	1	1	0	0
0*	1	1	0	0	0	0
-Vdc/3	0	1	0	0	1	0
-2Vdc/3	0	1	0	0	0	1
-Vdc	0	1	1	0	0	0

Note: "1" for ON, "0" for OFF

2.3 Total Harmonic Distortion (THD)

THD is a measurement of the harmonic distortion is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. It can be presented by expression below

$$THD = \frac{\sqrt{I_2^2+I_3^2+I_4^2+\cdots+I_\infty^2}}{I_1} \quad (2)$$

Formula above is for the current waveform. THD is used to characterize the linearity of a systems and the power quality of electric power systems.According to IEEE standard of THD limits, total harmonic current distortion shall be less than 5% of the fundamental frequency current at rated inverter output. The THD for simulated model will be shown in Section IV.

2.4 PWM Modulation Technique for 7-level Multilevel Inverter

Seven level multilevel inverter's PWM modulation contain three reference signal named Vref1, Vref2, and Vref3. These three reference signals had same frequency, amplitude and phase. The difference is that they had different offset values. The reference signals are positive sine waveform. To produce the signals for the switches, the reference signals need to be compared to a carrier signal (Vcarrier); a triangular wave signal, using a comparator.

III. CIRCUIT CONFIGURATION

The proposed solar power generation system composed of a solar cell array, a dc–dc power converter, and a new seven level inverter. The solar cell array is connected to the dc–dc power converter, and the dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. The dc–dc power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven-level inverter. This new seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, connected in a cascade. The power electronic switches of capacitor selection circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in series. Because of the multiple relationships between then voltages of the dc capacitors, the capacitor selection circuit outputs a three-level dc voltage.The full-bridge power converter further converts this three-level dc voltage to a seven-level ac voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility, which produces a unity power factor. This new seven-level inverter contains only six power electronic switches, so the power circuit is simplified.

IV. DC-DC POWER CONVERTER

The DC/DC converter used in the system is the boost type with the configuration. The model composed of PV array is the power dc source, (P&O) MPPT adjusts the D in order to keep the DC/DC converter work at MPP and compute Vm. Vm is the controlled voltage source for the converter. The DC/DC boost converter works as a matching circuit between PV array & a load. The following parameters affect the performance of the converter: Voltage gain Av, Current gain Ai, input impedance Rin, boundary filter inductance Lb, and minimum filter capacitance Cmin. The boost converter stability is reduced due to its sensitivity to the variation of duty cycle in Av and Ai. In order to operate the converter at MPP a matching between the input impedance Rs of the PV array and the input impedance Rin of the converter must be satisfied. This is done by adjusting the duty cycle of the converter. The converter can operate in two distinct modes CCM where IL>0 which preferred for high efficiency and CCM where IL=0 during the switching period.

DC/DC Boost Converter Design

BoostRatio

$$A_v = \frac{V_o}{V_s} = \frac{V_o}{V_m} = \frac{1}{1-D} \quad (3)$$

Where Vo is the output Voltage from converter and D is the duty ratio

$$D = 1 - \frac{V_m}{V_o}$$

Inductor selection

$$L = \frac{V_m \times D}{\Delta I_L \times f_s} \quad (4)$$

ΔI_L is inductor current ripple.

The maximum power transfer when input impedance Rin of the converter matches the input impedance Rs of the PV module Equation (3) . The following system is designed by adjusting duty cycle D with respect to the load from the Equation (6),

$$R_{in} = \frac{V_s}{I_s} = R_{in} = R_s = \frac{V_m}{I_m} \quad (5)$$

$$A_i = \frac{I_o}{I_s} = \frac{I_o}{I_m} = (1-D) \quad (6)$$

Io is the output current of the converter, Vs voltage source, and Is is the current source. Rin of the boost converter.
From Equation (1) and (4),

$$R_{in} = \frac{V_m}{I_m} = \frac{V_o\,(1-D)^2}{I_o} = R_L\,(1-D)^2 \quad (7)$$

$$D = 1 - \sqrt[2]{\frac{R_{in}}{R_L}} \quad (8)$$

Output capacitor selection

$$C_{out} = \frac{I_o \times D}{f_s \times \Delta V_o} \quad (9)$$

ΔV_o is the output voltage ripple The average boundary value of the filter inductance and capacitance between CCM and DCM is

For CCM and $L > L_b$ and
$C_{out} > C_{min}$

$$L_b = \frac{(1-D)^2 \times D \times R_L}{2 \times f_s} \quad (10)$$

$$C_{min} = \frac{V_o \times D}{\Delta V_o \times R_L \times f_s} \quad (11)$$

f_s is the switching frequency, ΔV_o is the output voltage ripple, D Duty cycle, RL load resistance, Vo is the output voltage of the converter.

V. A NEW 7-LEVEL INVERTER

As seen in Fig. 3, the seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade. Operation of the seven-level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are

assumed to be ideal, while the voltages of both capacitors C1 and C2 in the capacitor selection circuit are constant and equal to Vdc/3 and 2Vdc/3, respectively.Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility voltage, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Fig.4.

5.1 Mode of Operation

Mode 1: The operation of mode 1 is shown in Fig. 3(a). Both SS1 and SS2 of the capacitor selection circuit are OFF, so C1 is through D1 and the output voltage of the capacitor selection circuit is Vdc/3. S1 and S4 of the full bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is Vdc/3.

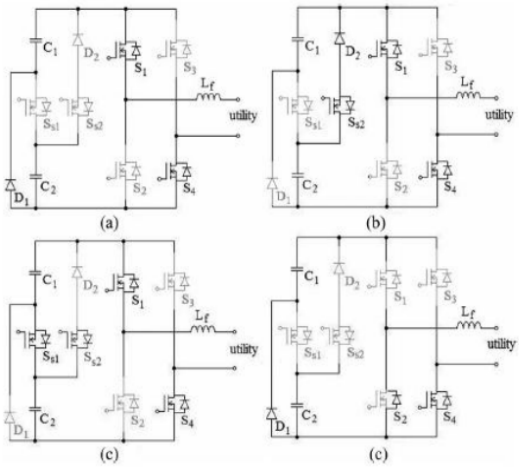

Fig No 3. Operation in the positive half cycle

mode 1 (b) mode 2 (c) mode 3 (d) mode 4

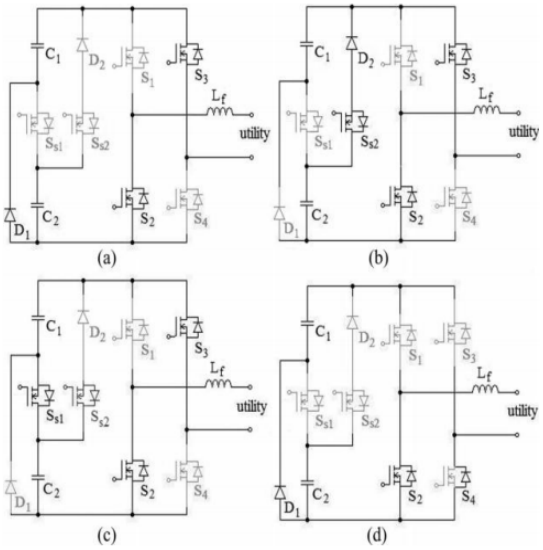

Fig No 4 .Operation in the negative half cycle

mode 1 (b) mode 2 (c) mode 3 (d) mode 4

Mode 2: The operation of mode 2 is shown in Fig. 4(b). In the capacitor selection circuit, SS1 is OFF and SS2 is ON, so C2 is discharged through SS2 and D2 and the output voltage of the capacitor selection circuit is 2Vdc/3. S1 and S4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is 2Vdc/3.

Mode 3: The operation of mode 3 is shown in Fig. 4(c). In the capacitor selection circuit, SS1 is ON. Since D2 has a reverse bias when SS1 is ON, the state of SS2 cannot affect the current flow. Therefore, SS2 may be ON or OFF, to avoiding switching of SS2. Both C1 and C2 are discharged in series and the output voltage of the capacitor selection circuit is Vdc. S1 and S4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is Vdc.

Mode 4: The operation of mode 4 is shown in Fig. 4(d). Both SS1 and SS2 of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is Vdc/3. Only S4 of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the anti parallel diode of S2 to be switched ON for continuous conduction of the filter inductor current. At this point, the output voltage of the seven level inverter is zero. Therefore, in the positive half cycle, the output voltage of the seven-level inverter has four levels: Vdc, 2Vdc/3, Vdc/3, and o (zero).The negative half cycle, the output current of the seven-level inverter is negative. The operation of the seven-level inverter can also be divided into four modes, as shown in Fig. 4. A comparison with Fig. 3 shows that the operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that S2 and S3 of the full-bridge

power converter are ON during modes 5, 6, and 7, and S2 is also ON during mode 8 of the negative half cycle. Accordingly, the output voltage of the capacitor selection circuit is inverted by the full-bridge power converter, so the output voltage of seven level inverter also has four levels: Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3, and −Vdc.

VI. SIMULATIONS AND RESULTS

For simulation purposes, To verify the performance of the proposed solar power generation system, a prototype was developed with a controller based on the DSP chip TMS320F28035. The power rating of the prototype is 500W, and the prototype was used for a single-phase utility. Simulation was done on MATLAB R2016a, the results was shown that the solar inverter has reduced harmonics.

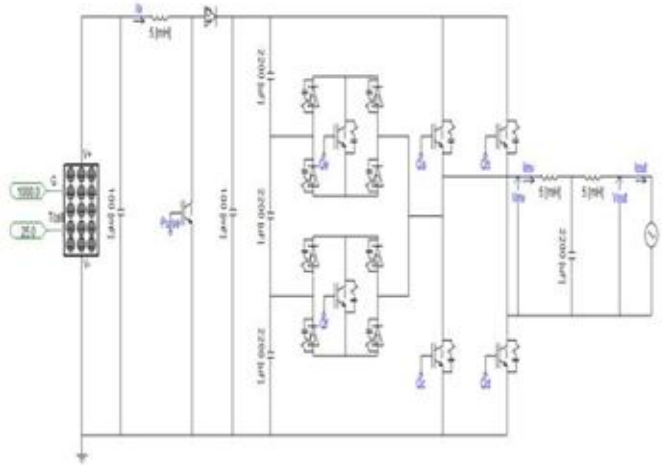

Fig.No 5 Model of 7-level multilevel inverter

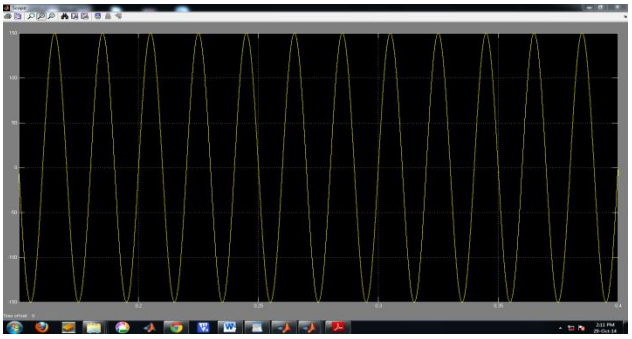

Fig.No 6 Input Voltage of a seven-level inverter

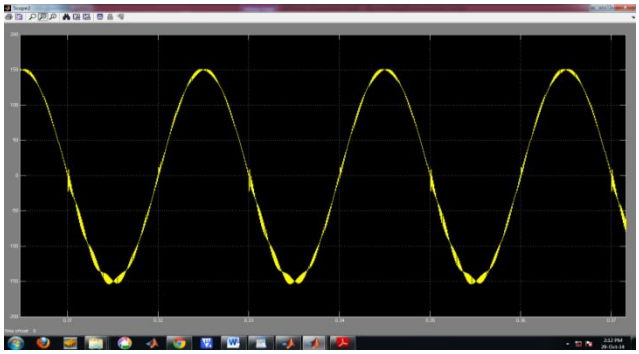

Fig.No 7 Input current of a seven-level inverter.

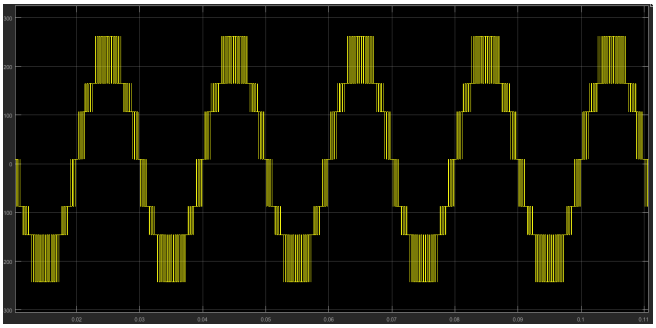

Fig.No 8 Output voltage of seven level inverter

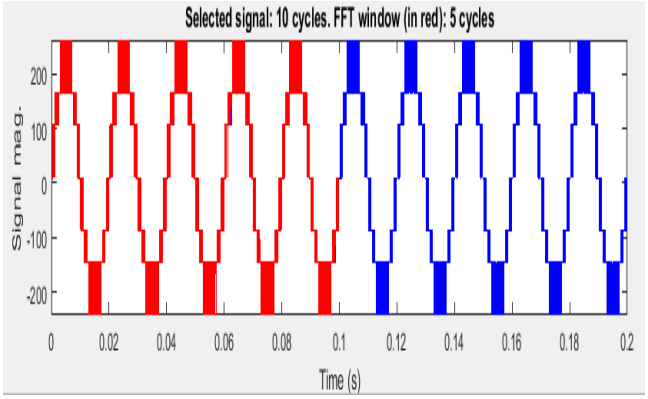

Fig. No 9 Selected Signal

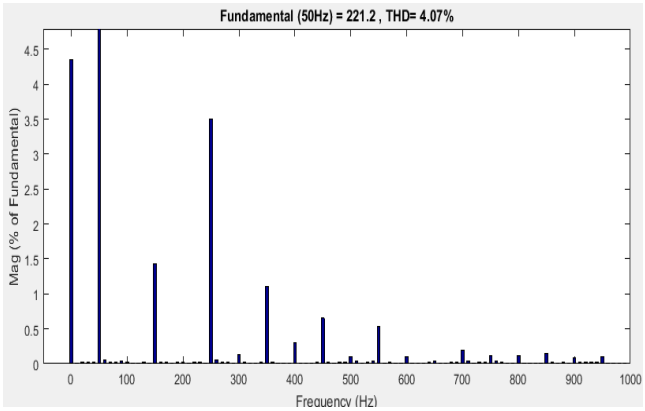

Fig.No 10 THD Waveforms

Figure 5. shows the 7-level inverter model. The output of the inverter is shown in figure 6,7 8 in which

sinusoidal current in phase with utility voltage and the THD of the 7-sevel level inverter also shown in figure 10.

VII. CONCLUSION

This paper proposes seven-level inverter control scheme have been verified analytically and demonstrated through simulation. Since the cost of conventional energy resources are increasing every year, this system is going to be economical in future. Besides the cost, the environmental benefits are likely to facilitate the widespread use and acceptance of this system. Thus the above proposed system is reliable and economical for remote applications. Solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Experimental results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell array.

REFERENCES

[1] Z. Zhao, M. Xu,Q. Chen, J. S. Jason Lai, and Y. H. Cho, “Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency pvinverter,”IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1304– 1313.

[2] K. Hasegawa and H. Akagi, “Low-modulation-index operation of a five level diode-clamped pwm inverter with a dc-voltage-balancing circuit for a motor drive,” IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3495–3505,Aug. 2012

[3] N. A. Rahim, K. Chaniago, and J. Selvaraj, “Single-phase seven-level grid-connected inverter for photovoltaic system,” IEEE Trans. Ind. Electr. vol. 58, no. 6, pp. 2435– 2443, Jun. 2011.

[4] Jinn-Chang Wu, Member, IEEE, and Chia-Wei Chou, “Solar Power Generation system with a Seven-Level Inverter,” IEEE Transactions on Power Electronics, vol. 29, no. 7, July 2014

[5] Arango, E.; Ramos-Paja, C.A.; Calvente, J.; Giral, R.; Serna, S. Asymmetrical interleaved DC/DC switching converters for photovoltaic and fuel cell applications—Part1: Circuit generation, analysis and design. Energies 2012, 5, 4590–4623.

[6] Walker, G.R.; Sernia, P.C. Cascaded DC–DC converter connection of photovoltaic modules. In Proceedings of the 33rd Annual Power Electronics Specialists Conference,Cairns, Queensland, Australia, 22–27 June 2002; pp. 24–29.

[7] Walker, G.R.; Sernia, P.C. Cascaded DC–DC converter connection of photovoltaic modules. In Proceedings of the 33rd Annual Power Electronics Specialists Conference,Cairns, Queensland, Australia, 22–27 June 2002; pp. 24–29.

[8] E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, ”Control Scheme of Three-Level NPC Inverter for Integration of Renewable Energy Resources Into AC Grid,“ Syst. J., Vol.6, No.2, pp.242-253, 2012.

[9] K. Hasegawa, H. Akagi, “Low-Modulation-Index Operation of a Five-Level Diode-Clamped PWM Inverter With a DC-Voltage-Balancing Circuit for a Motor Drive ,” IEEE Trans. Power Electron., Vol. 27, No. 8, pp.3495-3505.