A 30db Gain, Better S-Parameter Low Noise Amplifier Using 65nm Technology

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Abstract- *This paper show's the low noise amplifier having gain of 30 dB , S11 of -25 dB and S22 of -22 dB. The LNA designed is of two stage, both are body biased i.e. 0.3V is applied at the substrate of NMOS transistor. A inductor is also added in the first stage,between two transistor to improve the overall gain of the amplifier. The whole circuit consume 13 mW of power with 1V supply. The LNA designed for 3.4-3.6 GHz(5G) frequency range.*

Keywords- LNA, Gain, Body Biased, 5G, Substrate, Inductor.

I. INTRODUCTION

The Low noise amplifier (LNA) is a crucial building block of RF receiver. It is a big constructing block in view that its overall performance greatly influences each sensitivity and selectivity of the receiver. The contribution of LNA in RF receiver is to make bigger the signal and noise with out including any noise to its adget as a result SNR (Signal to Noise Ratio) isn't always degraded [1]. NF (Noise Figure) is an crucial issue of a receiver which defines standard SNR at the output to SNR on the input and it extensively relies upon the primary amplification component. LNA is the first amplification component of any receiver therefore plays a important role inside the RF receiver part as shown in Fig. 1. RF receiver has distinctive degrees specifically mixer, IF amplifier demodulator, LNA etc. however LNA need to have high benefit with low noise figure. Good linearity and stability also are desired properties of LNA for proper operation. For LNA designing, impedance matching is critical as it strongly influences the overall performance of a device [2].

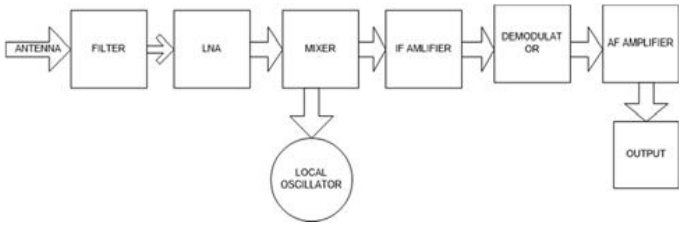

Fig.1 RF receiver

They have traits to provide good gain and low NF but fabrication and integration of these have been quite difficult. As the technology evolved, CMOS era came into existence. Inductive supply degeneration with cascade amplification LNA provides high overall performance in regards to noise discern and excessive advantage. This sort of LNA operates in a slender band of frequency.

At present, the popularity of 4G community is worldwide, and with the rapid boom of smart phones, the demand for bandwidth is retaining pace with the times, and the requirement for speed of wi-fi networks is also greater. As a result, a new generation of 5G (fifth technology wi-fi communication technology) [3] has been introduced. With the feature of a information transfer rate 10 times than 4G, low latency, 5G can meet the demand for future Mobile Health, Smart Home, and Internet of Vehicle; The release time for 5G uncovered by using Taiwan's NCC is ready 2020 [4] and the 5G spectrum might be announced by various nations gradually. The 5G trendy of superior nations in Europe, the US and Asia-Pacific can be the main references for Taiwan. Taiwan plan to launch 3.4-3.eight GHZ and 4.4-4.9 GHz, 28GHz, 700MHz and several other frequency bands. In this study, low noise amplifier (LNA) is designed to reap 3.4 - 3.8GHz band.

II. PROPOSED DESIGN

Fig.2 shows the proposed design. The design consist of two stage LNA in which first stage NMOS transistor's are bulk biased i.e. 0.3 V is connected in series with resistor of 20kΩ to substrate of transistor. This bulk bias concept is use to reduce the power consumption.

In first stage, the gate voltage of bottom transistor is supplied by current mirror which keep transistor in saturation region. The inductor is connected between the two transistor to increase the gain of overall LNA. Both stage are cascode architecture LNA. The input matching network consist of a capacitor in series with inductor and output matching network consist of inductor, capacitor and LC circuit. Matching network circuit is use to match the impedance. Input impedance is 50Ω.

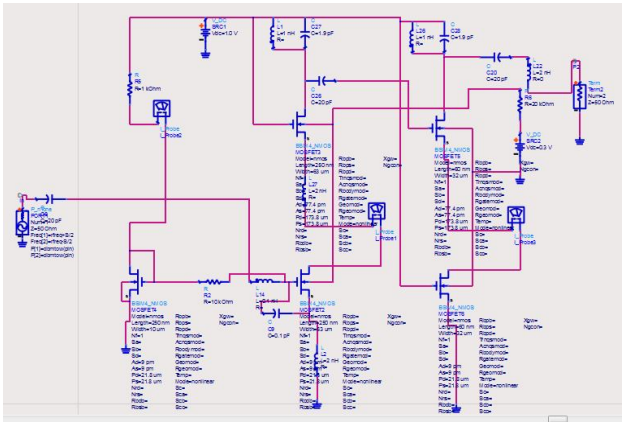

Fig. 2 Proposed design

The whole circuit designed on ADS software and using 65nm technology. Crcuit consume 13 mW of power from 1V supply.

III. SIMULATION RESULT

Important results to be observed for any LNA are gain, stability(K), S-parameters, noise figure, IIP3. All results obtained in dB except IIP3 and stability.

- Gain

Gain is denoted by S21. Fig.3 shows the circuit is having gain of 30 dB. S11 and S22 are -25 dB and -22 dB which indicate better values and makes this LNA good candidate for 5G application at 3.6 GHz.

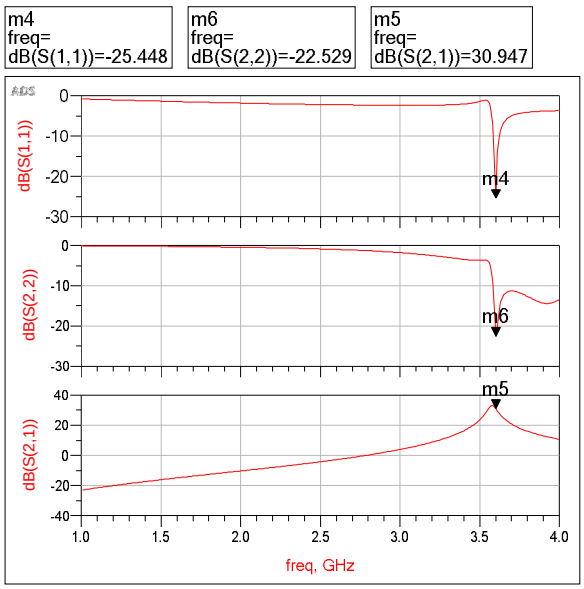

Fig. 3 S11,S21 and S22 graph

- Stability(K)

Stability is indicate by value of K. The value of K(fig.4) is 1.854 which is found to be greater than the minimum required value of K which is 1 .

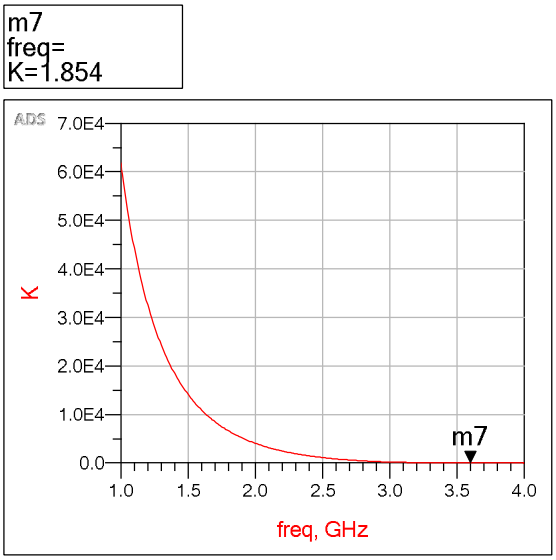

Fig. 4 Stability graph

- Noise Figure(NF)

Noise figure should be as low as possible. Fig.5 shows NF of 2.1 which indicate this circuit will remove noise from signal and provide to the further stage.

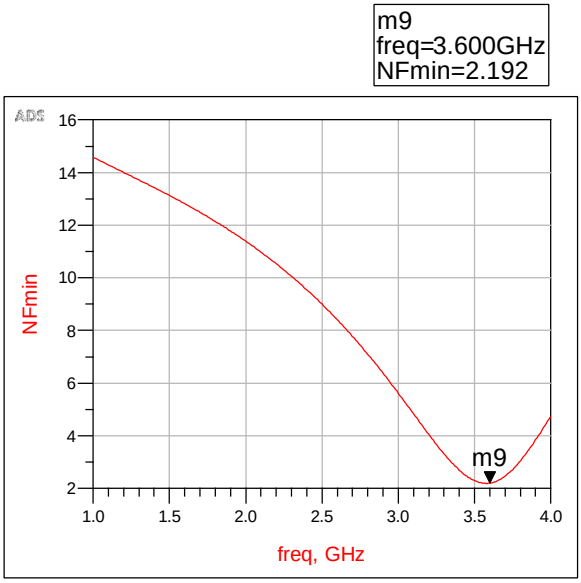

Fig. 5 Noise figure graph

Table 1 show the comparison between this design and others design.

TABLE I. COMPARISON TABLE

	Ref [5]	Ref [6]	**This work**
Frequency Range(GHz)	1.6-4.6	0.1-4.3	**3.4-3.8**
S11(dB)	-19	-8	**-25**
S21(dB)	28.1	21.2	**30**
IP3(dBm)	-9.2	-7.7	**-18**
Supply Voltage(V)	0.5 & 1.2	1.2	**1**
Power(mW)	8.9	2	**13**
NF(dB)	0.9	2.8	**2.1**
S22(dB)	-15	-	-22

IV. CONCLUSION

This paper shows that the inductor connected between two transistor in the first stage and bulk biased technique is improving the gain and S-parameters of the design. By this technique, gain of 30 dB, S11 of -25,S22 of -22 is achieved. The operating frequency is 3.6 GHz. The power consume is 13 mW. Since it id designed on 65nm technology, it will require less space on IC.

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