A Multilevel CHB STATCOM Using SVPWM Based Control For Wind Farm Applications

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Abstract- *Nowadays, electronic devices are very sensitive with harmonics. The needs for a free harmonic and high rating power source is increased to meet the requirement from the industries. This project is to eliminate THD using 7 level cascaded H-bridge of multilevel DC–AC inverter. The SVPWM for power electronic converters, provides high dynamic performance. This project proposes an SVPWM controller, which benefits high dynamic performance for the CHB STATCOM, despite the large set of inputs. The proposed FCS-MPC with SVPWM and park transformation performance is validated by applying to two configurations: 1) a 7-level CHB STATCOM with energy storage capability for a short-term active power smoothing and reactive power compensation of a 10 MW fixed speed wind farm at medium voltage, and 2) an experimental 7 level CHB STATCOM at low voltage. Experimental results are included to demonstrate effectiveness of the proposed inverter. This project is to reduce THD contributed by the level of inverter.*

Keywords- CHB STATCOM, Space vector pulse width modulation, Wind farm.

I. INTRODUCTION

The STATCOMs are an efficient alternative to the two-level ones, providing transformer less high voltage compensator, low harmonic currents, high quality voltage, and low Electro Magnetic Interference in the medium voltage level applications. One of the well-known and attractive multilevel STATCOM topologies is the Cascaded H-Bridge (CHB) STATCOM, due to an excellent modularity in the CHB configuration. CHB STATCOM, based on the series connection of H-bridges provides the required output voltage level. The CHB converter with equal dc link voltages, has many redundancies for the switching combinations to provide the same output voltage. The redundancies is used for dc links voltage balancing, reducing switching losses, and decreasing common mode voltage. Various classical linear control approaches and modulation techniques are proposed for the CHB STATCOM. Recently, Model Predictive Control (MPC) has received more attention in the power converters control. The advantages of MPC such as high dynamic performance, suitability for nonlinear and constrained systems, multi-objective capabilities, as well as, its simplicity and intuitiveness make it a powerful control strategy in power electronics. The MPC algorithms are classified into two groups of integer or continuous optimization problem .Continuous Control Set MPC (CCS-MPC) uses a modulator to synthesize the control action applicable to the power converter. The CCSMPC strategies, such as Generalized Predictive Control (GPC) and Explicit MPC (EMPC), present the MPC problem with complex formulations, but they have less computational cost. If the constraints are included in the GPC method, the optimization has to be computed by more computationally taxing numerical algorithms. The Finite Control Set MPC (FCS-MPC) uses the advantage of a limited number of switching combinations in a power converter to solve the optimization problem. A discrete converter model with integer control signals is used to predict the system behaviour for any permissible actuation sequence, up to the prediction horizon. The actuation sequence that minimizes a cost function is selected, and its first switching action is applied to the converter at the next sampling time. Main advantage of FCS-MPC relies on direct application of the control action to the converter, without requiring a modulation stage. The FCS-MPC is capable of improving converter parameters, such as switching losses and the common mode voltage. In the FSC-MPC, the optimization problem is solved online in a loop. Therefore, it is limited to lower prediction horizons due to online computational cost. In the FSC-MPC with control horizon one, the optimal control action should be applied at the same sampling time. However, due to online optimization delay, it is applied at the start of the next sampling time+1, affecting the converter performance.

II. BLOCK DIAGRAM OF PROPOSED

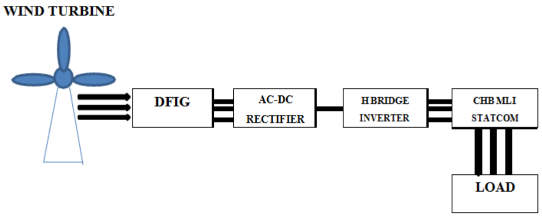

Fig 1: block diagram of proposed system

Voltage stability is a key issue to achieve the uninterrupted operation of wind farms equipped with doubly fed induction generators (DFIGs) during grid faults. A Static Synchronous Compensator (STATCOM) is applied to a power network which includes a DFIG driven by a wind turbine, for steady state voltage regulation and transient voltage stability support. The control schemes of the DFIG rotor-side converter, grid-side converter and the STATCOM are suitably designed and coordinated. The system utilizes dc bus voltage and generated voltage more effectively and generates less THD in the cascaded H- bridge multilevel inverter. Space vector pulse width modulation technique utilize a chaotic changing switching frequency to spread the harmonics continuously to a wide band area so that the peak harmonics can be reduced greatly. We apply a 7 level CHB STATCOM with energy storage capability for short term active power smoothing and reactive power compensation.

A new SVPWM technique is used for the control of pulse width modulation, it is used for the creation of AC waveform. The AC output voltage from the wind turbine is feed to the generator, where the generated voltage is converted into DC using the rectifier, the converted DC input is given capacitor storage unit and further it is converted into AC voltage and then transmitted to the transmission line. The CHB MLI STATCOM is connected to the Transmission line to compensate the power losess and voltages. The transformation techniques used in the SVPWM are park transformation. The Park's transformation, the time-varying differential equations are converted into time-invariant differential equations. The transformation converts the a–b–c variables to a new set of variables called the d–q–o variables. The conversions are made for the voltages for stable voltage and frequencies.

III. CIRCUIT DIAGRAM FOR PROPOSED SYSTEM

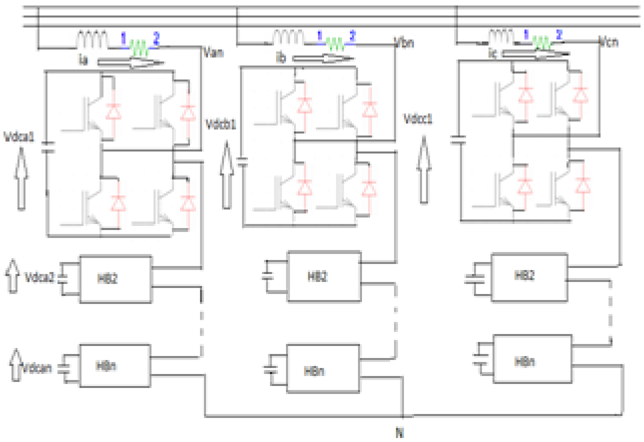

Fig 2: circuit diagram of multilevel cascaded H bridge inverter

They are Vs/2, Vs, 0,-Vs/2, and-Vs of cascading and H-bridge MLI. The applied for shunt active power filter to avoid harmonics drawn from a diode rectifier feeding RL load during unbalanced conditions.

PD modulation scheme has been proposed on series converters that may applied to parallel converters using interleaving techniques with multilevel characteristics. New MLI has been designed and implemented to improve performance by compensating some disadvantage like complex PWM and voltage balancing problem. In

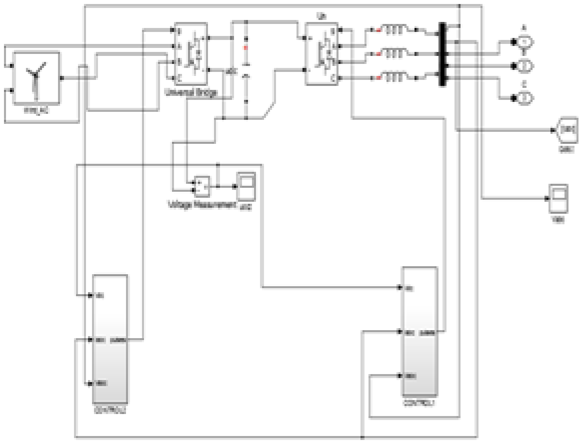

Fig 3 Wind modeling of CHB STATCOM

IV. PROPOSED TOPOLOGY AND OPERATING PRINCIPLE

The conventional H- Bridge inverter provides only three voltage levels, such as Vs, 0 –Vs only. The proposed switching technology for single phase H- bridge inverter provides fivevoltages. conventional inverters. A new approach has been proposed for Cascade H-bridge MLI to obtain low harmonic content at the output voltage.In order to improve the control performance a traditional digital control power converter with multi sampling techniques has been proposed, which can possess the advantage of reducing switching delay. The cascaded H bridge method is used to reduce the DC source and also avoid high switching frequency for high and medium stages of inverter. The CHB MLI solve the efficiency issues in interactions between stages.

V. SIMULATION OF MULTILEVEL CHB STATCOM

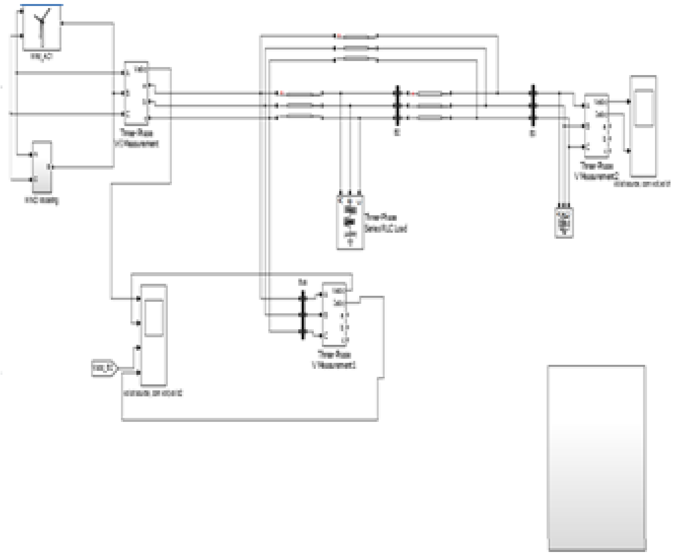

Fig 4 simulation model for CHB STATCOM

VI. SIMULATION RESULTS

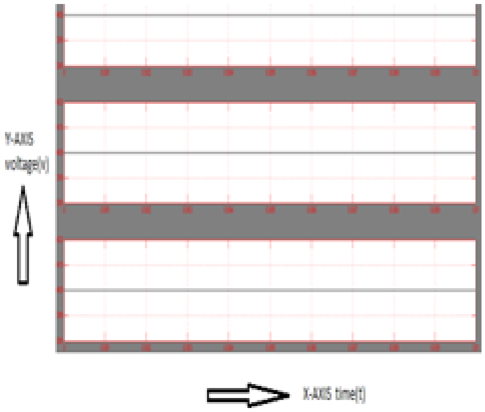

Fig 5 Input voltage waveform

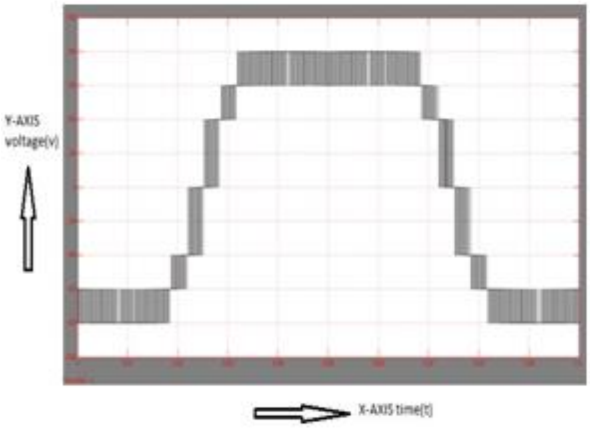

Fig 6 Single phase multilevel output of CHB

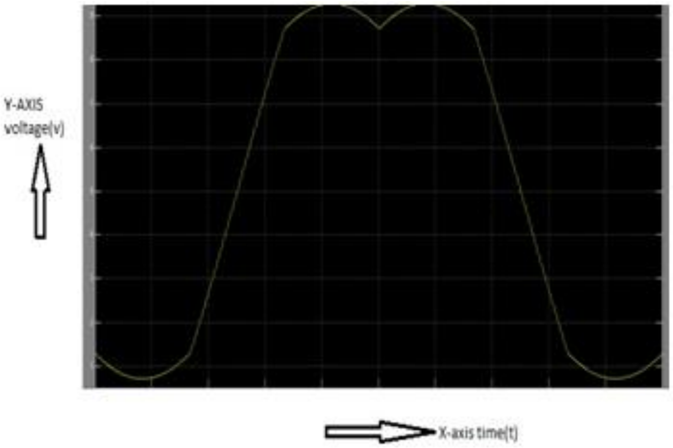

Fig 7 Space vector pulse width modulation output

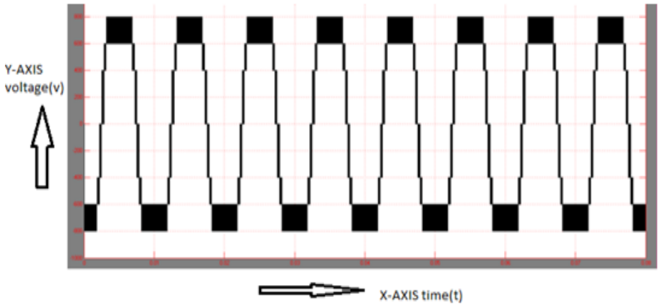

Fig8 Three phase multilevel output of CHB

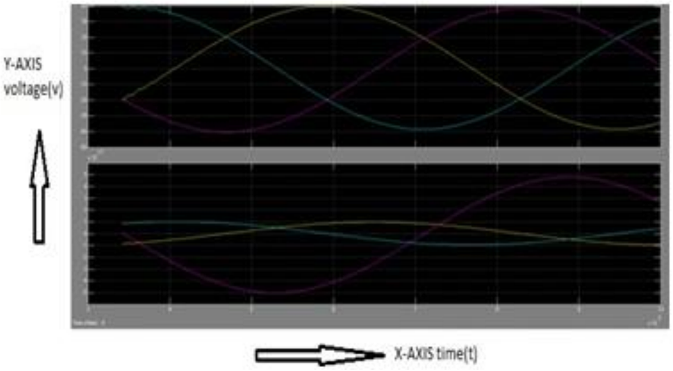

fig 9 non compensated output voltage

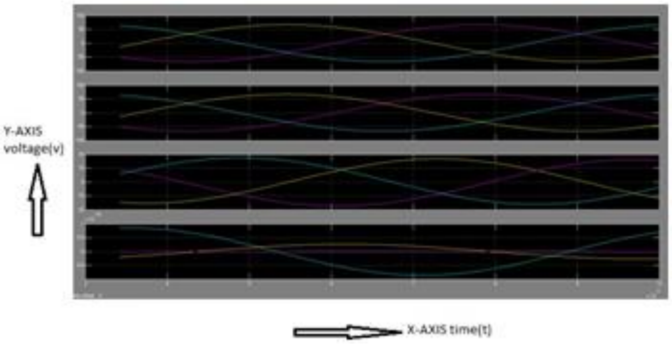

fig10 compensated output voltage

The simulation diagram of the proposed system in the shown figure 3. It consists of wind turbine model from where the three phase voltage is generated. The connected wind modeling consists of the doubly fed induction generator in which the input voltage generated is converted into DC voltage using rectifier and stored using the capacitor link. Further the voltage is converted using the inverter circuit. The voltage is measured using the V-I measurement and directed to the transmission line. The input voltage generated for the further compensation. The sub system part explains the generation of multilevel output. control parts associated with the modeling controls the signals that is to be transmitted. The converter ac voltage is given for the transmission line for the compensation.

VII. HARDWARE CIRCUIT

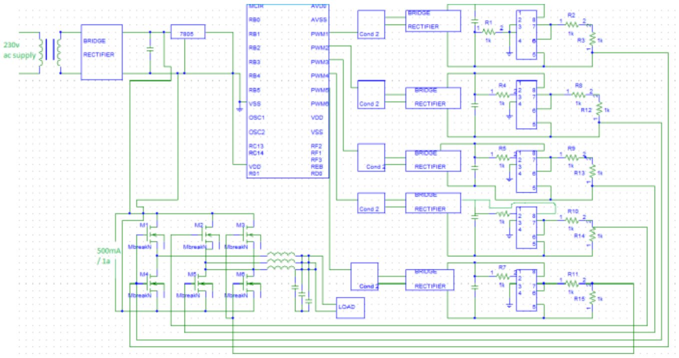

Fig 11 hardware circuit diagram

In figure 11 shows the hardware circuit diagram of the proposed system. The input will be 230/12V step down transformer along with a 500mA/1A .The input from the transformer is given to the controller to generate the PWM output signals. The bridge rectifier IN4007 is used for generating pulsating AC to DC signals. A LCD is placed across to represent the compensation and non compensation voltages .The voltage regulator used is IC7805 is to give a constant 5V to the controller. A crystal oscillator is used in the operating frequency of about 10 Mhz to 16 Mhz to generate signal clock pulse. The driver circuit TLP250 acts as amplifier, we give 12V from the tapping transformer, to amplify and given to the three phase inverter circuit, since we need to given a dc supply to the inverter circuit we use 1A transformer, the voltage from the transformer is given to bridge rectifier with the capacitor of value 220mf/160V that is filter capacitor. The three phase inverter has a MOSFET that is IRF840N. We use LC filters , for minimizing the harmonics. Finally it is connected to a resistive load (5W ceramic load) where the output voltages and waveforms can be obtained.

VIII. HARDWARE REQUIREMENTS

- MOSFET-IRF840N.
- CONTROLLER-DSPIC30F2010.
- DRIVER-TLP250.
- VOLTAGE REGULATOR-IC7805.
- BRIDGE RECTIFIER-IN4007.
- CAPACITOR-63µf/10V,220µf/160V,470µf/25V.
- INDUCTOR-2.8mH.
- RESISTIVE LOAD- 5W CERAMIC LOAD.
- CRYSTAL OSCILATOR-10MHz-16MHz.
- LCD DISPLAY- 16×2

IX. SOFTWARE REQUIREMENTS

MATLAB

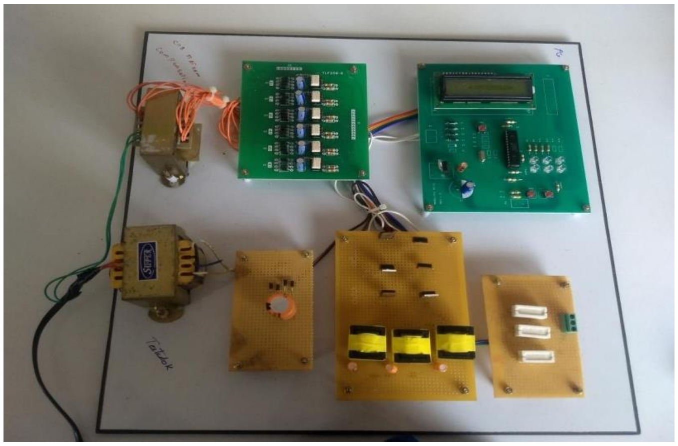

Fig 12 snapshot of hardware

X. OUTPUT WAVEFORM

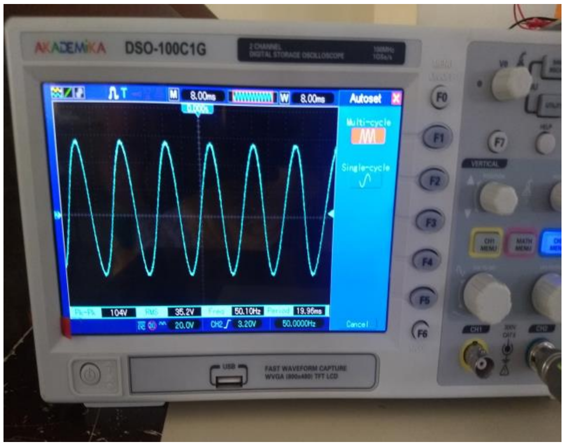

Fig 13 compensated output voltage

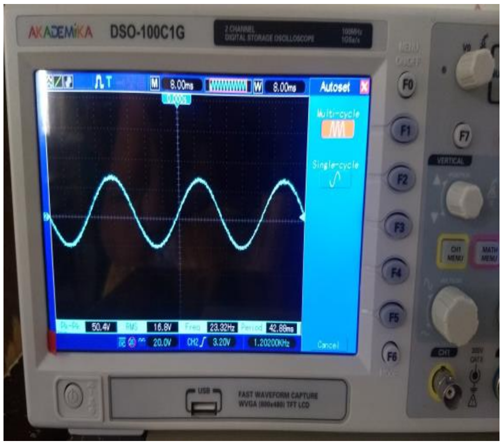

Fig 14 non compensated output voltage.

XI. CONCLUSION

Thus an CHB multilevel inverter of 7 levels using SVPWM technique is being implemented and the voltage compensation is obtained by reducing the harmonics. It provides less number of switching losses and reduction of harmonics using SVPWM technique and it is verified using the THD graph for existing and for the proposed system using simulation and the compensated voltage is obtained to be in the range of about 34-35V in the experimental prototype along with the waveforms. Although this research has covered most of the interesting issues and challenges of advanced STATCOM and several aspects of integration of ESS into STATCOM, there are certain aspects that might be interesting for future investigations which are given below: due to the excessive number of semiconductor devices and passive components , a fault protection scheme to enhance the ride through capability in various faults scenarios remains as an important challenge.Research on CMC based topology with ESS can be implemented for real and reactive power compensation in wind farms with DFIG .

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