Study on Application of Seven-Level Converter to Realize Fast Current Control In DC Micro-Grid With Extremely Low Impedance Interconnections

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Abstract- *DC micro grids have been emerging as next-generation small-scale electric power networks, where the line impedance is very low. This phenomenon causes large currents in the micro grids, even for a slight change in voltage; therefore, it is critical for a power flow controller to have faster transient response and precise power flow control. In this study, multi-level converters are applied as the power flow controllers to realize high-speed and high-precision power flow control in a DC micro grid. The output filter can be small, as a multi-level converter is used. This paper also presents the design of the output LC filter of a multi-level converter to satisfy a requirement of current ripple. We experimentally verified that a multi-level converter with a smaller filter can realize high-speed and high- precision power flow control for low line impedance conditions compared with the conventional 2-levelconverters.*

Keywords- Microgrids, DC-DC power converters, Power flow control

I. INTRODUCTION

VARIOUS studies, including the verification tests of DC micro grids, have been reported to enhance the reliability of the entire system [1-5]. A DC micro grid helps achieve efficient power transfer by reducing the number of power conversion stages between the AC and DC sides, because most grid-tied renewable energy systems deal with DC power on both input and output sides. Line impedances are usually very low in a DC micro grid owing to the shorter distances between the nodes such as the generators, batteries, and loads compared with a large-scale AC grid; thus, a large current flows through the lines even for a slight change in voltage. To suppress the excess current, a 2-level converter needs a bulky output filter. To overcome these limitations in a micro grid, a converter with high speed and precise power flow control is required. However, with a large LC filter, power flow cannot change rapidly, even for a sudden change in the reference of the power flow and load conditions.

In recent years, experimental investigations assuming the DC micro grid network have been extensively conducted. Examples of the grid network configuration connecting only two converters have been discussed in. Reference proposes an output impedance matrix model to describe the terminal frequency characteristics of a DC-DC converter around its switching frequency. In reference, a new configuration comprising the photovoltaic panels, a series DC electric spring, and a noncritical load is proposed to reduce the battery storage capacity of a DC micro grid that have substantial photovoltaic installations. proposes a control scheme of a bidirectional DC-DC converter for the energy storage systems to resolve the issue associated with change in its operation modes. A part of a grid configuration connecting only two converters and a passive resistive load has been investigated in. proposes an efficient power flow sharing and voltage regulation control method based on a hierarchical control to minimize the transmission loss of the DC micro-grids. An example of a network configuration by connecting three or more nodes has been presented in Reference presents these tabl is hment and operation control of the DC micro grid in corporating with an electric vehicle (EV) as a movable energy storage. The circuit topology used for the above studies in has been mainly the 2-level converter. Moreover, an improvement of the dynamic performance has not become their main objectives.

Meanwhile, there are studies aiming the realization of the high-speed response of the individual converter. In, a control method to realize the fast current response in a DC-DC converter was reported. This method assumes a low-voltage power supply with conversion from 5.5 V to 3.3 V and a switching frequency in MHz range to be integrated on a chip or in a package. Reference proposed a predictive current control for a bidirectional 2-level DC-DC converter to enhance the steady-state and dynamic performances of the DC micro grid.

In addition, there are studies dealing with the circuit topology of a 2-level bidirectional converter for the DC micro

grid . For the power converters on the DC micro grid, the conventional 2-level topology has usually been adopted; however, the 2-level topology has inherent limitations in achieving a higher switching frequency and a faster dynamic response.

In the present study, we apply a multi-level converter to realize higher speed and precise power flow control in a DC microgrid . An m-level converter can produce an output voltage with m-step seven without a filter. This clearly indicates that an m-level converter enables decrease of ripple content in a DC output voltage to 1/mth of that of the 2-level converter; thus, as the level (m) increases, the output filter can become smaller. It has been studied to apply multi-level converter to DC microgrid. However, there are no studies that DC network is constructed by using multiple multi-level converters.

In this study, the design procedure of the power flow controller for a DC small scale grid is investigated by dealing with the number of the levels as one of the design parameters. The contribution of this study is in the comprehensive design of the converters and LC filters for the DC microgrid based on the number of the levels. Moreover, experiments are conducted by constructing a DC network with multiple multi-level converters.

II. DESIGN OF POWER FLOW CONTROLLER AND FILTER

A. Assumed Circuit

A circuit for the investigation of power flow between two nodes as the minimum part of a DC microgrid is shown inFig.1.Intermsofpowerflow, a DC micro grid comprise three types of elements: a unidirectional power supply such as PV or wind, a bidirectional supply/load such as a battery bank, and unidirectional loads. These elements are connected one-to-one, one-to-plural, orplural-to-plural.InFig.1,$E1$,$R1$, $E2$, and $R2$ represent the power supplies and loads that are connected through a distribution line and a power flow controller. Fig. 2 shows the circuit configurations of the 2-level and multi-level topologies. In this study, flying-capacitor type multi-level topology is used as an example . The numbers of the circuit components in each converter are listed in TABLE I. A flying capacitor type *m*-level converter consists of ($2m$ – 2) switches and (m - 2) flying capacitors in the main circuit.

Although the number of the series connected switches increases in proportion to the number of the levels, the total conduction lossremainsalmostthesamewiththatofthe2-level converters. Because a switch with a lower voltage rating and lower on - state resistance can be applied in the multi-level converters due to the reduction of the voltage stress for each switch. From the viewpoint of the control, gate signals and the output switching frequency with the phase-shifted carrier modulation increase as the number of the levels increases. However, the number of the sensors does not increase in the control method of this study. In this way, there is a trade-off relationship between the reduction of the circuit components and improvement of the output control performance. Therefore, a comprehensive design procedure considering the number of the levels and output filter is necessary, and it is clarified in this study.

B. Theoretical design procedure for power flow controller considering the number of levels

The design of output filter of a power flow controller is performed with the objective to decrease both the current ripple (steady state) and the settling time (transient state) simultaneously; however, there is a trade-off relation between them depending on the filter parameters that can be improved in the case of a multi-level converter to match the lower output ripple of the 2-level converter. As the number of levels increases, the output LC filter becomes smaller and output response time decrease. Therefore, larger number of the levels provides improving the system dynamic behavior. However, the flying capacitor type *m*-level converter consists of a lot of the components such as ($2m$ – 2) switches and (m – 2) flying capacitorscomparedwiththe2-levelconverters.Thereistrade- off relationship between the number of the levels and improvement of the system dynamic behavior. Therefore, it is necessary to design in consideration of the number of the levels *m*. Fig.3 shows typical waveforms to demonstrate the trade-off between the ripple current and settling time in the 2-level and

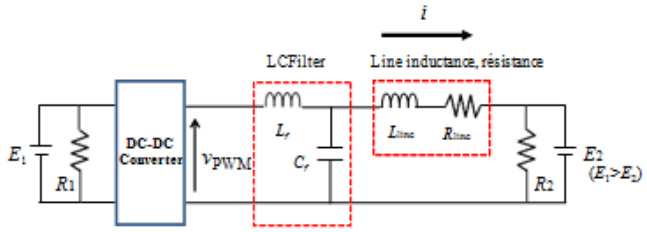
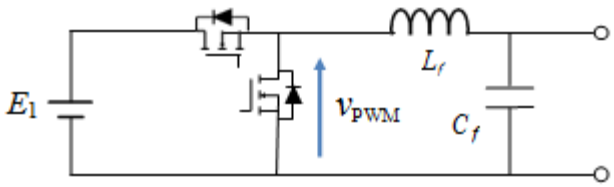


Fig. 1. Circuit for power flow control between two nodes.



(a) 2-leveltopology.

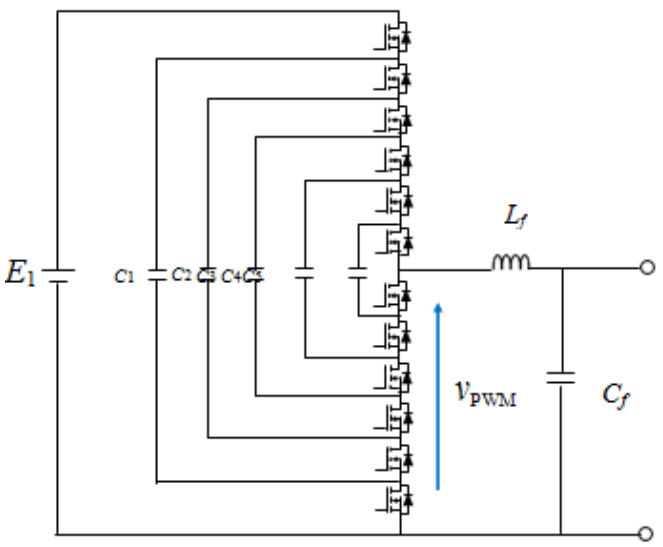


Fig. 2. Circuit configurations of power flow controllers.

TABLE I
THE NUMBER OF ELEMENTS IN CONVERTERS

The number of levels	2-level	7-level	*m*-level
Switching device	2	12	2*m*-2
Flying Capacitor	-	5	*m*-2
Output PWM switching frequency f_{PWM}	f_c	6 f_c	(*m*-1) f_c

multi-level converters. For the same ripple, the settling time is longer for the 2-level converter (larger filter) than that of the multi-level converter (smaller filter) as shown in Fig. 3(a). On the other hand, for the same filter, the ripple is larger for the 2-level converter than that of the multi-level converter as shown in Fig. 3(b). The 2-level converter has an inherent constraint in design with regard to improving both the ripple and the settling time for the same switching frequency, e.g. that of a multi-level converter. In the design, the gradient of the current rise in a step response is analyzed instead of the settling time considering that the gradient is proportional to the settling time when the current response is optimized for critical damping.Fig.4 shows the equivalent circuits for the analysis of the gradient and steady- state ripple of the output current considering the worst-case operation of the converter. Using theoretical investing ations, the maximum gradient of the current change is determined by(1).

For the sake of simplicity, R1 and R2 can be ignored.

$$\max\frac{di}{dt} = \frac{E_1 - E_2}{L_{line}L_fC_f(\alpha-\beta)(\alpha-\gamma)} \quad (1)$$

Here, α, β, and γ are the solutions of s in the following equation (2), where β and γ are the conjugate values.

$$s^3 + \frac{R_{line}}{L_{line}}s^2 + \left(\frac{1}{L_{line}C_f} + \frac{1}{L_fC_f}\right)s + \frac{1}{L_{line}L_fC_f} = 0 \quad (2)$$

The AC current *i*s in the steady state can be determined by the equation (3) -(5). *Vn* is the *n*-th order harmonics of *v*PWM. *Vn* is changed according to the number of levels (*m*). *v*PWM is the voltage, as shown in Fig. 2. *f*n is the frequency of the *V*n.

$$Z_n = R_{line}(1 - 4\pi^2 f_n^2 L_fC_f) + j2\pi f_n(L_{line} + L_f - 4\pi^2 f_n^2 L_{line}L_fC_f) \quad (3)$$

$$\varphi = \tan^{-1}\frac{2\pi f_n(L_{line} + L_f - 4\pi^2 f_n^2 L_{line}L_fC_f)}{R_{line}(1 - 4\pi^2 f_n^2 L_fC_f)} \quad (4)$$

$$i_s = \sum_{n=1}^{\infty}\frac{V_n}{|Z_n|}\sin(2\pi f_n t + \varphi_n) \quad (5)$$

The current ripple *i*ripple in the steady state can be calculated by taking the difference between the maximum and minimum values of *i*s. Since *i*s is periodic, the approximate maximum and minimum values can be obtained by calculation. The *L*f and *C*f are determined to satisfy the requirement of the current ripple for an application.

The *L*f and *C*f of the filter and the output level (*m*) can be designed by numerical calculations using the equations(1)-(5). In this way, the design procedure for the power flow controller and the filter is explained theoretically.

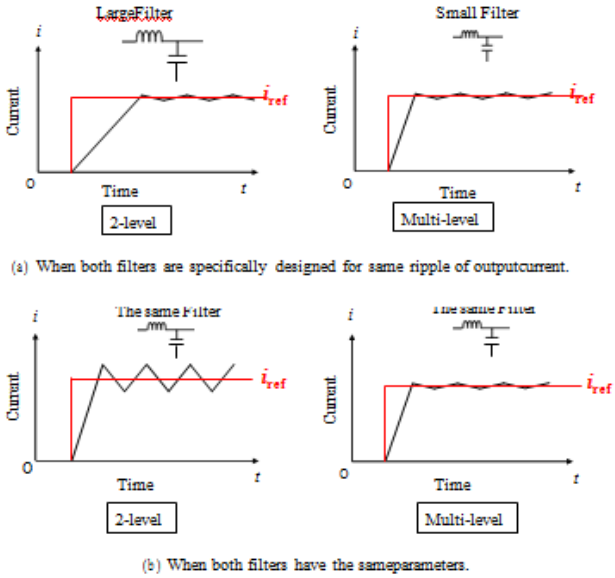


Fig. 3. Example of current waveforms in step response depending on the number of output levels and output filter of converters.

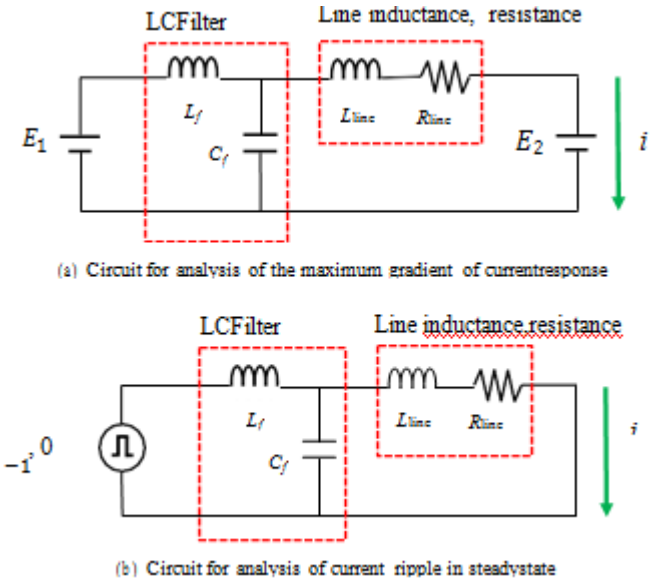


Fig. 4. Equivalent circuits for filter design of power flow controller considering the worst-case operation.

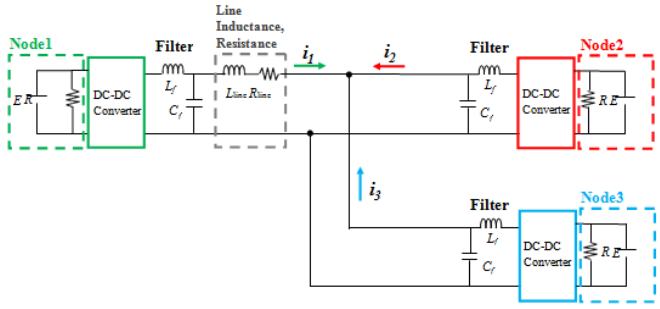


Fig. 5. Circuit configuration of distribution network with three nodes and three converters for validation of power flow control.

III. INVESTIGATION OF CONTROL PERFORMANCE OF 2-LEVEL AND 7-LEVEL POWER FLOW CONTROLLERS

A. Investigation condition of assumed circuit

The current control capability of the 2-level and multi-level converters are validated using a simulation. In this investigation, a distribution network comprising three nodes and three Converters is considered as a part of the assumed DC micro grid, as shown in Fig.5. In this circuit, three bid I rectional power supplies are assumed the batteries. They are connected to one another through the respective power flow controllers and distribution line, whose stray inductance and resistance values depend on its length. Two types of the distribution network are constructed, one with three 2-level converters and the other with three 7-level converters.

B. Practical calculation of filter design for 2-level and multi-level power flow controllers

The parameters of the circuits shown in Fig. 5 are listed in TABLE II. The output filters of the 2-level and 7-level power flow controllers are designed using (1) -(5) for a current ripple of 0.01 A. For fixed filter, the ripple needs to satisfy the requirements regardless of the length of the distribution line. As the length is shorter, the design of the filter becomes stringent. In this design, the length is assumed to be a minimum of 1 m. Considering that the same output PWM frequency is used for both converters , the carrier frequency of the7-levelconverter using a six-carrier phase-shifted modulation is set as 83.3 kHz. As a result, the filters of the 2-level and 7-level converters are designed as shown in TABLE III. In this design example, filter capacitors of the same value are used for ease of comparison of. From TABLE III, it can be confirmed that the filter parameter of the 7-level converter decreases by approximately one-sixth of that of the 2-level converter. This decrease is attributed to the output voltage ripple of the 7-level converter that becomes one-sixth of that of the 2-level converter according to the principle of operation.

C. Simulation validation in three-nodes distribution network

In this simulation, using the circuit simulator PSIM, the control performance of each output current is evaluated in the Step response, considering the transient changes in the power flow. The reference output current of each converter is shown in Fig. 6. Firstly, all the currents are initially set to zero, which means that the output voltages of all the three converters are controlled to the same value. Secondly, a current of 2.0 A from Node1 to Node2 is achieved by changing the output voltage of the converters, there by fixing current *i*3 at zero. Thirdly, a current of 2.0 A flows from Node1 to Node3, thereby fixing current*i*2at2.0A.Asaresult, a current of 4.0 A from Node 1 is distributed equally (2.0A) to Node 2 and Node 3. The current- control scheme adopted in each converter is based on PI controller using the feedback information of each inductor current.

Figs.7 and 8show the simulation results for the2 – level and 7-level converters, respectively. It is observed that the settling time in the case of the 7-level converter becomes approximately one fifth that of the 2-level converter, which is due to the lower time constant of the filter of the 7-level converter. In addition, it is observed that the response values of *i*2 and *i*3 do not follow the reference values at there spective in stants of the step change (0.0028 and 0.0020 s); this is due to the limitation of the response bandwidth of the converter. It is observed that their peak values are 0.25 A in

the 2-level and 0.5 A in the 7-level converter, respectively. While the settling time in the 7-level converter improves five times, the peak value of the discordance (ripple) only doubles. This faster power flow capability of the multi-level converter is expected to provide higher stability and reliability of the DC micro grid.

Since the outputs witching frequencies are equalized between the 2-level and the 7-level converters, the total number of switching in each circuit is the same. However, for this condition, the switching loss of the 2-level converter is larger thanthatofthe7-level converter;Therefore, from the efficiency viewpoint, considering the same carrier frequency for both converters would be a practical approach for a fair comparison. Accordingly, the switching frequency of the 2-level converter was changed from 500 kHz to 83.3 kHz, and the inductance of the filter was redesigned to 60 mH. Fig. 9 shows simulation result for the power flow using three 2-level converters (*F*pwm =83.3 kHz).

TABLE II
INVESTIGATION CONDITIONS

The number of levels	m	2-level	7-level
Node voltage	E	200 V	
Line resistance	R_{line}	0.0022 Ω	
Line inductance	L_{line}	0.3 μH	
Load resistance	R	200 Ω	
Capacitance of flying capacitors		—	19.8 μF
PWM switching frequency	f_{PWM}	500 kHz	83.3 kHz * 6 = 500 kHz

TABLE III
DESIGNED FILTERS IN THE CONDITION IN TABLE II

The number of levels	m	2-level	7-level
Filter capacitance	C_f	18 nF	
Filter inductance	L_f	10 mH	1.8 mH

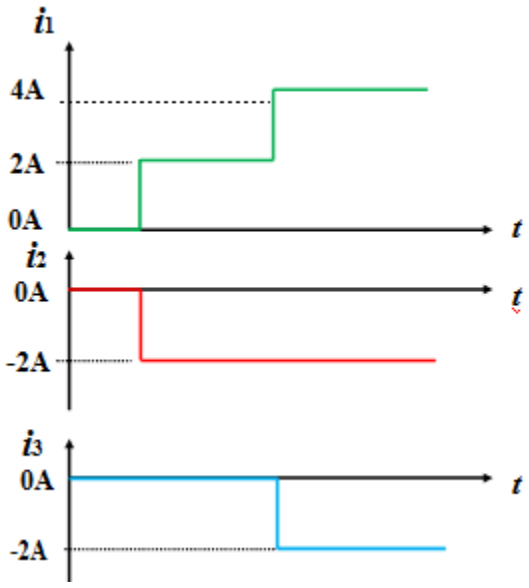


Fig. 6. Current references in this investigation.

IV. EXPERIMENTALVERIFICATION

A. Experimental setup andcondition

Prototypes of the 2-level and 7-level converters with the filters were designed and constructed for validation of the system with three nodes and three converters as shown in Fig. 5. Fig. 10 shows the experimental setup using three 7-level powerflowcontrollers.The experimental condition is the same as the simulation condition shown in TABLEs II and III. The DC power supply, power flow controller,output filter, andload resistor are used for each distribution node. A cable with a cross-sectionareaof8mm^{2}andalengthof100m(R_{line}=0.22 Ω and L_{line}=30 μH) is used for interconnecting the nodes. A feedback control system is configured using a DSP and FPGA digital controller (PE-Expert4, manufactured by Myway Plus Corporation), and the current sensors (LAX 100-NP, manufactured by LEM).

B. Efficiency measurement ofconverters

The efficiency of each prototype converter is measured for a typical output power of 500W. Fig.11 shows the circuit for the efficiency measurement. The parameters applied to the investigation circuit of Fig. 10 are listed in TABLE IV. The reference of the duty ratio is set as 0.5. The values of the load resistance are changed, as it consumes 500 W. Efficiency was measured using a power analyzer PW6001 manufactured by Hioki Corporation as shown in TABLE V. The loss of the 7- levelconverterwassmallerby25.8-18.3=7.5W,andthefilter loss was also smaller by 10.6 - 4.4 = 6.2 W compared with the 2-level converter with *f*PWM = 500 kHz. In the comparison between the 7-level converter and the

2-level converter with *f*PWM = 83.3 kHz, the loss of the 7-level converter was largerby 18.3 - 10.8 = 7.5 W, and the loss due to the filter was smaller by 15.4 - 4.4 = 11 W. Thus, the total efficiencies of the 7-level and 2-level converter with *f*PWM = 83.3 kHz were measured as almost the same value. As the result of this measurement, the loss reduction in the output filter is observed in the 7-level case. It is one of the attractive features for the multi-level converters.

C. Comparison of current control performance under the same switching frequency in 2-level and 7-levelconverters

Figs. 12 and 13 show the experimental results of the power flow control using three 2-level and three 7-level power flow controllers at a common *F*pwm of 500kHz. It is observed that all the wave forms are in good agreement with the simulation results in Figs. 7 and 8. It is experimentally verified that the 7- level converter can realize faster current controlcompared with the 2-level converter. The settling time of the current response in the 2-level converter is observed as 250 μs as shown inFig. 12 and that in the 7-level converteris 50μs as shown inFig.13; therefore, it is evident that the settling time of the current response is improved by a factor of 5 by using 7-level converter.

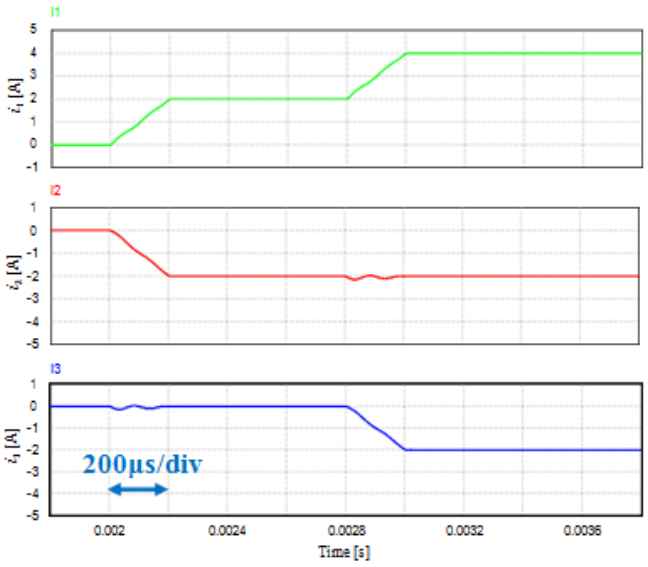


Fig. 7. Simulation result of power flow using three 2-level converters (*f*PWM=500 kHz)

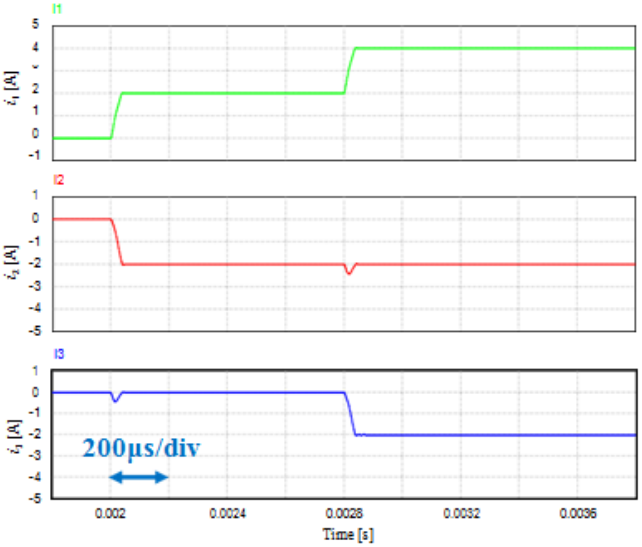


Fig. 8. Simulation result of power flow using three 7-level converters. (*f*PWM=500 kHz)

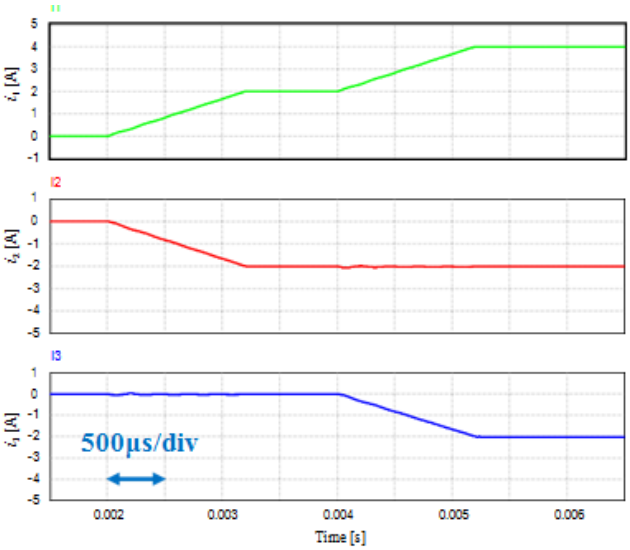


Fig. 9. Simulation result of power flow using three 2-level converters (*f*PWM=83.3 kHz)

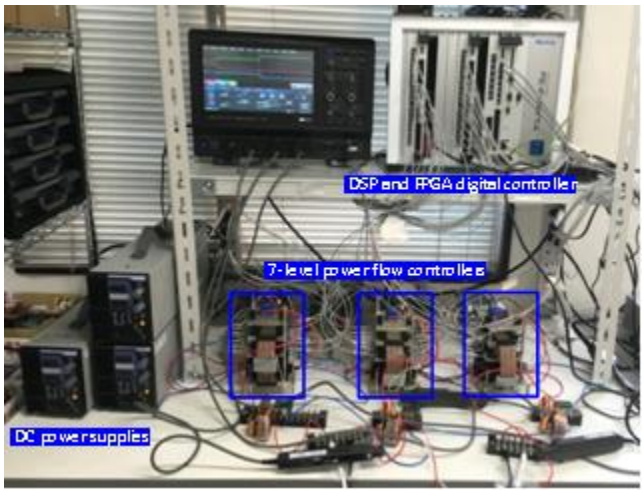


Fig. 10. Experimental setup of 7-level converters.

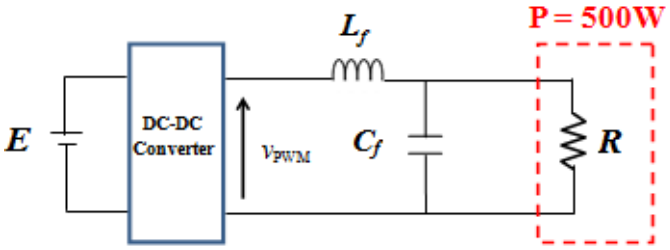


Fig. 11. Circuit for efficiency measurement

TABLE IV
INVESTIGATION CONDITIONS

The number of levels	m	2-level		7-level
Node voltage	E	200 V		
Reference of duty ratio	d	0.5		
Deadtime	T_d	200 ns		
Filter capacitance	C_f	18 nF		
PWM switching frequency	f_{PWM}	83.3 kHz	500 kHz	500 kHz
Filter inductance	L_f	60 mH	10 mH	1.8 mH

TABLE V
RESULT OF EFFICIENCY MEASUREMENT
(OUTPUT POWER: 500 W)

The number of levels	m	2-level		7-level
Output PWM switching frequency	f_{PWM}	83.3 kHz	500 kHz	500 kHz
Efficiency of Converter [%] (Loss [W])	η_{con}	**98.0% (10.8 W)**	**95.1% (25.8 W)**	**96.4% (18.3 W)**
Efficiency of Filter [%] (Loss [W])	η_{filter}	**97.1% (15.4 W)**	**97.9% (10.6W)**	**99.1% (4.3W)**
Efficiency of Converter+Filter [%] (Loss [W])	η_{total}	**95.2 % (26.2 W)**	**93.6 % (36.4 W)**	**95.6 % (22.6 W)**

D. Comparison of current control performance considering the switchinglossin2-leveland7-levelconverters

As discussed in sections III.C and IV.B, a comparison under the same output switching frequency is practically unfair considering the differences in switching loss and efficiency. In this section, the control performance of the 7-level converter with *f*PWM of 500 kHz and 2-level converter with *f*PWM = 83.3 kHz are compared considering the converter efficiency.

Fig. 14 shows the experimental result of the power flow control using three 2-level converters (*f*PWM=83.3 kHz). This result corresponds to the simulation result of Fig. 9. As can be seen, the settling time for the current response in the 2-level converter is 1400 □s. Compared with the result of the 7-level converter for *f*PWM of 500kHz shown in Fig.13,the settlingtime of the current response for *f*PWM of 83.3 kHz is improved by a factor of 28 due to the use of 7-level converter.

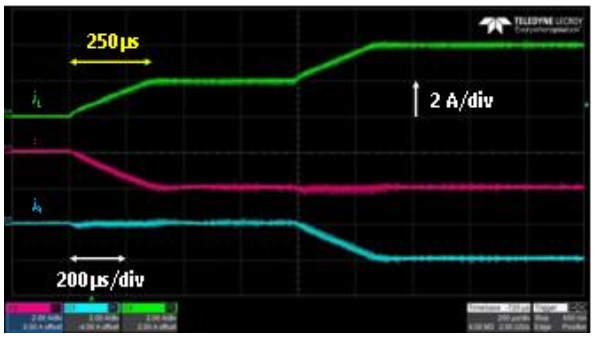


Fig. 12. Experimental result of power flow using three 2-level converters. (*f*PWM=500kHz)

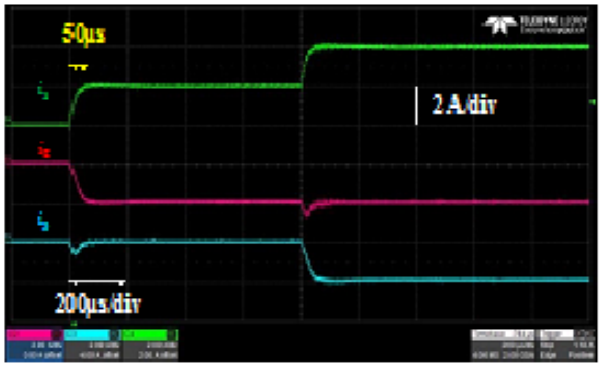


Fig. 13. Experimental result of power flow using three 7-level converters. (*f*PWM=500kHz)

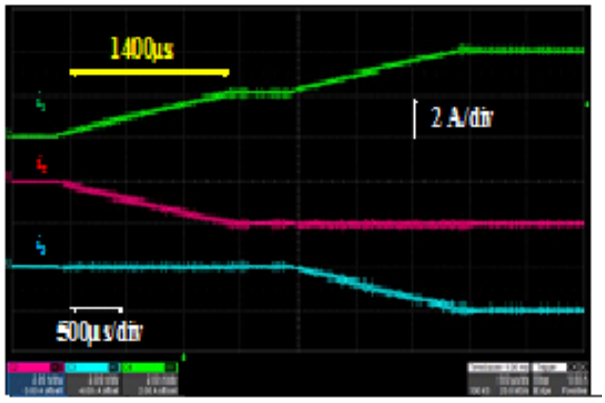


Fig. 14. Experimental result of power flow using three 2-level converters. (*f*PWM=83.3kHz)

V. CONCLUSION

In this study, we investing a ted multi-level converters to realize faster current control in a DC micro grid with extremely low- impedance interconnections. The design procedure for the output filter of the power flow controller was deliberated considering the number of the output levels, steady-state ripple, and gradient of the transient change in the output current. The current-control performances of the 2-

level and 7-level converters were investing a ted using simulations and experiments. The study established that a power flow controller using a multi-level converter realizes faster current control, fixing the current ripple in the same level. In this way, the multi-level power flow controllers are expected to strike a significant impact on small-scale DC distribution networks providing higher stability and reliability based on their faster power flow control.

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