An Impact of Gate Dielectric Material on MOS Devices

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Abstract- *Metal Oxide Field effect transistor (MOS) consists a, controlling Input, called 'Gate electrode', it is often called "gate metal" or "gate conductor", which controls the threshold voltage of the device. The underlying material of this gate terminal is a dielectric, usually silicon -die-oxide. The composite form of Silicon substrate-oxide layer-metal gate, form a MOS transistor. A inversion channel is formed in MOS by applying gate voltage, which is the conduction path in between source and drain. It is seen that, the choice of material for the underlying oxide or dielectric has huge impact on the performance of MOSFET, in terms of output Drain current, breakdown voltage, threshold and so on. Thus, this paper presents an comparative study of various dielectric material and their associative effects on MOSFET. Typical gate materials, which we used to characterize MOSFET are* SiO_2*,* Si_3N_4*,* Al_2O_3 *and* Ta_2O_5*. In addition, a fabrication process simulation and device of n-channel MOSFET in SILVACO TCAD is also done, with simulation of MOSFET* SiO_2 *as a gate electrode.*

Keywords- MOSFET, Gate Dielectric,SiO_2, Si_3N_4, Al_2O_3 and Ta_2O_5.

I. INTRODUCTION

The metal oxide semiconductor field effect transistor also known as MOS transistor is a type of insulated gate field effect transistor, that is fabricated by the controlled oxidation of a semiconductor typically silicon. The MOSFET was invented by Mohamed M. Atalla and DawolKahng at bell labs in 1959.MOSFET can either be manufactured as a part of MOS integrated circuit chips or as a discrete MOSFET device and can take a form of single gate or multi-gate transistor. MOSFET can be made either P type or N type semiconductor. The basic cross sectional view of NMOS with gate electrode is shown in figure 1 [1].

The Gate electrode Source/Drain is formed by Ion-Implantation. Gate electrode may be plucked of Polysilicon, Silica or may be Metal composite such as TIN,Ta_2O_5,Al_2O_3.The material used depend upon intended work function, thus the device type.

The gate dielectric can be made up of single layer high dielectric constant (high-k) material.The use of high-k dielectrics directly subjected on the silicon wafer would demote the short channel performance. High-k dielectric offers a solution to leakage problem that occur at gate oxide as thickness is scaled down. The drain current is increased as dielectric constant of material is increased. But such films with high dielectric constant have stability problems[2].

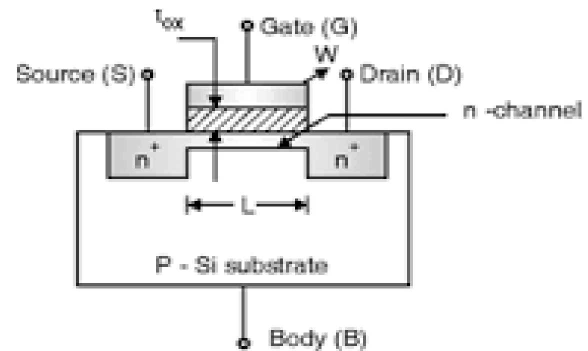


Fig 1: Cross sectional view of NMOS

The primary criteria for the gate material are that it is a good conductor. Highly doped poly crystalline silicon is acceptable but certainly not an ideal conductor, and also suffers from some more technical deficiencies in its role as standard gate material.

Although polysilicon gates has been used since 20 years, they have some disadvantages which have led to their replacement by metal gates. The disadvantages are:

- Polysilicon is not a great conductor hence it reduces the signal propagation speed through the material.
- While scaling down the transistors it is necessary to make gate dielectric layer very thin(around 1nm)[1].

This Paper is organized as follows: Section II represents the literature survey. In Section III, the comparative analysis of various gate materials has been discussed in detail

followed by simulating fabrication of NMOS using SiO_2gate electrode is Section IV .Conclusions are drawn in Section V.

II. LITERATURE SURVEY

The continuous evolution of digital technology is the result of ever shrinking, faster and cheaper transistors that make up the ubiquitous integrated circuit of our devices[3].
In electronics, a self-aligned gate is a transistor manufacturing feature where a refractory gate electrode region of a MOSFET is used as a mask for the doping of the source and drain regions. In this technique the gate will slightly overlap the edges of source and drain.

The use of self-aligned gates in MOS transistors is one of the major innovations that led to the rise in computing power in 1970s. Still self-aligned gates are used in modern integrated circuit processes [4].

The Field Effect Transistor (FET) is the main device for the integrated circuits era. The beginning of FET was the Lilienfeld patent filled in 1925. Experimental MOSFET was designed in 1960s. But it was not fabricated due to the technical difficulties. The classical MOSFET was composed of Aluminum (Metal), silicon dioxide (Oxide) and Silicon (Semiconductor). In order to avoid the short channel effects the classical MOSFET was upgraded with different gate electrode like polysilicon heavily doped,TiN and TaN. In order to boost the carriers mobility the silicon channel has been modified to strained silicon (uniaxial and biaxial), SiGe, Ge, InGaAs. The MOSFET structure has been improved from Bulk MOSFET to SOI (Silicon-on-Insulator) MOSFET and later from planar to vertical multiple-gate devices like FinFET, Triple Gate and Gate all around devices for enhancing the electrostatic coupling. [5].

III. COMPARATIVE ANALYSIS OF VARIOUS GATE DIE-ELECTRIC MATERIAL

The use of a metal gate electrode along with a titanium or tantalum nitride gate dielectric barrier layer can, provide highly reliable semiconductor device having an increased operating speed as compared to conventional transistors.[6]

$SiON/Ta_2O_5$ stacked gate dielectric exhibits 3 - 5orders smaller leakage current than SiO2 at 1.8nm, while the transistor characteristics such as mobility, Id-Vg, and Id-Vd, are similar to those of SiO_2 transistor. N-channel MOSFET with equivalent SiO_2 thickness down to 1.8nm (1.4nm equivalent due to elimination of poly-Si depletion) is demonstrated [7].

A possible future is the use of high mobility materials such as Germanium for the active areas of a transistor instead of Silicon. As a step towards building devices Ge, it is characterize a gate last process with epitaxial deposition of $Si_{0.75}Ge_{0.25}$ source and drain areas on bulk Si wafers. [4].For a high-electron-mobility-transistor using atomic layer deposited (ALD) Al_2O_3 as the gate dielectric.Al_2O_3 offers large band gap(9 eV),High dielectric constant(K~10),High breakdown field (10^7V/cm).The ALD Al_2O_3/AlGaN interface is of high quality and high potential. ALD Al_2O_3/AlGaN proclaim lower gate leakage current.Al_2O_3 make allowance for the effective two dimensional (2D) high electron mobility at AlGaN. It has additional advantages of a debunk low defect density, High uniformity and nanometer scalability [8].

Silicon oxide (SiO_2) has been used as gate dielectric material since the inception of MOSFET in 1960, because of its electrical stability at the interface between Si and SiO_2 and thermal stability. High-speed and compact integrated circuits are achieved by scaling down of physical thickness of the SiO_2 gate dielectrics and gate length. But, the gate leakage current due to direct tunneling of electrons through the SiO_2 will be too high, and circuit power dissipation will increase to unacceptable values, when the gate dielectric goes ultra-thin and less than 1.5 nm. While MOSFETs have been realized at 1.5 nm oxide thickness, a major obstacle to overcome is the high level of direct tunneling current through the gate. One possible solution is to incorporate the use of a high-*K* gate dielectric [9].

Silicon Nitride is used as a sensing film . It has resistant to hydration, large coupling capacitance, high chemical stability and high melting point. Hydrogen ions reside at the surface of the insulator in proportion to the PH[10]. A strong electric field is produced and uniformly distributed over the channel which confirms excellent gate control over the flow of current.

Table1 : Electrical Properties of gate dielectric material

Parameter	Gate Dielectric Material			
	SiO_2	Ta_2O_5	Si_3N_4	Al_2O_3
High dielectric constant (high-k)	Low	High	Medium	High
Leakage current	Low	Medium	Medium	Low
Breakdown fields	Low	High	High	High
Gate capacitance	Low	High	Moderate	High

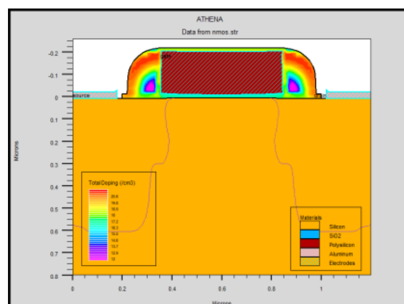
Thus, it is clear from the above table [11][12][13][14][15], that choice of material for gate dielectric is depend upon the device application. For high power operation, say, MOS is used as a power MOS, the device should have high breakdown voltage. High dielectric will also be preferable in this case. Low leakage current, improve the current drive in capability. High gate capacitance improve the charge storage. But at high level of integration it, may be the cause of problem of latch up in MOS.

Thus, optimal selection of gate dielectric is a challenging task. On the basis of application, the material is selected which is performed by modeling of fabrication process from design engineer.

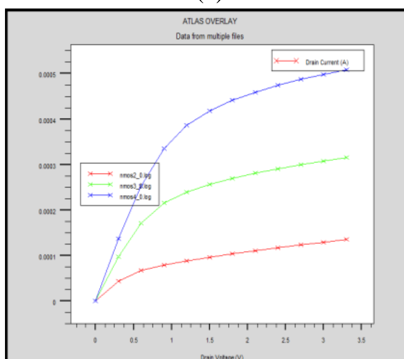
IV. SIMULATION

Process Simulation

Athena™ simulator provides general capabilities for physically-based, simulation of semiconductor processing. Athena™ environment was used to simulate N-channeel MOSFET. Silicon wafer with orientation<100> was used. initially silicon wafer of (0.8x0.6) µm thickness was chosen. Then pattering of field oxide was done. Growth of gate oxide and deposition of silicon dioxide as a sensing layer with a thickness of 0.2 µm was achieved. In the diffusion process, doping of phosphorous was done for source and drain regions. For electrical contacts aluminum metal was used.



(a)



(b)

Fig2: Fabrication of MOSFET (a) Gate Material SiO_2 , (b) of V-I Characteristics curves of MOS

V. CONCLUSION

Silicon nitride is used as sensing film in case of MOSFET. In this paper we have listed several types of dielectric material for gate electrode (Si_3N_4, Ta_2O_5, Al_2O_3, SiO_2). It is been depicted that for advance applications and better performance gate material Ta_2O_5 and Al_2O_3 are preferable over other materials.

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