Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking

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***Abstract*—This paper presents a novel grid-connected boost-half-bridge photovoltaic (PV) microinverter system and its control implementations. In order to achieve low cost, easy control, high efficiency, and high reliability, a boost-half-bridge dc–dc converter using minimal devices is introduced to interface the low-voltage PV module. A full-bridge pulse width-modulated inverter is cascaded and injects synchronized sinusoidal current to the grid. Moreover, a plug-in repetitive current controller based on a fourth-order linear- phase IIR filter is proposed to regulate the grid current. High power factor and very low total harmonic distortions are guaranteed un- der both heavy load and light load conditions. Dynamic stiffness is achieved when load or solar irradiance is changing rapidly. In addition, the dynamic behavior of the boost-half-bridge dc–dc con- verter is analyzed; a customized maximum power point tracking (MPPT) method, which generates a ramp-changed PV voltage ref- erence is developed accordingly. Variable step size is adopted such that fast tracking speed and high MPPT efficiency are both ob- tained. A 210 W prototype was fabricated and tested. Simulation and experimental results are provided to verify the validity and performance of the circuit operations, current control, and MPPT algorithm.**

***Index Terms*—Boost-half-bridge, grid-connected photovoltaic (PV) system, maximum power point tracking (MPPT), photovoltaic microinverter, repetitive current control.**

I. INTRODUCTION

THE concept of microinverter (also known as module-integrated converter/inverter) has become a future trend for single-phase grid-connected photovoltaic (PV) power systems for its removal of energy yield mismatches among PV modules, possibility of individual PV-module-oriented optimal design, independent maximum power point tracking (MPPT), and “plug and play” concept. In general, a PV microinverter system is often supplied by a low-voltage solar panel, which requires a high-voltage step-up ratio to produce desired output ac voltage [1]–[3]. Hence, a dc–dc converter cascaded by an inverter is the most popular topology, in which a HF transformer is often implemented within the dc–dc conversion stage .

In terms of the pulse width modulation (PWM) techniques employed by the PV microinverter system, two major categories are attracting most of the attentions. In the first, PWM control is applied to both the dc–dc converter and the inverter. In addition, a constant voltage dc link decouples the power flow in the two stages such that the dc input is not affected by the double-line-frequency power ripple appearing at the ac side. By contrast, the second configuration utilizes a quasi-sinusoidal PWM method to control the dc–dc converter in order to gen- erate a rectified sinusoidal current (or voltage) at the inverter dc link. Accordingly, a line-frequency-commutated inverter un- folds the dc-link current (or voltage) to obtain the sinusoidal form synchronized with the grid. Although the latter has the advantage of higher conversion efficiency due to the elimination of HF switching losses at the inverter, the double- line-frequency power ripple must be all absorbed by the dc input capacitor, making the MPPT efficiency (defined as the ratio of the energy drawn by the PV inverter within a certain measuring period at the steady state to the theoretical available energy from the PV module) compromised unless a very large capacitance is used. Moreover, the dc–dc conversion stage requires more challenging control techniques to meet the grid current regulation requirement. Therefore, in terms of the MPPT performance and output current quality, the first category of PV microinverter is more appropriate and will be adopted in this paper.

A boost dual-half-bridge dc–dc converter for bidirectional power conversion applications was first proposed in and then further investigated in. It integrates the boost converter and the dual-half-bridge converter together by us- ing minimal number of devices. High efficiency is realizable when the zero-voltage switching (ZVS) technique is adopted. By replacing the secondary half bridge with a diode voltage doubler, a new boost-half-bridge converter can be derived for unidirectional power conversions [15]. In this paper, the boost-half-bridge converter is incorporated as the dc–dc conversion stage for the grid-connected PV microinverter system. Benefiting from its circuit simplicity, ease of control, and minimal semiconductor devices, the promising features such as low cost, high efficiency, and high reliability are obtained.

A full-bridge PWM inverter with an output *LCL* filter is incorporated to inject synchronized sinusoidal current to the grid. In general, its performance is evaluated by the output current total harmonic distortions (THDs), power factor, and dynamic response. Repetitive control (RC) is known as an effective solution for elimination of periodic harmonic errors and has been previously investigated and validated in the uninterruptible power system (UPS) systems, active power filters, boost-based PFC circuits, and grid- connected inverters/PWM rectifiers. In, a fourth- order linear-phase IIR filter has been synthesized for the RC- based UPS systems. This IIR filter is implemented to obtain very high system open-loop gains at a large number of harmonic fre- quencies such that the harmonic rejection capability is greatly enhanced. In this paper, a plug-in repetitive current controller is proposed. It is composed of a proportional part and an RC part, to which the IIR filter in [24] is accommodated. The proposed current controller exhibits the following superior features:

1) high power factor is obtained;
2) current harmonic distortions (up to the 13th-order) caused by the grid voltage nonideality are minimized;
3) outstanding current regulation is guaranteed within a wide range of load conditions;
4) fast dynamic response is achieved during the transients of load or solar irradiance change.

MPPT is performed by the boost-half-bridge dc–dc converter. Numerous MPPT techniques have been studied and validated, for example, perturb and observe (P&O) method, incremental conductance method, ripple correlation method, reduced current sensor method, etc. Different tech- niques have shown different tradeoffs among the steady-state MPPT efficiency, the transient tracking speed, and the control complexity. Another critical concern for MPPT implementation is the dynamics of the specific converter adopted. In, an optimal P&O method has been developed to limit the negative effect of the converter dynamic responses on the MPPT efficiency. In, a closed-loop control technique has been proposed to minimize the PV voltage oscillation. How- ever, the converter dynamic behavior associated with the MPPT operation can also influence the converter efficiency and functioning, which has been rarely discussed previously. For example, the MPPT methods using step-changed perturbations on the PV voltage (or current) or the converter duty cycle periodically may sometimes cause problems such as inrush current, *LC* oscillation, magnetic saturation, etc. These undesirable transient responses can result in higher power losses or even circuit malfunctioning, and of course, they are different from case to case. In this paper, the dynamics of the boost-half-bridge converter is carefully studied for guiding the MPPT design. A customized MPPT producing a ramp-changed PV voltage is then developed for practice. In addition, for the purpose of fast tracking and high MPPT efficiency, the power–voltage (*P*–*V*) curve of the PV module is divided into three different operation zones, where the MPPT step size is varied accordingly.

II. BOOST-HALF-BRIDGE PV MICROINVERTER

The boost-half-bridge microinverter topology for grid-connected PV systems is depicted in Fig. 1. It is composed of two decoupled power processing stages. In the front-end dc–dc converter, a conventional boost converter is modified by splitting the output dc capacitor into two separate ones. C_{in} and L_{in} denote the input capacitor and boost inductor, respectively. The center taps of the two MOSFETs (S_1 and S_2) and the two output capacitors (C_1 and C_2) are connected to the primary terminals of the transformer T_r, just similar to a half bridge. The transformer leakage inductance reflected to the primary is represented by L_s and the transformer turns ratio is $1 : n$. A voltage doubler composed of two diodes (D_1 and D_2) and two capacitors (C_3 and C_4) is incorporated to rectify the transformer secondary voltage to the inverter dc link. A full-bridge inverter composed of four MOSFETs (S_3 –S_6) using synchronized PWM control serves as the dc–ac conversion stage. Sinusoidal current with a unity power factor is supplied to the grid through a third-order *LCL* filter (L_{o1}, L_{o2}, and C_o).

Other symbol representations are defined as follows. The duty cycle of S_1 is denoted by d_1. The switching period of the boost-half-bridge converter is T_{sw1} . The PV current and voltage are represented by i_{PV} and v_{PV} , respectively. The voltages across C_1, C_2, C_3, and C_4 are denoted by v_{c1}, v_{c2}, v_{c3}, and v_{c4}, respectively. The transformer primary voltage, secondary voltage, and primary current are denoted as v_{r1} , v_{r2} , and i_{r1} , respectively. The low-voltage side (LVS) dc-link voltage is v_{dc1} and the high-voltage side (HVS) dc-link voltage is v_{dc2}. The switching period of the full bridge inverter is T_{sw2}. The output ac currents at the inverter side and the grid side are represented by i_{inv} and i_g , respectively. The grid voltage is v_g.

The boost-half-bridge converter is controlled by S_1 and S_2 with complementary duty cycles. Neglect all the switching dead bands for simplification. The idealized transformer operating waveforms are illustrated in Fig. 2. When S_1 is ON and S_2 is OFF, v_{r1} equals to v_{c1} . When S_1 is OFF and S_2 is ON, v_{r1} equals to v_{c2} . At the steady state, the transformer volt-second is always automatically balanced. In other words, the primary volt-second A_1 (positive section) and A_2 (negative section) are equal, so are the secondary volt-sec A_3 (positive section) and A_4 (negative section). Normally, D_1 and D_2 are ON and OFF in a similar manner as S_1 and S_2, but with a phase delay t_{pd} due to the transformer leakage inductance. Ideally, the transformer current waveform is determined by the relationships of $v_{c1} - -v_{c4}$, the leakage inductance L_s, the phase delay t_{pd}, and S_1 's turn-ON time $d_1 T_{\text{sw1}}$.

In order to reach an optimal efficiencyofthe boost-half-bridge converter, ZVS techniques can be considered for practical implementation. It is worth noting that engineering tradeoffs must be made between the reduced switching losses and increased conduction losses when soft switching is adopted. Detailed optimal design processes of the boost-half-bridge con- verter will not be addressed in this paper.

For simplicity, hard switching is employed and the transformer leakage inductance is regarded as small enough in this paper. Therefore, (1) and (2) can be derived as follows:

$$v_{c1} = \frac{(1 - d_1)}{d_1} v_{\text{PV}} \qquad v_{c2} = v_{\text{PV}} \qquad v_{\text{dc1}} = \frac{v_{\text{PV}}}{d_1} \tag{1}$$

$$v_{c3} = \frac{n(1 - d_1)}{d_1} v_{\text{PV}} \qquad v_{c4} = n v_{\text{PV}} \qquad v_{\text{dc2}} = \frac{n v_{\text{PV}}}{d_1}. \tag{2}$$

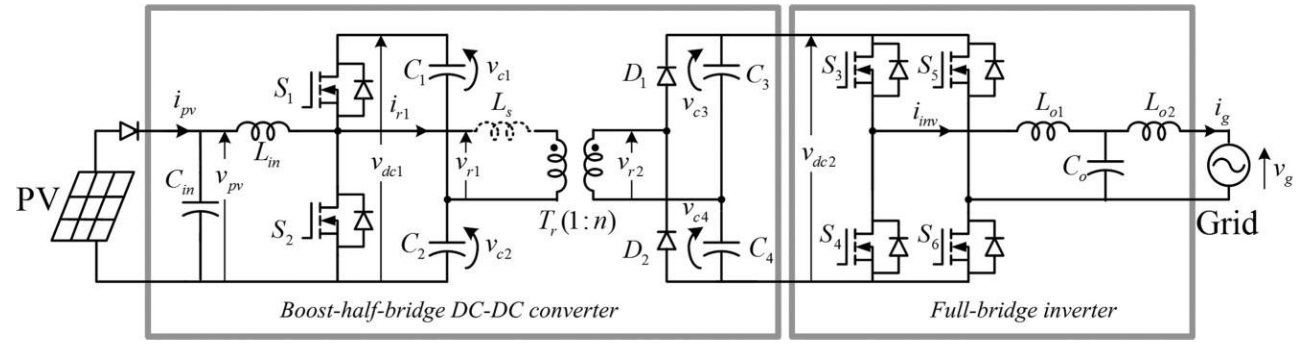

Fig. 1. Topology of the boost-half-bridge PV microinverter.

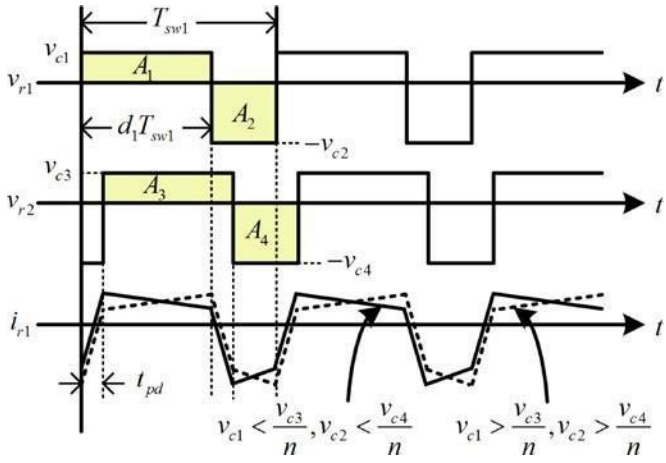

Fig. 2. Idealized transformer voltage and current.

When viewing from the full-bridge inverter, the boost-half-bridge converter just operates identically as a conventional boost converter, but with the extra features of the galvanic isolation as well as the high step-up ratio. The simple circuit topology with minimal use of semiconductor devices exhibits a low total cost and good reliability.

III. SYSTEM CONTROL DESCRIPTION

An all-digital approach is adopted for the control of the boost-half-bridge PV microinverter system, as shown in Fig. 3. The PV voltage v_{PV} and current i_{PV} are both sensed for calculation of the instantaneous PV power P_{PV}, the PV power variation ΔP_{PV}, and the PV voltage variation Δv_{PV}. The MPPT function block generates a reference v^*_{PV} for the inner loop of the PV voltage regulation, which is performed by the dc–dc converter. At the inverter side, the grid voltage v_g is sensed to extract the instantaneous sinusoidal angle θ_g, which is commonly known as the phase lock loop. The inverter output current i_{inv} is pre-filtered by a first-order low-pass filter on the sensing circuitry to eliminate the HF noises. The filter output i^{f}_{inv} is then fed back to the plug-in repetitive controller for the inner loop regulation. Either v_{dc1} or v_{dc2} can be sensed for the dc-link voltage regulation as the outer loop. In practice, the LVS dc-link voltage v_{dc1} is regulated for cost effectiveness. The grid current and the LVS dc-link voltage references are represented by i^*_{inv} and v^*_{dc1}, respectively.

In order to achieve fast dynamic responses of the grid current as well as the dc-link voltage, a current reference feedforward is added in correspondence to the input PV power P_{PV}. The magnitude of the current feed forward is expressed as follows:

$$|i_{\mathrm{inv}}|_{ff} = \frac{2P_{\mathrm{PV}}}{|v_g|} \tag{3}$$

where $|v_g|$ is the magnitude of the grid voltage and can be calculated by

$$|v_g| = \frac{1}{2}\int_0^{\pi} v_g d\theta_g. \tag{4}$$

IV. PLUG-IN REPETITIVE CURRENT CONTROLLER

So far, using an *LCL* filter in a grid-connected inverter system has been recognized as an attractive solution to reduce current harmonics around the switching frequency, improve the system dynamic response, and reduce the total size and cost. Typically, an undamped *LCL* filter exhibits a sharp *LC* resonance peak, which indicates a potential stability issue for the current regulator design. Hence, either passive damping or active damping techniques can be adopted to attenuate the resonance peak below 0 dB. On the other hand, a current regulator without introducing any damping method can also be stabilized, as long as the *LCL* parameters and the current sensor location are properly selected. In this paper, the *LCL* parameters are selected by following the guidelines provided in the current sensor is placed at the inverter side instead of the grid side. Resultantly, no damping techniques are needed such that the current control is much simplified. Table I summarizes the key parameters of the full-bridge inverter.

A. Plant Transfer Function

The control-output-to-inverter-current transfer function in the continuous time domain can be derived as (5), where r_1 and r_2 represent the equivalent series resistance of L_{o1} and L_{o2}, respectively. Based on the power loss estimation of the inductors, $r_1 = 1.4\ \Omega$ and $r_2 = 1.0\ \Omega$

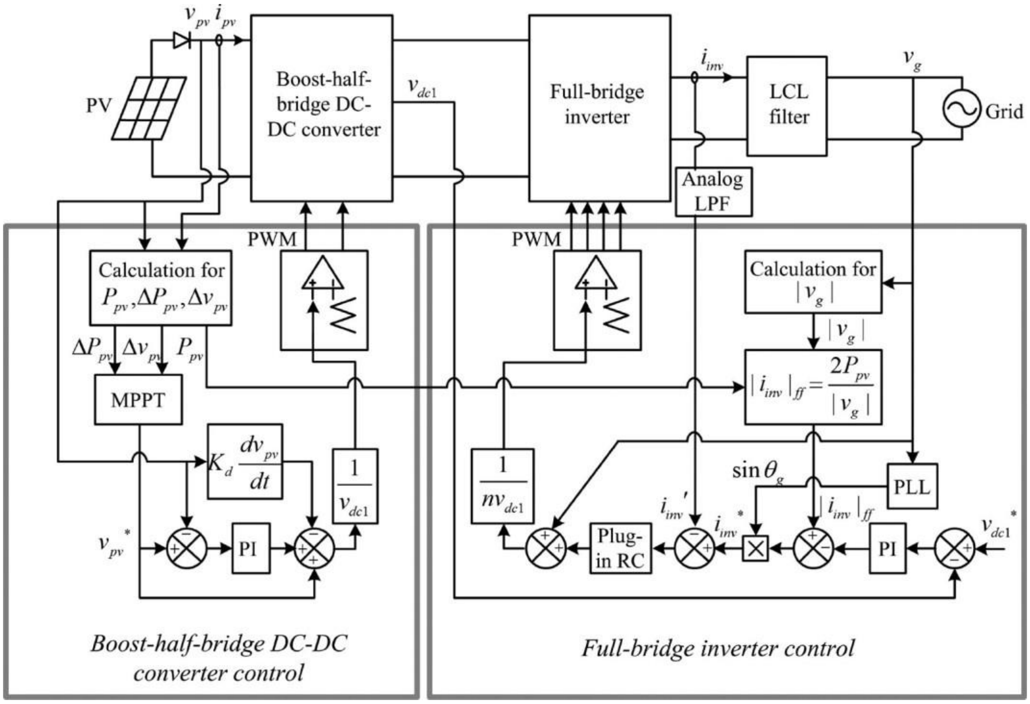

Fig. 3. Architecture of the proposed PV microinverter system control.

TABLE I
FULL-BRIDGE INVERTER PARAMETERS

HVS DC link voltage	370 V
Switching frequency	10.8 kHz
Sampling frequency	10.8 kHz
Rated output power	210 W
Grid voltage	180
Grid line frequency	60 Hz
Filter inductor (L_{o1}, L_{o2})	8.5 mH
Filter capacitor (C_o)	330 nF

From (5), as shown at the bottom of this page, the *LC* resonance frequency is

$$\omega_r = \sqrt{\frac{r_1 r_2 C_o + L_{o1} + L_{o2}}{L_{o1} L_{o2} C_o}}. \tag{6}$$

The system hardware and software delay is summarized as T_d, which is typically around one and a half sampling period (T_d = 140 us). In order to reduce the switching noises in the sensed inverter current, an analog low-pass filter (7) is placed on the current feedback path

$$F_{\text{LPF}}(s) = \frac{\omega_{\text{fc}}}{s + \omega_{\text{fc}}}. \tag{7}$$

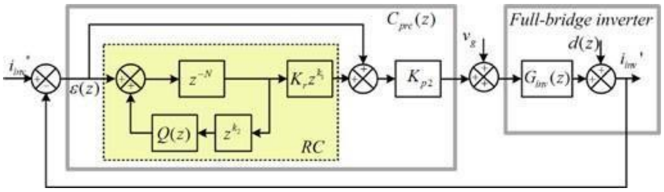

Fig. 4. Block diagram of the proposed plug-in repetitive controller.

The cutoff frequency is chosen as $\omega_{\text{fc}} = 4\times10^4$ rad/s. Therefore, by using the zero-order hold discretization scheme, the entire plant combining (5) and (7) can be discretized as (8), as shown at the bottom of this page.

B. Plug-In RC Scheme

The plug-in digital repetitive controller is designed, as shown in Fig. 4. The conventional proportional controller with a gain of K_{p2} is incorporated to guarantee fast dynamics. The RC is then plugged in and operates in parallel with the proportional controller.

$\varepsilon(z)$ and $d(z)$ represent the tracking error and the repetitive disturbances, respectively.

The modified internal model [33], which is denoted by the positive feedback loop inside the RC, plays the most critical role

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$$G_{LCL}(s) = \frac{L_{o2} C_o s^2 + r_2 C_o s + 1}{L_{o1} L_{o2} C s^3 + (r_1 L_{o2} + r_2 L_{o1}) C_o s^2 + (r_1 r_2 C_o + L_{o1} + L_{o2}) s + r_1 + r_2} e^{-sT_d}. \tag{5}$$

$$G_{\text{inv}}(z) = \frac{0.00265z^{-2} + 0.00548z^{-3} + 0.00474z^{-4} + 0.00559z^{-5} + 0.000254z^{-6}}{1 + 0.5468z^{-1} - 0.5653z^{-2} - 0.9606z^{-3} + 0.024z^{-4}} \tag{8}$$

in the proposed current regulator. z^{-N} is the time delay unit, where N denotes the number of samples in one fundamental period. In an ideal RC, a unity gain is along the positive feedback path such that all the repetitive errors based on the fundamental period are completely eliminated when the system reaches equilibrium. However, in order to obtain a sufficient stability margin, a zero-phase low-pass filter is often incorporated rather than the unity gain. This can be realized by cascading a linear-phase low-pass filter $Q(z)$ and a noncausal phase lead compensator z^{k_2}. z^{k_1} is another noncausal phase lead unit, which compensates the phase lag of $G_{\text{inv}}(z)$, particularly, at HFs. Here k_1 and k_2 both stand for the number of sampling periods. K_r is the constant gain unit that determines the weight of the RC in the whole control system.

From Fig. 4, the transfer function of the entire plug-in RC current regulator can be described as follows:

$$C_{\text{prc}}(z) = \frac{K_r K_{p2} z^{-N} z^{k_1}}{1 - Q(z) z^{k_2} z^{-N}} + K_{p2}. \qquad (9)$$

C. Analysis and Design of the Plug-In RC

The selection of K_{p2} follows exactly the same rules as the conventional proportional controller design. Basically, it requires a tradeoff between the obtainable stability margin and the current regulation performance. In this paper, $K_{p2} = 50$.

From Fig. 4, the tracking error $\varepsilon(z)$ can be derived as follows:

$$\varepsilon(z) = \varepsilon(z) z^{-N} \left(Q(z) z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{\text{inv}}(z)}{1 + K_{p2} G_{\text{inv}}(z)} \right) + \left(\frac{1 - Q(z) z^{k_2} z^{-N}}{1 + K_{p2} G_{\text{inv}}(z)} \right) [i^*_{\text{inv}}(z) - d(z)] \qquad (10)$$

It is noticeable that a larger K_{p2} will result in a smaller tracking error during the transient because the second summation term on the right side of (10) is reduced. This exactly explains the function of the proportional control part

Let

$$|H(z)|_{z=e^{j\omega T_{\text{sw}2}}} = \left| Q(z) z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{\text{inv}}(z)}{1 + K_{p2} G_{\text{inv}}(z)} \right|, \quad \omega \in \left(0, \frac{\pi}{T_{\text{sw}2}} \right)$$

in which $T_{\text{sw}2}$ is also the sampling period. A sufficient condition to meet the stability requirement is

$$\left| H(e^{j\omega T_{\text{sw}2}}) \right| < 1. \qquad (11)$$

At the fundamental and harmonic frequencies, z^{-N} is simply equal to unity. Hence, the steady-state error can be derived from (10) as follows:

$$|\varepsilon(z)| = |i^*_{\text{inv}}(z) - d(z)| \left| \frac{1 - Q(z) z^{k_2}}{[1 + K_{p2} G_{\text{inv}}(z)][1 - H(z)]} \right|. \qquad (12)$$

From (11) and (12), the general design criteria of $Q(z)$ for obtaining a good stability as well as a small steady-state error can be summarized as: 1) $Q(z)$ must have sufficient attenuation at HFs; 2) $Q(z)$ must be close to unity in a frequency range,

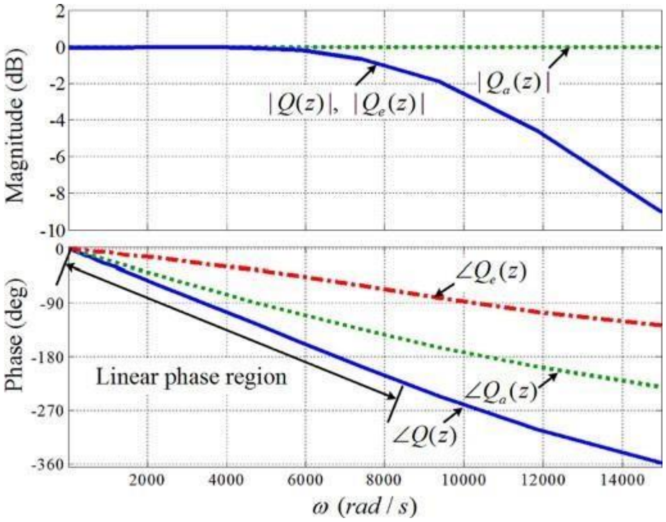


Fig. 5. Bode plots of $Q_e(z)$, $Q_a(z)$, and $Q(z)$.

which covers a large number of harmonics; and 3) $Q(z)z^{k_2}$ must have a zero phase when $Q(z)$ is close to unity.

In a fourth-order linear-phase IIR filter has been synthesized for the repetitive voltage controller for UPS systems. Compared with the conventional linear-phase finite impulse response filters used for RC, the linear-phase IIR filter exhibits a flat gain in the passband and a much faster roll off in the transition band, when the filter order. Hence, it is a good candidate for th. repetitive current controller in this paper as well.

In practice, $Q(z)$ is synthesized by cascading a second-order elliptic filter $Q(z)$ and a second-order all-pass phase equalizer $Q_a(z)$. $Q(z)$, $Q_e(z)$, and $Q_a(z)$ are obtained from MATLAB and expressed by (13)–(15)

$$Q(z) = Q_e(z) Q_a(z) \qquad (13)$$

$$Q_e(z) = \frac{0.1385 + 0.2564 z^{-1} + 0.1385 z^{-2}}{1 - 0.7599 z^{-1} + 0.2971 z^{-2}} \qquad (14)$$

$$Q_a(z) = \frac{0.1019 - 0.6151 z^{-1} + z^{-2}}{1 - 0.6151 z^{-1} + 0.1019 z^{-2}} \qquad (15)$$

The bode plots of $Q(z_e)$, $Q(z)_a$, and $Q(z)$ are shown in Fig. 5. The linear-phase region of $Q(z)$ is from 0 to 1403 Hz (8816 rad/s). In order to compensate the phase delay of $Q(z)$ to zero in this region, $k_2 = 5$ is selected. The maximum passband gain and the cutoff frequency of $Q(z)$ are 0.9975 and 1670 Hz, respectively.

The locus of $H(e^{j\omega T_{\text{sw}2}})$ is useful for guiding the selection of K_r and k_1. The fundamental principle for choosing K_r and k_1 is that $H(e^{j\omega T_{\text{sw}2}})$ should keep a sufficient margin from the unity circle when ω increases from 0 to the nyquist frequency $\pi/T_{\text{sw}2}$. When K_r and k_1 are assigned with different values, $H(e^{j\omega T_{\text{sw}2}})$ can be plotted in Fig. 6(a) and (b). In Fig. 6(a), K_r is fixed, $k_1 = 4$ renders a good stability margin. Likewise, $K_r = 0.3$ would be an appropriate choice from Fig. 6(b).

The open-loop gain of the plug-in RC system is denoted as $|C_{\text{prc}}(z) G_{\text{inv}}(z)|$. In particular, the magnitude of

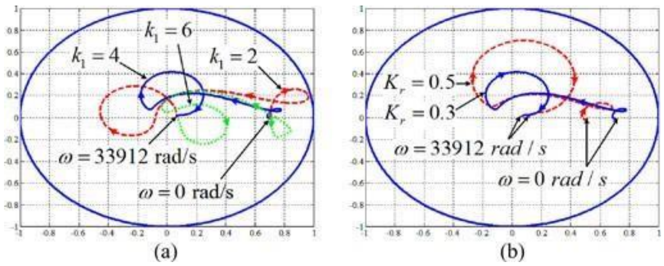


Fig. 6. Locus of the vector $H\,(e^{j\omega T_{sw2}})$. (a) $K_r = 0.3$, k_1 is varying; (b) $k_1 = 4$, K_r is varying.

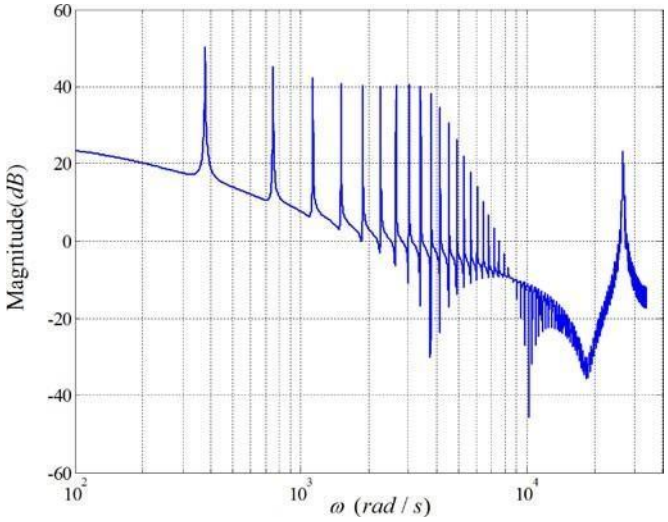


Fig. 7. Frequency response of $|C_{\mathrm{prc}}(z)G_{\mathrm{inv}}(z)|$.

$|C_{\mathrm{prc}}(z)G_{\mathrm{inv}}(z)|$ at the fundamental frequency and high-order harmonic frequencies determines the steady-state tracking error. The frequency response of $|C_{\mathrm{prc}}(z)G_{\mathrm{inv}}(z)|$ is plotted in Fig. 7. The gain peaks are higher than 40 and 20 dB at the harmonic frequencies up to the 9th order and 13th order, respectively, yielding an excellent harmonic rejection capability.

V. BOOST-HALF-BRIDGE CONVERTER CONTROL

Table II summarizes the key parameters of the boost-half-bridge dc–dc converter. As aforementioned, the PV voltage is regulated instantaneously to the command generated by the MPPT function block. The continuous-time control block diagram is shown in Fig. 8. High bandwidth proportional-integral control is adopted to track the voltage reference v^*_{PV} and to minimize the double-line-frequency disturbance from the LVS dc link. The capacitor voltage differential feedback is introduced for active damping of the input *LC* resonance [48].

Typically, the MPPT function block in a PV converter/inverter system periodically modifies the tracking reference of the PV voltage, or the PV current, or the modulation index, or the converter duty cycles. In most cases, these periodic perturbations yield step change dynamic responses in power converters. If the converter dynamics are disregarded in the MPPT control, undesirable transient responses such as *LC* oscillation, inrush current, and magnetic saturation may take place. Consequently, the conversion efficiency can be deteriorated or even malfunction of the converter may occur.

TABLE II
BOOST-HALF-BRIDGE CONVERTER PARAMETERS

Input PV voltage (MPPT)	30 V~50 V
Nominal PV power	210 W
Switching frequency	21.6 kHz
LVS DC link voltage	63 V
Transformer turns ratio	1:6
Transformer magnetizing inductors	0.7 mH:25.2 mH
Input inductor (L_{in})	200 uH

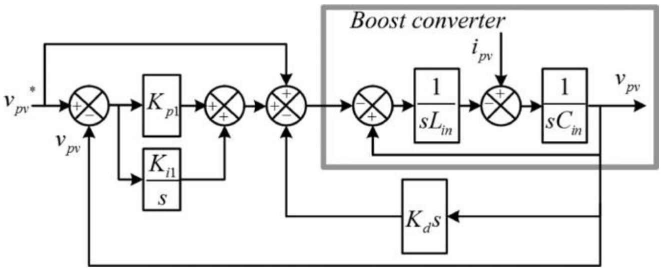


Fig. 8. Block diagram of the PV voltage regulator.

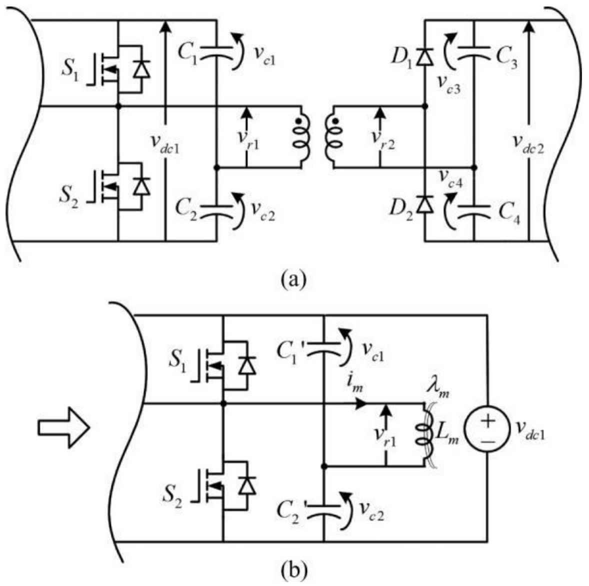


Fig. 9. (a) Half-bridge converter part. (b) Equivalent circuit seen from the LVS dc link of (a).

Equations (1) and (2) indicate that v_{c1}–v_{c4} are changing dynamically in accordance with d_1 . It is worth noting that the charge and discharge of C_1 –C_4 caused by the uneven voltage distribution on the upper capacitors (C_1 and C_3) and the lower capacitors (C_2 and C_4) can only be conducted through the transformer magnetizing inductor. As a result, at any time, the charge and discharge rate of C_1 –C_4 must be limited such that the transformer flux is not saturated. Intuitively, this can be done by either introducing the transformer flux as a state variable into the inner PV voltage regulator or designing the

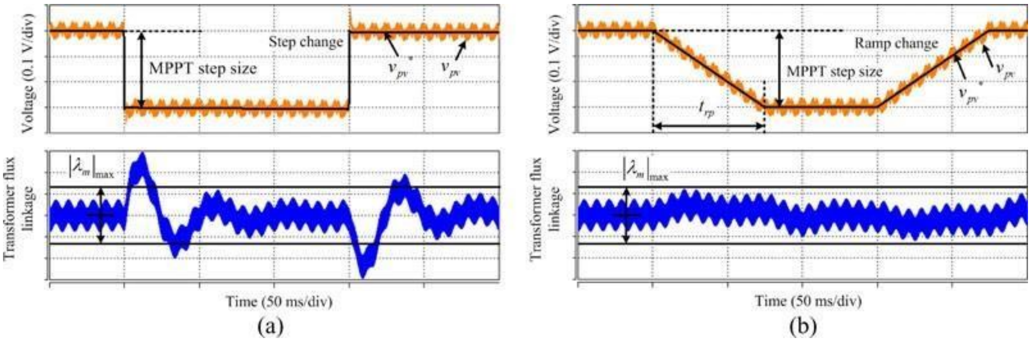


Fig. 10. Dynamic responses corresponding to the different voltage reference generation methods in the MPPT. (a) Using a step-changed voltage reference. (b) Using a ramp-changed voltage reference.

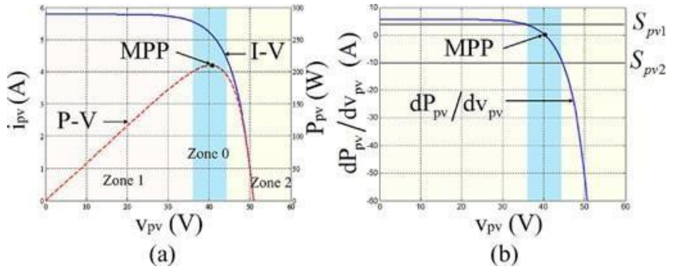


Fig. 11. (a) *I–V*, *P–V* curves. (b) PV operation zone division based on dP_{PV}/dv_{PV}.

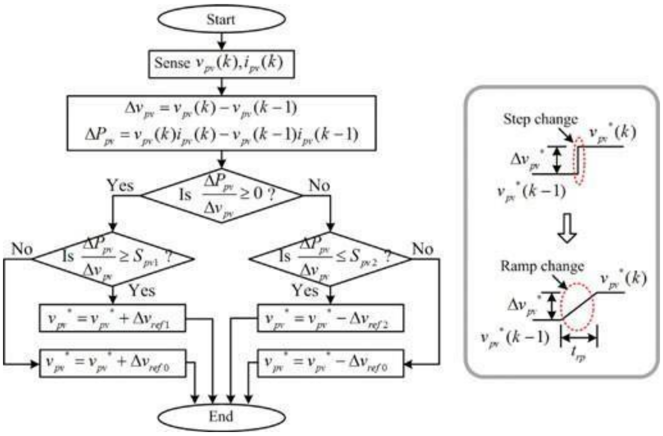


Fig. 12. Flow chart of the variable step-size MPPT.

outer MPPT block adaptively. For the sake of control simplicity and low cost, developing a customized MPPT method by carefully taking care of the boost-half-bridge converter dynamics would be more desirable.

A. Dynamics of the Boost-Half-Bridge Converter

As previously discussed, the boost-half-bridge converter can be regarded as the integration of two subcircuit topologies: 1) the boost converter and 2) the half-bridge converter. The PV voltage regulator depicted in Fig. 8 has ensured that both the steady state and the dynamic response of the boost converter part are taken care of. Hence, the following analysis will be only concentrated on the dynamics of the half-bridge converter part.

The major role of the half-bridge converter here is to transfer energy from the LVS dc link to the HVS dc link through the transformer. But besides that, it also allocates the amount of stored charges on the upper dc-link capacitors (C_1 and C_3) and the lower dc-link capacitors (C_2 and C_4).

Neglecting the effect of the transformer leakage inductance and power losses at this time, Fig. 9 depicts the extracted half-bridge converter part and its equivalent circuit seen from the LVS dc link. As v_{dc1} is regulated to a constant dc, the LVS dc link in Fig. 9(b) is simplyconnected to a constant voltage source for approximation. C_3 and C_4 are both reflected to the transformer primary and combined with C_1 and C_2. C'_1 and C'_2 stand for the equivalent dc-link capacitors, where $C'_1 = C_1 + n^2 C_3$ and $C'_2 = C_2 + n^2 C_4$. L_m, i_m, and λ_m denote the transformer primary magnetizing inductor, dc current, and dc flux linkage, respectively. At the steady state, both i_m and λ_m are zero. But once the converter duty cycle d_1 is perturbed, i_m and λ_m will increase or decrease such that the electric charges can be transferred from C'_1 to C'_2 or vice versa. According to the Faraday's law, one has

$$v_{c1}(t) d_1(t) - v_{c2}(t)(1 - d_1(t)) = \frac{d\lambda_m(t)}{dt}. \tag{16}$$

Define the duty cycle change rate $d'_1(t) = d(d_1(t))/dt$. Take derivative on both sides of (16), then

$$v_{dc1} d'_1(t) - \frac{dv_{c2}(t)}{dt} = \frac{d^2 \lambda_m(t)}{dt}. \tag{17}$$

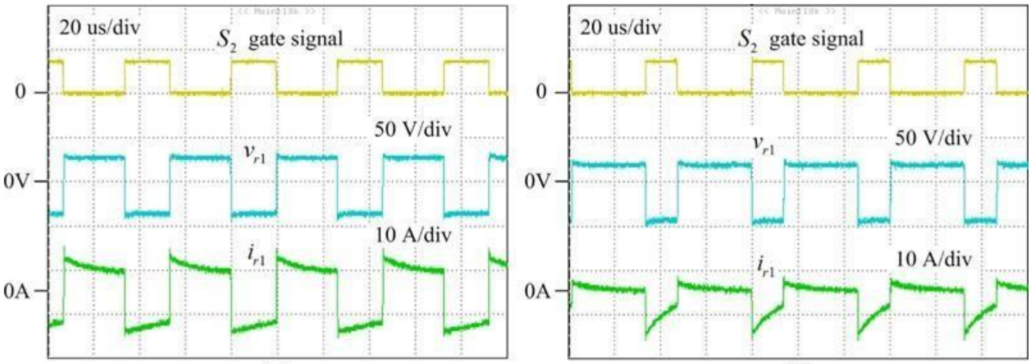
Furthermore, the capacitor charge and discharge equation can be expressed as follows:

$$(C'_1 + C'_2) \frac{dv_{c2}(t)}{dt} = i_m(t) = \frac{\lambda_m(t)}{L_m}. \tag{18}$$

Plug (18) into (17), then

$$\frac{d^2\lambda_m(t)}{dt} + \frac{\lambda_m(t)}{L_m(C'_1 + C'_2)} - v_{dc1} d'_1(t) = 0. \tag{19}$$

Equation (19) describes the dynamics of a typical second-order system, where $d'_1(t)$ is the excitation and $\lambda_m(t)$ is the response. If d_1 is constant initially (at the steady state) and then perturbed by the MPPT operation, λ_m will start to oscillate with a



(a) (b)

Fig. 13. Transformer voltage and current responses of the boost-half-bridge converter. (a) $P_{PV} = 190$ W, $v_{PV} = 36.8$ V. (b) $P_{PV} = 74$ W, $v_{PV} = 44.5$ V.

frequency of $1/(2\pi\sqrt{L_m(C'_1 + C'_2)})$. Defining the magnitude of λ_m as $|\lambda_m|$ and assumimg $d'_1(t) = d'_1$ as a constant, one has

$$|\lambda_m| = 2v_{dc1}L_m(C'_1 + C'_2)d'_1 \tag{20}$$

Assume that $|\lambda_m|_{max}$ is the maximum permissible flux linkage in the transformer for avoidance of the magnetic saturation, then the constraint for the duty cycle change rate is given by

$$d'_1 < \frac{|\lambda_m|_{max}}{2v_{dc1}L_m(C'_1 + C'_2)}. \tag{21}$$

B. MPPT With a Ramp-Changed Voltage Reference

Generally speaking, L_m and $(C'_1 + C'_2)$ are relatively large because of the high permeability of the transformer core and the required energy storage capability of the dc-link capacitors to absorb the double-line-frequency power ripple. Therefore, the constraint given by (21) can hardly be satisfied if an MPPT method that produces a step-changed voltage reference is implemented. In order to strictly follow (21), a customized MPPT method that periodically generates a ramp-changed voltage reference is developed in this paper.

Applying the system control provided in Fig. 3, the simulation results of the boost-half-bridge converter are depicted in Fig. 10. The step-changed voltage reference and the ramp-changed voltage reference are implemented for MPPT, respectively. Transformer leakage inductance and power losses are both taken into account in the simulation. From Fig. 10, it is noticeable that λ_m has an average of zero with the double-line-frequency ripple when the PV voltage is constant. An oscillation of λ_m occurs once the PV voltage is perturbed by the MPPT operation. The slope of the voltage ramp in Fig. 10(b) is chosen in consistency with (21). Here, the MPPT step size is selected as 0.3 V. The time duration of the voltage ramp in Fig. 10(b) is denoted by t_{rp}. In this paper, $t_{rp} = 75$ ms. One can clearly see that with the ramp-changed voltage reference, the transformer flux linkage is well confined within the permissible range.

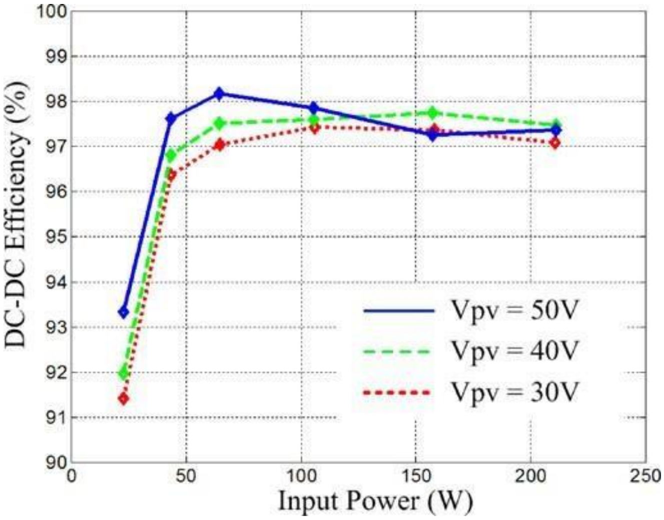
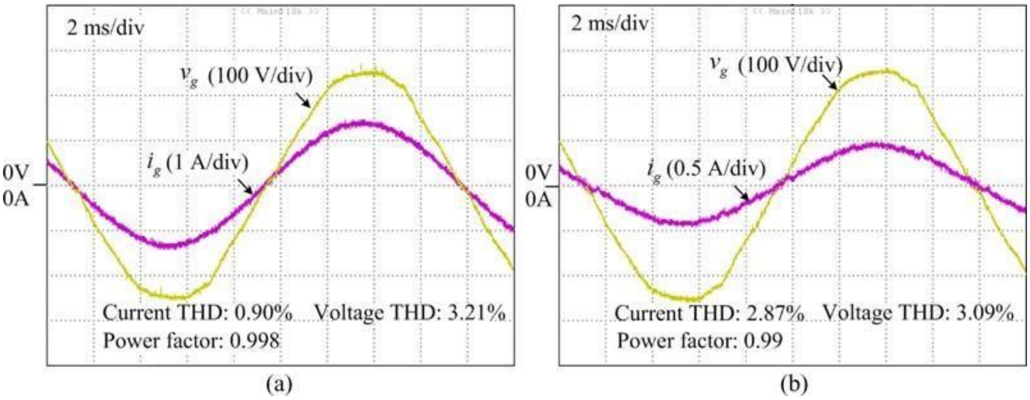


Fig. 14. Efficiency chart of the boost-half-bridge dc–dc converter.

C. Variable Step-Size MPPT Algorithm

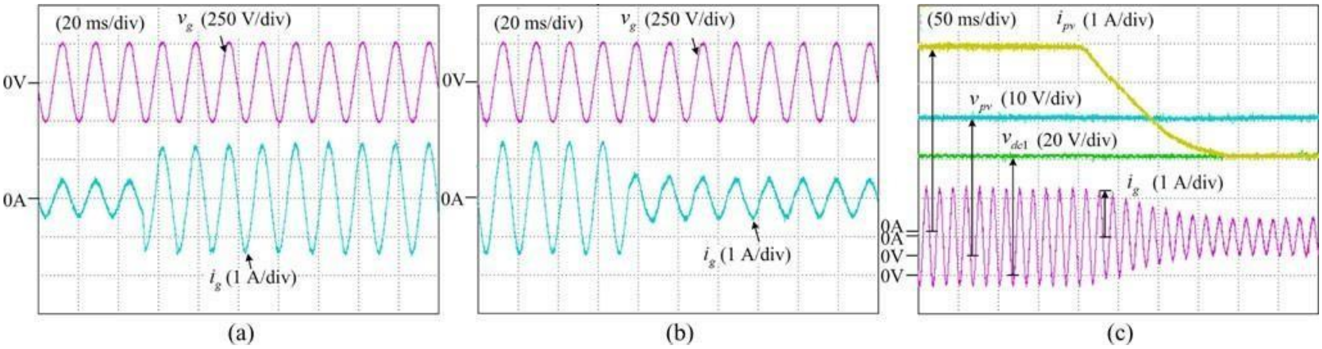
For simplicity, it is assumed that the PV module is working under the standard irradiance (1000 W/m²) and the room temperature (25 °C). Fig. 11(a) sketches the operation curves of Sanyo HIT-210N, which best fits the proposed microinverter. In Fig. 11(b), dP_{PV}/dv_{PV} is illustrated. It is worth mentioning that some MPPT techniques calculate the step size online relying on the instantaneous values of ΔP_{PV} and Δv_{PV} in order to make the MPPT more adaptive. However, the sensed ΔP_{PV} and Δv_{PV} are vulnerable to noises, particularly, when they are small. Therefore, an alternative method is adopted for robustness. Two points S_{PV1} and S_{PV2} on the dP_{PV}/dv_{PV} curve are selected to divide the PV operating points into three different zones, as shown in Fig. 11(b). In zone 0, PV output power is close to the MPP, where a fine tracking step size is used to approach the exact MPP. In zones 1 and 2, a larger tracking step size is applied to boost up the tracking speed.

The adopted MPPT algorithm is shown in Fig. 12. The tracking step sizes in zones 0, 1, and 2 are represented by Δv_{ref0}, Δv_{ref1}, and Δv_{ref2}, respectively. k denotes the iteration number. In practice, Δv_{ref0}, Δv_{ref1}, and Δv_{ref2} are selected as 0.1, 0.3, and 0.3 V, respectively. The PV voltage reference v^*_{pv} is updated every 150 ms.



(a) (b)

Fig. 15. Steady-state grid voltage and current. (a) Heavy load. (b) Light load.



(a) (b) (c)

Fig. 16. Transient responses of the microinverter system under load and solar irradiance change. (a) Grid current step change (0.33–1 A). (b) Grid current step change (1–0.33 A). (c) Solar irradiance change (840 W/m² to partial shading).

VI. EXPERIMENTAL RESULTS

A 210 W boost-half-bridge PV microinverter has been built and experimentally tested in the laboratory. The microinverter is controlled by the 32-bit DSP (TI TMS320F28035). One Sanyo PV module (HIT-210N) is selected as the low-voltage power source. The validity of the boost-half-bridge dc–dc converter, the plug-in repetitive current controller, and the variable step size MPPT method are verified by the following experimental results.

A. Verification of the Boost-Half-Bridge DC–DC Converter

The experimental waveforms of the boost-half-bridge dc–dc converter are obtained in Fig. 13. In Fig. 13(a), the PV voltage is regulated to 36.8 V and the PV power is 190 W. In Fig. 13(b), the PV voltage and power are 44.5 V and 84 W, respectively. The transformer leakage inductance is designed as very small such that when S_1 and S_2 are turning ON/OFF, the transformer current reverses and reaches the opposite peak rapidly. From Fig. 13(a), the transformer current shape is quite “square” at high power, indicating a small peak-to-average ratio or low conduction losses.

The conversion efficiency of the boost-half-bridge main circuit is summarized in Fig. 14. It is measured based on the different input PV voltages and power levels. High efficiency (97.0%–98.2%) is achieved over the entire input voltage range (30–50 V) when the PV power is above 30% of the nominal value. The peak efficiency is measured as 95.6% at P_{PV} = 160 W and v_{PV} = 40 V when the full-bridge inverter is included.

B. Verification of the Plug-In Repetitive Current Controller

The steady-state grid voltage and current waveforms are depicted in Fig. 15. Both heavy load and light load conditions are tested to verify the current controller performance. As can be seen from Fig. 15(a), the proposed plug-in RC achieves a THD as low as 0.9% and a high power factor of 0.998 under heavy load. Low THD (2.87%) and high power factor (0.99) are still obtained even when the load is reduced by 2/3, as shown in Fig. 15(b).

Dynamic responses of the plug-in RC are verified by the experimental results in Fig. 16. Fig. 16(a) and (b) shows the results when the full-bridge inverter is tested independently. In Fig. 16(a) and (b), the grid current reference is step changed from 0.33 to 1 A and 1 to 0.33 A, respectively. The proportional part in the plug-in RC enables the controller to respond to the abrupt reference change promptly. Meanwhile, the RC part cancels the harmonic distortions in several fundamental cycles following the step change. Fig. 16(c) demonstrates the transient waveforms when the whole system is running and partial shading is suddenly applied to the PV module in order to generate an abrupt change of the input PV power. It can be observed that after the partial shading occurs, the LVS dc-link voltage is

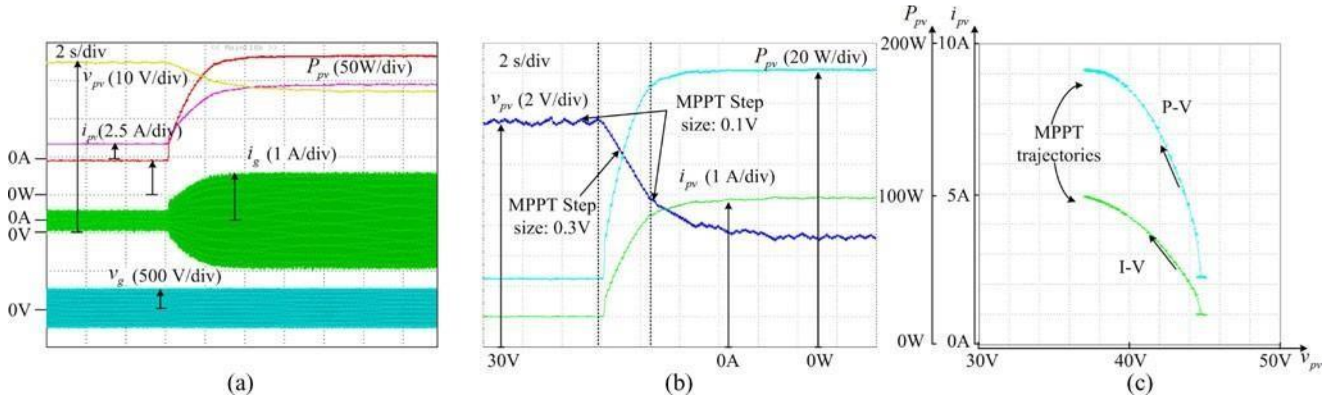


Fig. 17. MPPT of the PV microinverter system under solar irradiance change. (a) Input and output waveforms under solar irradiance change (partial shading to 880 W/m² at 50 ◦C). (b) Zoomed-in PV voltage, PV current, and PV power in (a). (c) MPPT trajectories (*P*–*V* and *I*–*V* curves).

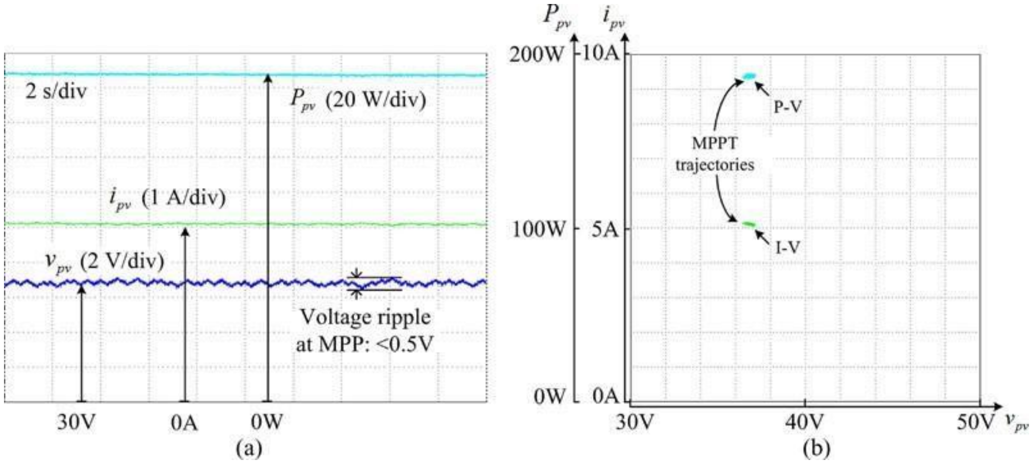


Fig. 18. MPPT of the PV microinverter system at the steady state. (a) PV voltage, PV current, and PV power (solar irradiance: 900 W/m² at 50 ◦C) (b) MPPT trajectories (*P*–*V* and *I*–*V* curves).

still regulated stiffly and the power injected to the grid precisely follows the input power trajectory.

C. Verification of the Variable Step-Size MPPT

As discussed in Section V, the variable step-size MPPT with ramp-changed PV voltage reference is implemented experimentally. Thanks to the ramp-changed PV voltage, the system is able to run correctly and reliably. The MPPT response under solar irradiance change (partial shading to 880 W/m²) is presented in Fig. 17. It can be seen that the MPPT employs a larger step size 0.3 V right after the solar irradiance changes to achieve fast tracking speed, and then shifts to a smaller step size 0.1 V for fine tracking. The steady-state performance of the MPPT is verified by Fig. 18. The PV voltage oscillates around the MPP within a very small range (0.5 V) at the steady state, providing an MPPT efficiency higher than 99.7%.

VII. CONCLUSION

A novel boost-half-bridge microinverter for grid-connected PV systems has been presented in this paper. A plug-in repetitive current controller was proposed and illustrated. The operation principles and dynamics of the boost-half-bridge dc–dc converter were analyzed and a customized MPPT control method was developed correspondingly. Simulation and experimental results of the 210 W prototype were shown to verify the circuit operation principles, current control, and MPPT method.

Thanks to the minimal use of semiconductor devices, circuit simplicity, and easy control, the boost-half-bridge PV microinverter possesses promising features of low cost and high reliability. According to the experimental results, high efficiency (97.0%–98.2%) is obtained with the boost-half-bridge dc–dc converter over a wide operation range. Moreover, the current injected to the grid is regulated precisely and stiffly. High power factor (>0.99) and low THD (0.9%–2.87%) are obtained under both heavy load and light load conditions. Finally, the customized MPPT method that generates a ramp-changed reference for the PV voltage regulation guarantees a correct and reliable operation of the PV microinverter system. The variable step-size technique provides a fast MPP tracking speed and a high MPPT efficiency (>99.7%). As a result, the proposed boost-half-bridge PV microinverter system with its advanced control implementations will be a competitive candidate for grid-connected PV applications.

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