Study of Low Power Operational Amplifier Using 22nm Technology

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Abstract- *The Operational Amplifier (OA) is the basic building block in any analog - mixed signal system. The architecture of the operational amplifier plays a vital role in designing low voltage, low power integrated circuits. The challenge lies in designing IC with reduced supply voltage and power to realize portable equipment with a minimum number of battery cells and a longer life period. This manuscript depicts the review of existing designs for low power two stage operational amplifier using miller compensation technique to increase the voltage gain. A comparative analysis is also shown in this paper.*

Keywords- OPAMP, Miller Compensation, Gain, Bandwidth.

I. INTRODUCTION

The operational amplifier is undeniably one of the most advantageous maneuvers in analog electronic circuitry. Op-amps are fabricated with massively dissimilar levels of intricacy to be used to grasp functions fluctuating from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the utmost broadly used electronic devices nowadays, being used in a vast array of customer, engineering, and technical devices. Operational Amplifiers, more frequently known as op-amps, are among the most extensively used edifice blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. [1, 2]

Op-amps are linear expedients which has closely all the belongings mandatory for not only ideal DC intensification but is used expansively for signal conditioning, filtering and for execution mathematical operations such as addition, subtraction, integration, differentiation etc. Generally an Operational Amplifier is a 3-terminal device. It contains chiefly of an Inverting input represented by a negative sign, ("-") and the other a Non-inverting input designated by a positive sign ("+") in the symbol for op-amp. Both these inputs have very high impedance. The output signal of an Operational Amplifier is the extravagant difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier [3].

A perfect operational amplifier having a single ended out is portrayed by a differential input, infinite voltage increase, interminable input resistance and zero output obstruction. In a genuine operational amplifier anyway, these characters can't be produced however their execution must be adequately useful for the circuit conduct to firmly rough the characters of a perfect operational amplifier in many applications. With the presentation of each new age of CMOS advancements structure of op-amp keeps on acting further difficulties like the supply voltages and transistor channel lengths downsize.

In this paper, three stage RC miller compensated op-amp is compared with another similar op-amp which uses double cascade telescopic input in the first stage and common source amplifier in the second stage. Also the load capacitor improves the phase margin of the Miller compensated op-amp.

II. LITERATURE REVIEW

Priyanka Kakoty et. al. [4], a technique is offered in this paper for the proposal of a high frequency CMOS operational amplifier (Op-Amp) which operates at 3V power supply using TSMC 0.18 micron CMOS technology. The Op-Amp designed is a two-stage CMOS Op-Amp trailed by an output buffer. This Operational Transconductance Amplifier (OTA) pays a Miller capacitor and is remunerated with a current buffer compensation technique. Design has been agreed out in Tanner tools. Simulation results are verified using S-edit and W-edit.

J. Mahattanakul [5], the intention technique of the two-stage CMOS operational amplifiers retaining Miller capacitor in combination with the common-gate current buffer is presented.

R. Chatterjee et. al. [6], in this manuscript a CMOS two stage operational amplifier has been discussed which operates at 2.5 V power supply at 0.18 micron (i.e., 180 nm) technology and whose input is be contingent on Bias Current.

The supply voltage has been scaled down to reduce overall power depletion of the system.

N Sachdeva et. al. [7], with the incessant emergent development towards the condensed supply voltage and transistor channel length, designing of high performance analog integrated circuits such as operational amplifier in CMOS (complementary metal oxide semiconductor) technology develops more perilous. In this research, the two stage CMOS Operational amplifier (op-amp) has been deliberate using miller compensation technique which operates at 2.5V.

D. J. Moni et. al. [8], in this script a two stage RC Miller compensated op-amp and its investigation is shown. In order to get a high dc gain, a two stage op-amp is castoff. The two stage op-amp contains of a magnifying op-amp in the first stage and a conjoint source output rail-to-rail stage in the second stage. In adding to the dc gain, the main benefit of this op-amp is the voltage swing.

K A Shah et. al. [9], the tendency to low voltage low power silicon chip schemes has been rising rapidly due to the cumulative plea of smaller size and longer battery life for portable submissions in all marketing segments. The supply voltage is being scaled down to decrease overall power consumption of the system.

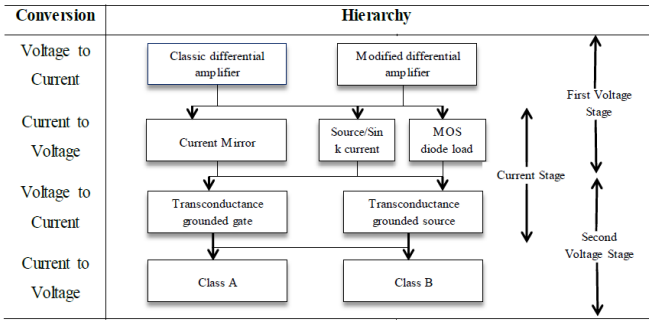
Manash Pratim Sarma et. al. [10], this tabloid accounts a novel design of a short power two stage operational amplifier with Miller compensated topology for improving constancy. The circuit is premeditated and replicated in Tanner EDA tool using 45 nm CMOS technology. A momentous reduction in power and improvement of unity gain BW is attained with a satisfactory phase margin

On the basis of above research paper, we can conclude the literature review is as follows:

Parameters	[4]	[5]	[6]	[7]	[8]	[9]	[10]
Tech (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.045
V_{dd} (V)	3	2.5	2.5	1.1	1.8	1.8	1
DC Gain (dB)	49	81	36.7	48.27	60	55.5	49.15
Phase Margin (degree)	60	65	48.1	86.4	50	60	60.4
Power (µW)	396	378	804	-	1.03m	300	70
Unity Gain (MHz)	477	5	16.5	11.2	26.02	12.6	533.1

In order to understand the design of CMOS op amps it is worthwhile to examine their classification and categorization. Table 1 explains the classification in detail [11].

Table 1: Categorization of CMOS Op Amps



III. DESIGN SPECIFICATION

The full op-amp schematic designed using the previous designed current mirror and differential amplifiers and the common source amplifier circuit is as shown in figure 1 below:

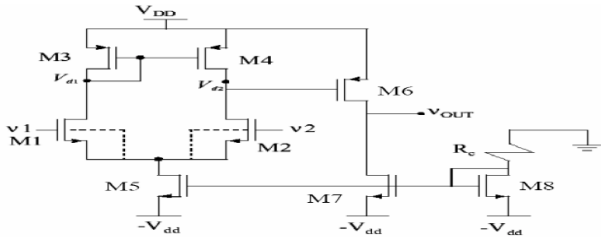


Figure 1: Block diagram for practical operational amplifier

The designing of op amps can be separated into two different design-related activities that are for the most sovereign of one another. The first of these actions involves selecting or crafting the basic structure of the op amps. Once the structure has been nominated, the designer must select dc currents and commence to size the transistors and design the compensation circuit. Most of the work tangled in completing the design is associated with this second work.

Typical Specification	Design Factors
DC Gain (Av)	Frequency Response
Unity Gain Bandwidth	Phase Margin
Power Dissipation	Load Capacitance
Slew Rate	Compensation
Input Offset Voltage	Device Dimensions
Output Voltage Swing	
CMRR	

Specifications	
Open loop Gain	40 dB
Gain B/W at -3 db gain	5 MHz
Load Capacitance (CL)	10 pf
Slew Rate	10 V/Us
Mirror Pole kept at	>=10GB
Maximum Power Dissipation	≤ 2mw
Phase Margin	>=60
Channel Length	22 nm
CMRR	>=60 dB
PSRR	>=60 dB
Power Supply	0.8 Volt

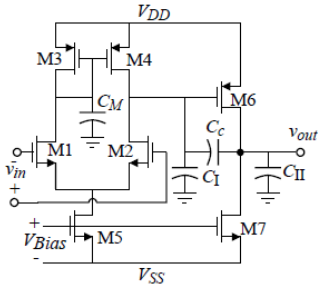


Figure 3: Miller compensated two stage op amp

IV. COMPENSATION TECHNIQUE

Operational amplifiers are generally used in a negative feedback configuration. In this way the relatively high, inaccurate forward gain can be used with feedback to achieve a very accurate transfer function that is a function of the feedback elements only [11]. To achieve the stable operation of op amps, compensation techniques are used. There are three types of compensation techniques, which are discussed as follows:

1. Miller Compensation - Usage of a capacitor feeding back around a high-gain, inverting stage.
    a. Miller capacitor only
    b. Miller capacitor with a unity-gain buffer to block the forward path through the compensation capacitor. It can eliminate the RHP zero.
    c. Miller with a nulling resistor. Analogous to miller but with an additional series resistance to gain control over the RHP zero.
2. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.
3. Self-Compensating - Load capacitor compensates the op amp.

V. CONCLUSIONS

Here, we have reported the review of a low power op-amp topology. On the basis of above literatures low power operational amplifier can be implemented using 45 nm technology or below this technology like 25 nm, 22 nm etc. We can reduce the power supply voltage for the operational amplifier or use of 4 terminal CMOS can reduce the power. According to the above manuscript, the proposed design will be implemented using Tanner EDA tool.

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