Vhdl Implementation of PID Controller on Fpga

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Abstract- *PID stands for proportional, integral derivative. It is commonly employed in process control industries for controlling various process variables such as pressure, temperature, level, flow etc It is a feedback controller to generate an output that causes some corrective effort to be applied to a process to derive a measureable process variable towards a desired value known as the set point. The techniques to be adopted for determining the proportional, integral and derivative constants of the controller depends upon the dynamic response of the plant .*

The various elements used in PID controller are set point, Plant, sensor, error signal. Plant is the physical heating and cooling part of the system. Set point is the process variable which is to be controlled .Error signal is the difference between the response of the plant and the desired response (set point). Sensor senses the variable within the plant. Controller can be tuned using various methods. One of the methods is using Zigler Nichols method.

IN FPGA based temperature control. Initially, the digital design (block diagram) will be drafted showing the basic functioning of the hardware in terms of the blocks. This will then be coded in a hardware description language (VHDL). The functioning of the coded design is to be simulated on a simulation software (e.g. ISim). After proper simulation, the design is to be synthesized and then translated to a structural architecture in terms of the components on the target FPGA device (Spartan 3s200ft256) and the perform the post-translate simulation in order to ensure the proper functioning of the design after translation. After the successful simulation of the post-translate model the design is mapped to the existing slices of the FPGA and the post-map model simulated. The post-map model doesn't include the routing delays. After the successful completion of the post-map simulation, the design is then routed and a post-route simulation model with the appropriate routing delays is generated to be simulated on the HDL simulator. After this a programming file is generated to program the FPGA device. The objective is to run the programmed FPGA at a frequency as high as possible. The working of the device is to be demonstrated by making an appropriate testing hardware.

I. INTRODUCTION

PID stands for proportional, integral derivative. It is commonly employed in process control industries for controlling various process variables such as pressure, temperature, level, flow etc. It is a feedback controller to generate an output that causes some corrective effort to be applied to a process to derive a measureable process variable towards a desired value known as the set point. The techniques to be adopted for determining the proportional, integral and derivative constants of the controller depend upon the dynamic response of the plant.

The various elements used in PID controller are set point, Plant, sensor, error signal. Plant is the physical heating and cooling part of the system. Set point is the process variable which is to be controlled .Error signal is the difference between the response of the plant and the desired response (set point). Sensor senses the variable within the plant. Controller can be tuned using various methods. One of the methods is using Zigler Nichols method. It is first assumed that controller has only proportional gain term; we then proceed to determine the critical gain for the closed loop system to just get continuous oscillations. The corresponding period of oscillation is determined, knowing these two values; the PID controller can be tuned. Comparator compares the set temperature value and output response value and generate an error .Depending upon this error controller will adjust the vale of proportional gain, derivative gain and integral gain to generate an output signal using an mathematical equation which is applied to the plant.

PID controllers are process controllers with the following characteristics:

- Continuous process control
- Analog input (also known as "measurement" or "Process Variable" or "PV")
- Analog output (referred to simply as "output")
- Setpoint (SP)
- Proportional (P), Integral (I), and / or Derivative (D) constants

II. OBJECTIVE AND FEATURES OF PID CONTROLLER

The objective of the thesis work is to design PID controller for temperature control using FPGA.

IN FPGA based temperature control. Initially, the digital design (block diagram) will be drafted showing the basic functioning of the hardware in terms of the blocks. This will then be coded in a hardware description language (VHDL). The functioning of the coded design is to be simulated on a simulation software (e.g. ISim). After proper simulation, the design is to be synthesized and then translated to a structural architecture in terms of the components on the target FPGA device (Spartan 3s200ft256) and the perform the post-translate simulation in order to ensure the proper functioning of the design after translation. After the successful simulation of the post-translate model the design is mapped to the existing slices of the FPGA and the post-map model simulated. The post-map model doesn't include the routing delays. After the successful completion of the post-map simulation, the design is then routed and a post-route simulation model with the appropriate routing delays is generated to be simulated on the HDL simulator. After this a programming file is generated to program the FPGA device. The objective is to run the programmed FPGA at a frequency as high as possible. The working of the device is to be demonstrated by making an appropriate testing hardware.

Features:

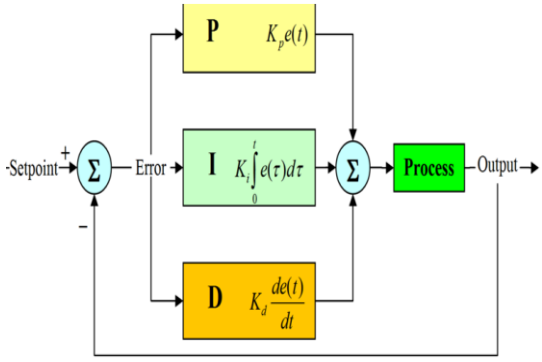
The features of the PID controller which is to be implemented are finalized as specified below:

- PID will control the temperature from ambient to 100 ^{0}C
- We can control the temperature with an accuracy of less than± 1^{0}C
- Cycle time is between 1 second to 66 minutes
- The operation is on the 50 MHZ clock rate

III. PID CONTROLLER

History & Architectures:

- The proportional integral derivative (PID) controllers have been the most commonly used controllers in process industries for over 50 years even though significant development has been made in advanced control theory. According to survey conducted by Japan electric measuring instrument manufacturer association in 1989. 90% of the control loops in industries are of the PID type. These useful functions are sufficient for large number of process applications and the transparency of features lead to the wide acceptance of the users. A strength of the PID controller is that it also deals with the important practical issues such as actuator saturation and integrator windup.PID controllers performs well for a wide class of processes and they give robust performance for a wide range of operating conditions and they are easy to implement using analog and digital hardware. Moreover due to process uncertainties a more sophisticated control scheme is not necessarily more efficient than a well tuned PID controller
- A large industrial process may have hundreds of PID controllers. Proper tuning of the controllers is crucial for achieving the desired response characteristics. They have to be tuned individually to match the process dynamics in order to provide good and robust control performance. The tuning procedure if done manually is very time consuming; the resultant system performance mainly depends upon the experience and process knowledge of the engineers. It is recognized that in practice many industrial control loops are poorly tuned. However with the advent of the auto tuning of PID controller concept, this problem has been solved to the considerable extent.
- .Automatic tuning technique thus draws more and more attention of the researchers and practicing engineers. By automatic tuning we mean a method which enables the controller to be tuned automatically on demand from a operator or external signal. Typically, the user will either push a button or send a command to the controller. Industrial experience has clearly indicated that this is highly desirable and useful feature.



Action of PID controller. [12]

- The main elements used in PID controller are set point, plant, sensor, error signal.
- **Plant**:- The physical heating and cooling parts of the system. Depending upon the output error of the PID controller, heater will be on or off.
- **Sensor**:-The device that measures the variables within the plant. Sensor will sense the temperature of the heater.

- **Set Point**:-Set point is the fixed value of temperature that we want to control. Depending upon the analog value of temperature ADC will control this temperature into digital format.
- **Error Signal**:-This is the difference between the response of the plant and the desired response (set point).This error signal generated will be applied to the PID calculation block. Depending upon the value of the error PID calculation block will take decision.
- **Disturbances**:-These are the unwanted inputs to the plant ,which can be common. The disturbance would be an open entry door allowing aguest of cold air to blow in, guickly droping the temperature and causing the heat to come on.
- **Controller** :-This is the most significant element of the control system. The controller is responsible for several tasks.It measures the signal of the plant sensor, processes the signal and then drives an error based on the signal measurement and the set point.Once the sensor data has been collected and processed, the result must be used to find PID values, which then must be sent out to the Plant for error correction.

Tuning of PID controller:

- Tuning" a control loop is the adjustment of its control parameters (gain/proportional band, integral gain/reset, derivative gain/rate) to the optimum values for the desired control response. The optimum behavior on a process change or setpoint change varies depending on the application. Some processes must not allow an overshoot of the process variable from the setpoint. Other processes must minimize the energy expended in reaching a new setpoint. Generally stability of response is required and the process must not oscillate for any combination of process conditions and setpoints. Tuning of loops is made more complicated by the response time of the process; it may take minutes or hours for a setpoint change to produce a stable effect. Some processes have a degree of non-linearity and so parameters that work well at full-load conditions don't work when the process is starting up from no-load. This section describes some traditional manual methods for loop tuning.

IV. XILINX ISE DESIGN SUITE

History

- In this modern era, **Xilinx ISE** (**I**ntegrated **S**yndissertation **E**nvironment) is a very imperative software tool created by **Xilinx** which provides various functions such as for blend and scrutiny of HDL designs, helps in permitting the designer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to diverse stimuli and also establish the objective method with the programmer. **Xilinx** is a technology developed by an American company, mainly a purveyor of programmable logic devices. This technology is also known for originating the field programmable gate array (FPGA) and be the first semiconductor company with a fables built-up model.
- In 1984, Silicon Valley is one of the company which is headquartered in San Jose, California to establish this technology, with additional offices in Longmont, Colorado; Dublin, Ireland; Singapore; Hyderabad, India; Beijing, China; Shanghai, China; Brisbane, Australia and Tokyo, Japan. The one of the foremost FPGA product
- families includes Virtex (high-performance), Kintex (mid-range) and Artix (low-cost), and the retired Spartan (low-cost) series and it also includes chief computer software such as Xilinx ISE and Vivado Design Suite[30][33].

V. VHDL SIMULATION RESULTS

5.1 VHDL Model for controlling temperature of electric bulb:

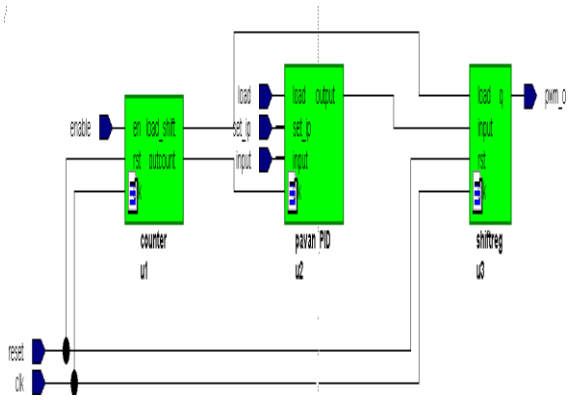


Fig 5.1 Block diagram of VHDL model

Block diagram for VHDL model is shown as above.There are three blocks known as PID block, counter block and shift register block.Shift register shifts 8 bits one by one in 8 clock cycles.In the 9 th clock cycle when the value of load is high, then the new value will be loaded.Again shift register will shift 8 bits one by one from MSB to LSB and in the 9 th clock new data will be loaded.Conter will increament one by one.Shift register output is 8 bit PWM that will goes to the relay.Now Relay will be on only once in a cycle.This PWM will goes to the bulb.Now a LM 35 temperature is used.This temperature sensor will sense the temperature of the bulb in Analog form.So we have to convert this into digital form.So for this we use ADC 0804.ADC0804 convert analog value of temperature into digital 8 bit value.This 8 bit scan

value will go to the FPGA .Now FPGA will copare the scan value and the set value of temperature. If the scan value of temperature is more than the scan value then 8 bit PWM value will decrease. and if the scan value of temperature is less than the scan value then 8 bit PWM value will increase .This process is repeated again and again till we get the eqact value of temperature. Means scan value and set value are equal.

Design and implementation of PWM block:

Set Input: when load equal 1 then temperature set by the user is stored at set signal.when load equals 0 then if set value is greater than input then difference is between set value and input is stored at dif signal and when input is greater than set value then difference between input and set value is stored in variable

Code Implementation

```
if (load='1') then
set<=set_ip;
elsif load='0' then
if clk'event and clk='1' then
if set > input then
gt<='0';
dif<=set-input ;
else
gt<='1';
dif<=input-set;
end if;
end if;
end if;
diff<=dif;
```

when signal gt=’0’ then if difference of set value and scan value is more than or equal to 8then PWM value is 11111111.This means PWM is of full duty cycle.If temperature difference is 7 then PWM on time decreases and Value of PWM is11111110.In this case on time of PWM is 7/8 means87.5%.Similarly if the temperature difference is 7, then PWM again decreases and its value is 11111100.On time of this PWM is 75% and off ime is 25%..In the end when temperature difference is zero than PWM value is 00000000.This means On time is almost zero.

Code Implementation

```
if gt='0' then
case diff is
when "00001000"  => output<="11111111";
when "00000111"  => output<="11111110";
when "00000110"  => output<="11111100";
when "00000101"  => output<="11111000";
when "00000100"  => output<="11110000";
when "00000011"  => output<="11100000";
when "00000010"  => output<="11000000";
when "00000001"  => output<="10000000";
when "00000000"  => output<="00000000";
when others => output<="11111111";
end case ;
```

When signal gt =’1’ then if difference of scan value and set value is 8 or more than 8, then PWM is fully on.If temperature difference between scan value and set value is 7 then value of PWM is 00000001.This means on time of PWM is 12.5% and off time is 87.5%.If the temperature difference between scan value and set value is 6 then value of PWM is 00000011.This means on time of PWM is 25% and off time is 75%.Similarly we can calculate the vale of PWM as the difference of temperature between the scan value and set temperature value decreases

Code Implementation of PWM block:

```
if gt=’1' then
case diff is
when "00001000"  => output<="00000000";
when "00000111"   => output<="00000001";
when "00000110"  => output<="00000011";
when "00000101"  => output<="00000111";
when "00000100"  => output<="00001111";
when "00000011"  => output<="00011111";
when "00000010"  => output<="00111111";
when "00000001"  => output<="01111111";
when "00000000"  => output<="11111111";
when others => output<="00000000";
end case ;
 end if;
```

Flow chart for PWM generation Block:

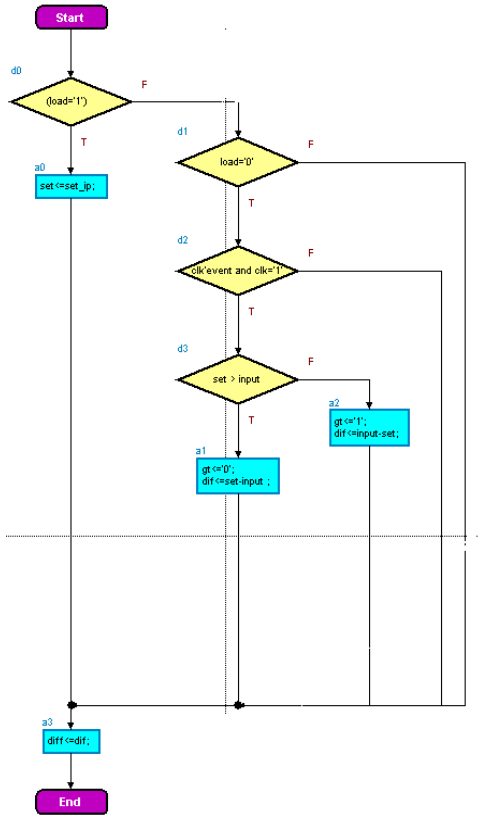


Fig 5.2 Flow Chart for PWM generation Block

Design and implementation of Shift Register Block:

If the value of reset is 1 then temp register stores the value"00000000".Now if the value of load is 1, then value of scan input should stored in the scan register.When load value is zero then shift register will shift one by one bit from MSB to LSB.In 8 clock cycles all 8 bits are shifted.Now in the 9 th clock cycle value of load is set to 1 and new input value is stored in the temp register.This process is repeated again and again

5.3.1 Code Implementation of shift register block:

```
if rst='1' then
 temp<="00000000";
 elsif load='1' then
 temp<=input;
 else
 if clk'event and clk='1' then
 q<=temp(7);
 temp(7)<=temp(6);
 temp(6)<=temp(5);
 temp(5)<=temp(4);
 temp(4)<=temp(3);
 temp(3)<=temp(2);
 temp(2)<=temp(1);
 temp(1)<=temp(0);
temp(0)<= '0';
 end if;
 end if;
```

5.3.2 Flow Chart For Shift Register Block:

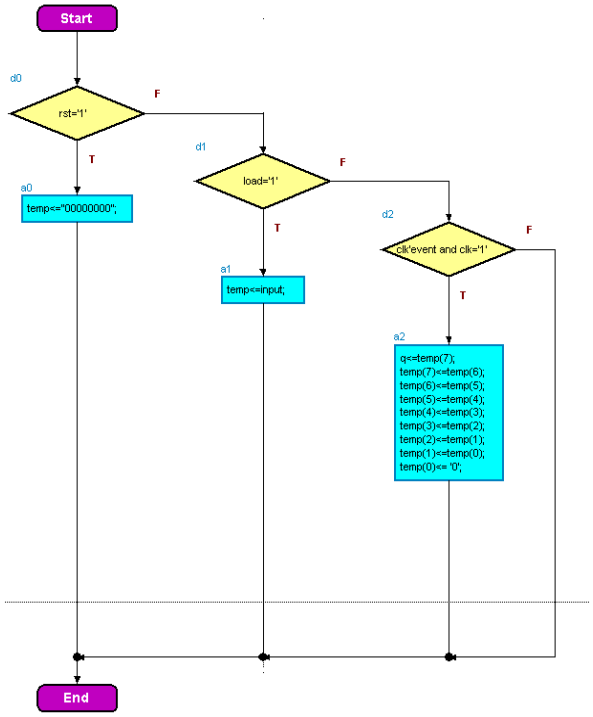


Fig 5.3 Flow Chart for Shift Register Block

Design and implementation of Counter block:

When the value of reset is 1 then count is" 0000" and signal s(which goes to shift register and high at every 9 th clock cycle).Now when en is equal to 1 then count is incremented at each clock cycle.After completing 8 clock cycles the signal s will change from 0 to 1 means low to high.This means when signal s value will change from low to high then new value of scan value will be loaded in the temp register.

5.4.1 Code implementation

```
if (rst='1')then
s<='0';
dummy<=(others=>'0');
load_shift<='0';
elsif(en='1')then
if(clk'event and clk='1' )then
dummy<=dummy +"0001";
if(dummy="1000")then
s<=not s;
load_shift<='1';
```

```
dummy<="0000";
else
 load_shift<='0';
 end if;
 end if;
end if;
```

5.4.2 Flow Chart for Counter block:

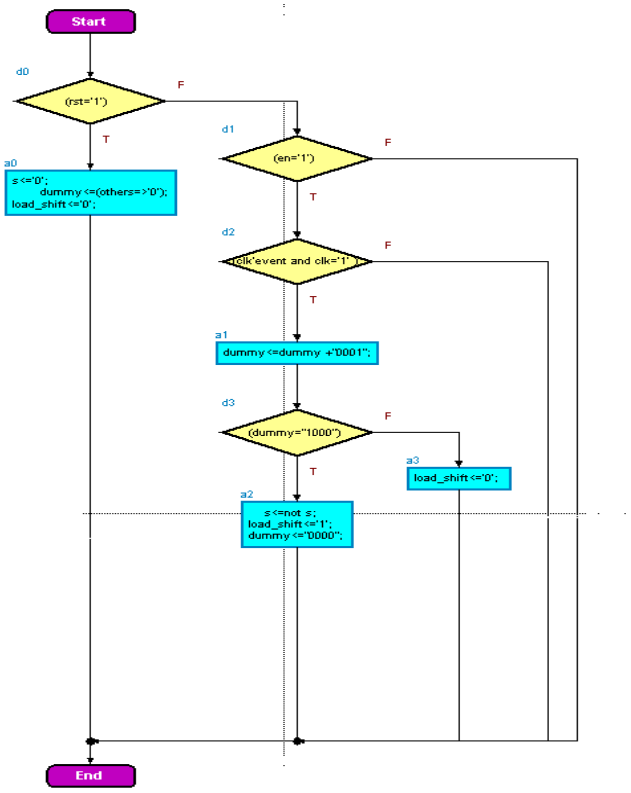


Fig 5.4 Flow Chart for Shift Register Block

5.5 RTL View of PID Controller:

RTL View of the combined block is given as

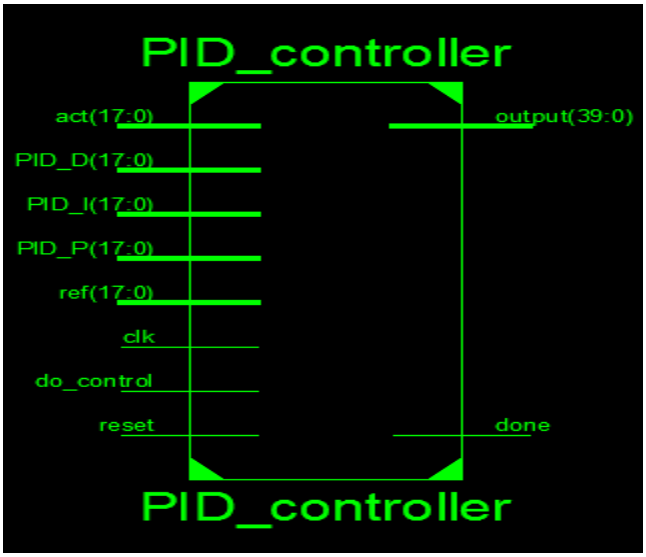


Fig: 5.5 RTL Block of PID Controller

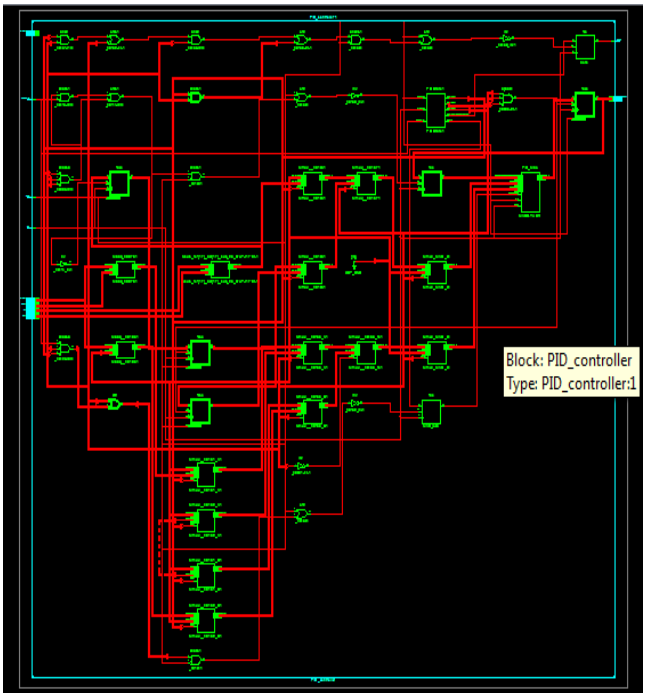


Fig:5.6 **RTL View of PID Controller**

5.6 VHDL based Simulation Results:

5.6.1 Combined Block Simulation Result

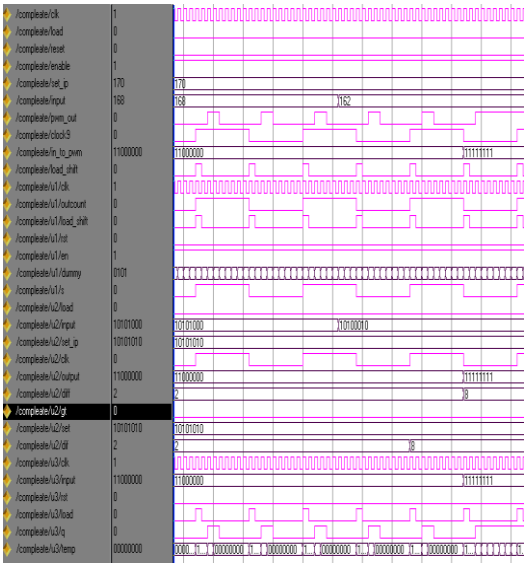


Fig 5.7 : Simulation block of combined block

Load: This signal decides whether we have to load a new value or for shifting operation.When the value of this signal is '1', then we are loading new value of set temperature and when its value is '0' , then we are doing shifting operation

Reset: This signal is used for resetting initial values

Enable: This signal is used for the proper operation of shift register

PWM_output: This output signal will decide the on or off time of the bulb depending upon the 8 bit of PWM.

5.8 Simulation Result of Diffrence block:

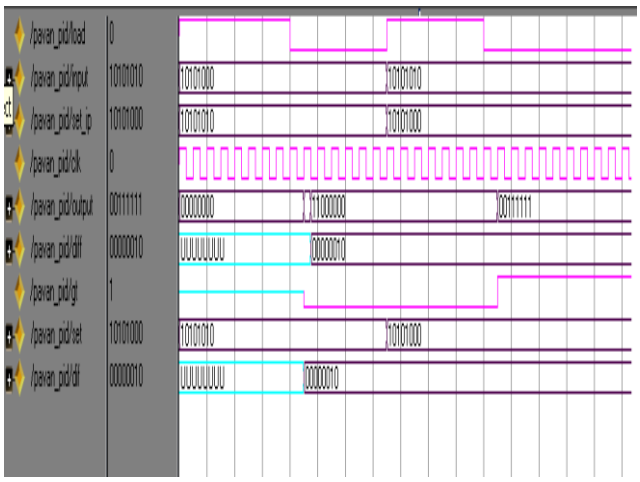


Fig 5.8: Simulation Result Of Diffrence block

Gt: This signal will decide whether set value of temperature is more than scan value or less .If gt is '0' this means set value of temperature is more than scan value.If the value of gt is '1' , this means scan value is more than set value.

PID_SET: This is the value of temperature that we want to control.It is set by the user.

PID_INPUT: This is the scan value of temperature that comes from ADC

5.9 Simulation Result of Shift Register:

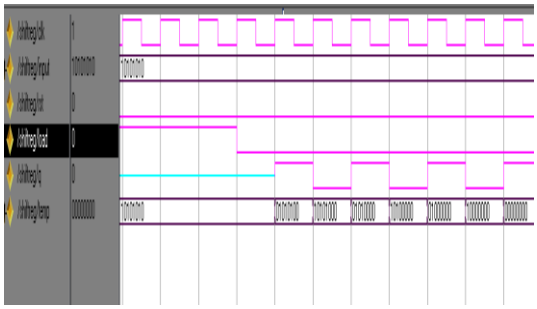


Fig4.4 : Simulation Result Of Shift register

Load: This signal decides whether we have to load a new value or for shifting operation.When the value of this signal is '1', then we are loading new value of set temperature and when its value is '0' , then we are doing shifting operation

Simulation Result of Counter:

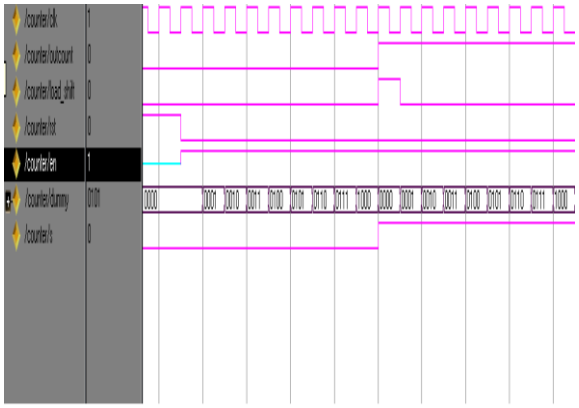


Fig4.5 : Simulation Result Of Counter

Outcount: It is clock for loading input values

Load_shift: when load_shift is low, thenbits of PWM are shifting one by one.When its value is high, then new new value of set input input is loaded.

En: this signal is used for enabling the counter

VI. CONCLUSION

A VHDL model is developed for controlling the temperature of the bulb. Although Temperature controller system has been developed in this work, but more features can be added to increase its utility. There are several modifications, both to the hardware and software which may improve the system performance. The present-day structure of PID controllers is quite different from the original analog PID

controllers. Now the implementation of the PID is based on digital design, these digital PIDs include many algorithms such as anti-wind-up, auto-tuning, adaptive, and fuzzy fine tuning to improve their performances, but the basic actions remain the same.

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