A Review on High-Frequency Compensation Using Text Fixture

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Abstract- *In power electronics applications one of the challenges at high-frequency passive components is the presence of parasitic components present at high-frequency which effect the measurement of an LCR meter. Thus a new test fixture with less stray capacitance and inductance has been developed for compensating these parasitic components at high-frequency. Compensation is used to enhance the calibration range of the LCR meters using the new text fixture.*

I. INTRODUCTION

Several challenges are present in characterizing the passive components in any power electronic applications. In many applications impedance analyzers can be used to characterize resistors, capacitors, inductors and transformers, but they have their limitations which can be problematic for power components. Still they are most convenient to characterize a component; also high accuracy can be achieved more often.

Impedance analyzers using four-terminal (4T) or four-terminal-pair (4TP) connections for connecting device under test (DUT) can accurately measure much lower impedances. However, the parasitic components present in the test fixture can becomes a severe problem for present and future microprocessor power delivery circuits as the impedances required is very low.

1.1 Parasitic components

Generally the values of L, C and R components are represented by the nominal values of capacitance, inductance or resistance at specific or standard conditions. But all the components in a circuit are neither purely resistive nor purely reactive. Parasitic components are always present in all real-world devices like unwanted inductance in resistors, unwanted resistance in capacitors, unwanted capacitance in inductors, etc.

Parasitic are also present due to different types of materials used in manufacturing and due to different manufacturing technologies. These parasitic reside in components, thus affecting the components usefulness and accuracy. These parasitic components combined with primary elements, makes a component looks like a complex circuit as show in below figure 1.

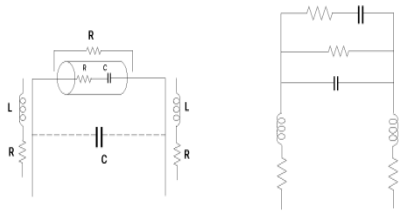

Figure 1: Component (capacitor) with parasitic represented by an electrical equivalent circuit [13]

A. Parasitic Capacitance:

Parasitic capacitance or stray capacitance is unwanted and unavoidable capacitance. It exists because of the close proximity of the parts of the electronic component or circuit to each other. When in any electrical circuit two electrical conductors at different voltages are close to each other, an electric field is generated between them, because of this electric field electric charge are stared to store on the conductors and the conductors stared to act like an capacitor, this effect is parasitic capacitance.

All circuit elements such as inductors, diodes, transistors etc. have internal capacitance, because of which they behave differently from there 'ideal' circuit elements behavior. Also there is always a non-zero capacitance between any two conductors; which can be significant at higher frequency with very closely spaced conductors like wires or printed circuit board traces.

B. Parasitic Inductance:

Parasitic inductance or stray inductance is unwanted and un-intended inductance in a circuit. Inductance does not exists within the inductors only, any wire or component leads that have current passing through them creates magnetic field, when this magnetic field is created it produce the inductive effect, making the wire or component lead to act as an

inductor, if they are long enough. Such effects are mostly present inside the circuit (like, between wire traces or components with long leads such as capacitor), even though it was not intended. This unintended inductance is referred as stray inductance or parasitic inductance and it can disturb the normal current flow in the circuit.

The circuit designers are trying to minimize stray inductance as much as possible. It can be done by keeping the leads of electronic components very short and grouping components in such a way that it reduces capacitive coupling.

1.2 Four-Terminal-Pair Configuration

In this paper we are using four-terminal-pair (4TP) auto-balancing bridge system [11], as shown in figure 2. This system minimizes the effect of stray impedance in the interconnections. Voltage across the DUT is measured at the high-potential (H_p) terminal pair with respect to a virtual ground maintained by the low-potential (L_p) terminal pair by feedback control of a second source at the low-current terminal pair. Signal is applied at the high-current terminal pair. The analyzer can compute complex impedance from the magnitude and phase of the measure voltage and current.

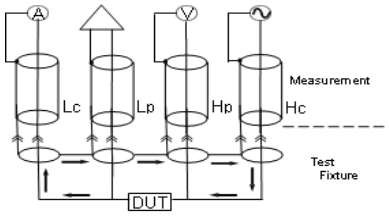

Figure 2: Schematic of the Auto Balancing Bridge Measurement [11]

II. FREQUENCY COMPENSATION

Frequency compensation is mostly used in amplifiers especially negative feedback amplifiers. Frequency compensation is mostly used to avoid the unintentional creation of positive feedback, due to which an amplifier oscillate and to control overshoot and ringing in the step response of an amplifier. It also improves the bandwidth of single pole systems. Frequency compensation is used in this paper to improve the calibration range of LCR meter.

2.1 Dominant- Pole Compensation:

The most commonly used method for frequency compensation is the dominant-pole compensation method. Dominant-pole compensation is also a type of lag compensation. In this method a dominant pole is from a low frequency pole by adjusting a low frequency pole such that the other higher poles are made very far from the dominant pole, thus the transfer function (gain Vs frequency curve) crosses the 0dB line between the dominant pole and the other poles. Mainly, the lowest frequency pole is made as the dominate pole, so that it can dominates the effect of higher frequency pole and thus reduces the phase margin. It helps in making open loop output phase and closed loop phase response of the feedback network, maintaining constant gain and do not falls below 1800. Trans-conductance operational amplifiers (OTA) use dominant-pole compensation method. it added a capacitor in between the gain stages of the OTA, which introduces a pole adjusted to low frequency such that the gain Vs frequency curve cross 0dB just after the low frequency is made a dominant. Depending upon the location of next higher poles, it results approximate 45° of the phase margin. In commonly used feedback systems, this phase margin is used to control the oscillation to be happened in the amplifier.

The dominant pole compensation has advantage such as:

a. It controls the overshoot and ringing of the amplifiers when we apply to step input.
b. It improves the noise immunity as the noise frequency components outside the bandwidth are eliminated.
c. It is simple and effective.

But dominant-pole compensation also has two drawbacks:

a. As it reduces the amplifier's bandwidth, it also reduces the available open loop gain at higher frequency. Thus, reducing the feedback available at higher frequency in turns.
b. It also reduces the slew rate of the amplifiers. This reduction in slew rate is the result because of the time it takes to drive current from the compensation stage to charge the compensating capacitor. This shows the inability of the amplifier to reproduce high amplitude, at rapidly changing signals accurately.

Often when we implement dominant-pole compensation it results in pole-splitting. Because of the pole-splitting the lowest frequency pole of an uncompensated amplifier moves to an even lower frequency and becomes the dominant-pole, while the higher- frequency pole moves to an even higher frequency. This drawback can be overcome by using pole-zero compensation.

2.2 Pole splitting compensation;

A. Single capacitor miller compensation:

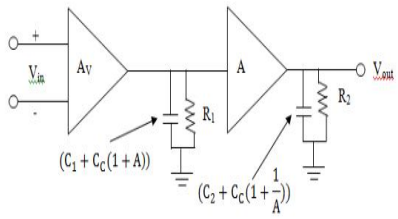

Figure 3: two stage op-amp with single capacitor miller compensation [9]

Single capacitor miller compensation reduces the frequency of the dominant pole and moves the outer poles away from the origin. This effect is known as pole-splitting. In this compensation method, the compensating capacitor is connected in the second stage. According to the Miller theorem, impedance parallel with the gain stage can be treated as the impedance connected from the input of the gain stage to the ground and as the impedance connected from the output of the gain stage to the ground. This impedance is purely capacitive. Also before the implementation of the pole-splitting, the second stage has inverting gain. The frequency of the first stage reduces, thus phase margin of the op-amp improves, in turns making the op-amp more stable after compensation. While designing the cascaded amplifier with miller compensation it should be kept in mind that zeroes has to be quite far from the origin. It is because there is more phase shifting as poles are in left half of the plane and zeros are in right half of the plane. Two different approaches can be used to eliminate the effects of the zeros in right half plane: the first approach is to insert a source follower in the path between the output and the compensating capacitor. And the second approach is to insert a null resistor in series with the compensating capacitor.

The first and second stage pole frequencies before the implementation of the pole-splitting compensation methods are:

$$\omega_1 = \frac{1}{R_1 C_1} \text{ and } \omega_2 = \frac{1}{R_2 C_2}$$

And the pole frequencies after compensation are:

$$\omega_1 = \frac{1}{R_1(C_1 + C_C(1+A))} \text{ and } \omega_2 = \frac{1}{R_2(C_2 + C_C(1+\frac{1}{A}))}$$

Where R_1 and C_1 are the output resistance and capacitance of the first stage and R_2 and C_2 are he output resistance and capacitance of the second stage.

A. *Single capacitor miller compensation with null resistor*:

To cancel the first non-dominant pole we can move zero. This can be possible if the null resistor vale is selected such that the frequency of the zero and the first non-dominant pole becomes same. Thus to remove the right-half plane zero, we have to used miller capacitor with null resistor in series with the amplifier. The equation of the zero becomes

$$Z_1 = \frac{1}{C_C(\frac{1}{g_{m6}} - R_M)}$$

The zero moves to infinity if the value of the miller resistor R_M becomes equal to the $1/g_{m6}$. But if the value of R_M becomes more that $1/g_{m6}$, then the RP zero mover to the LHP, this can improve the phase margin and increase the stability.

III. TEST FIXTURE

To connect the device under test (DUT) to an impedance analyzer or to any system test fixtures are used. Typically the DUT uses the four-terminal-pair (4TP) configuration with the auto- balancing technique, as shown in figure 2. As the technology is advancing it becoming difficult to develop high performance high-current power system for microprocessor power delivery, thus commercially available test fixtures can't be used for measuring very low impedances at high frequencies extending into the MHz range.

The four-terminal-pair (4TP) configuration is used because it is more effective to prevent the stray impedances of the cables, mostly includes series inductance and resistances and shunt capacitance, which effect the impedance measurement [12]. But, the stray impedances in the close proximity of the DUT still remain. For instant, the resistance of the ground path adjacent to the DUT appears as the part of the measurement [8].This resistance is mostly neglected for both low-impedance and high-impedance devices, but it introduces inductances in the current loop containing the DUT and the adjacent ground path. This inductance loop is considered as a defect in the design of the 4TP systems. But, this inductive impedance is not defined other than for a loop[13]. Thus, for any impedance measurement, introduction of the inductance in a current loop through the DUT and returning through ground path becomes a fundamental requirement. Thus it become necessary for the users and designers of the test fixture to become aware of the current loop, to make sure that the measurement for the application is appropriate.

The return path for the modern high-performance circuit applications, which have mostly surface-mount devices, is a ground plane immediately below the device. There can be more return paths which also introduces the

inductance. These inductance can be considered that the as the board inductance rather than the device inductance. The vertical distance between the ground plane and the device also cause the loop inductance. Thus, the inductive impedance of a component mount on the surface is considered as the inductance of the loop containing the current path through the device and the return path in a plane.

Presently the surface-mount devices available for commercial text fixtures have the return path at a 5 to 10mm distance away from the device. These cause two problems to arise. Firstly, the inductance is in the range of 100nH for the loop where fixture is shorted. Based on the open-circuit and short-circuit measurements impedance analyzer can compensate test-fixture stray impedances. But, if we try to compensate for stray impedance whose value is much larger than the DUT impedance can result in poor resolution and accuracy. Secondly, ground return path affects the current distribution in the DUT, thus establishing the boundary conditions that determine the electromagnetic phenomena occurring in the DUT. To minimize stray inductance in an actual application, the return path should be close to the DUT, thus it become necessary to represent this configuration in the test. This is important as it reduce the errors that arise from fixture loop impedance which is can be equal to the DUT or much larger impedance, and to established proper boundary conditions to make the behavior of the DUT to match with the in-circuit behavior.

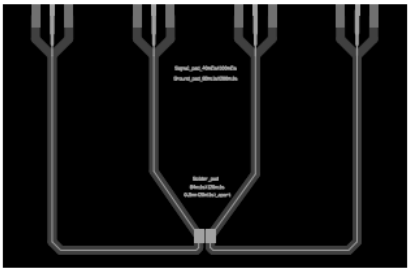

Figure 4: Layout of the text fixture designed for low stray impedance

Coaxial test fixtures which are introduced recently, reduces the stray inductance of the current loop, but for most of the applications they established the boundary conditions which are very different from the boundary conditions in the applications. It provides repeatable results, but not the results that are required for a typical application.

Some high-frequency test fixtures can achieve low stray inductance and realistic boundary conditions as they place the component directly on the top of a ground plane. But all such fixtures are commercially available uses two-point contacts to the DUT and thus introduce series resistance which can be very large as compared to the DUT resistance. Also each time a DUT is places in the fixture the resistance varies, its means that compensation based on a short-circuit measurement does not solve the problem. The commercial four-point contact fixtures have the drawback of the high stray inductance and unrealistic boundary conditions, as these fixtures use large return-path spacing.

Two-point solder connections to the DUT is been used, even through the resistance at solder-joints appears in the measurement and reduces precision, the solder connection has lower resistance and better repeatability, and also it is a realistic model of how the components should be used.

The 4TP interface of the analyzer is maintained till the traces reached the solder pads of the DUT, this minimize the portion of the stray impedance appearing in the measurement. This helps the impedance analyzer to work properly above 20MHz [12]. The text fixture helps in testing and calibrating based on the short-circuit impedance without any solder joints included in the measurement, such that the measurement of the DUT will include the resistance of its solder joints [8]. With these test fixtures, we measure stray inductance and resistance, even though we did not want to measure the stray capacitance, but we still measure stray capacitance with an open-circuited test fixture. The low stray capacitance can be because of the fact that the 4TP configuration ignores capacitance to ground [8]. Due to the close proximity of the pads to the ground path, the pads are effectively shielded from each other. Thus, this configuration is most effective for the measurement of the low-capacitance and inductance.

By calibrating the analyzer with a short in place (or by simply subtracting the short-circuit values from the measurement) , the effect of stray inductance and resistance on the measured value can be removed. Thus we can hope to achieve better repeatability. In applications where small stray impedance is needed the sensitivity of a good solder technique is also important.

The main disadvantage of this test fixture is its necessity of soldering on components. Soldering on components takes more time than connecting a DUT into a spring-loaded fixture, it means that application of this fixture is limited to design and research: it can't be used as production tool. As discussed above, limitations on repeatability arise due to soldering, even though the design of the fixture is insensitive to the solder joints, but both resistance and inductance is sensitive to the thickness of the solder joints. And thus any small variation we saw is the result of the large error in our measured inductance. Another disadvantage of the

solder connection is that the life of a single test fixture is limited [8].

This fixture helps in measuring impedance accurately and provides correct boundary conditions such the electromagnetic behavior of the DUT matches with its behavior in a high-performance circuit with a ground plane. Works has been going on to use the fixture to measure low-impedance capacitors in [14] and to measured the micro-fabricated inductors [15].

IV. MEASUREMENT UNCERTAINTY

There are a number of measurement methods and techniques are available nowadays to measure impedance. But to estimate uncertainty for each method requires a lot of space. Also estimation of uncertainty in impedance measurements is not a completely developed subject. The mathematical methods mentions in the Guide to the Expression of Uncertainty in Measurements (GUM) cannot be applied directly. Works have been going on the extension of the GUM approach, so that it can be applied to impedance measurements. But different problems are occurring in GUM approach like sample size may be insufficient for estimate the uncertainty, and differentiation of complex-valued models required computation of sensitivity matrices, also many times the results of even a simple models is a very complex mathematical expressions. Different works has been going on to address such problems, so that re-sampling numerical methods can be successfully applied.

V. CONCLUSION

Impedance metrology for the high-frequency range is a century-old activity, which is still an active field. In this paper we have tried to study one of the major problem that arises in during the study of the impedance metrology at high-frequencies i.e. presence of parasitic or stray components, which effect the measurement values. We discussed about different frequency compensation techniques that can be used to compensate the measured values. We also developed a test fixture that helps us to reduce the parasitic components at the contact of DUT and the impedance analyzer. Its primary limitation is that solder connections should be made carefully.

REFERENCES

[1] Yukio Sakabe, Masami Hayashi, Takefumi Ozaki and James Canner (1996), “High frequency measurements of multilayer ceramic capacitors”, IEEE Transaction on Components Packaging and Manufacturing Technology, vol. 19, no. 1.

[2] Li Li, Ben Cook and Mark Veatch (2001), “Measurement of RF properties of glob top and under encapsulated materials”, in Conference on Electrical Performance of Electronic Packing, 2001, pp. 121-124.

[3] Michael F Caggiano, Jack Ou, Selaka Bulumulla, and David Lischner (2001), “ RF electrical measurements of fine pitch BGA packages,” IEEE Transactions on Components and Packaging Technologies, vol. 24, no. 2.

[4] Y.L.Li, D.G. Figueroa, J.P.Rodriguez, L.Huang, J.C. Liao, M.Taniguchi, J.Canner, and T.Kondo (1998), “A new techniuuw for high frequency characterization of capacitors”, in Proceedings of the 48th Electronic Components and Technology Conference, 1998,p.1384.

[5] D.G.Figueroa and Y.L.Li (2000), “A technique for the characterization of multi-terminal capacitors for high frequency applications”, in Proceesings of the 50th Electronic Components and Technology Conference, 2000,p. 445.

[6] New Technologies for Accurate Impedance Measurement (40 Hz to 110MHz), Agilent Tehnologies, 1999,2000.

[7] S. Prabhakaran,C. R. Sullivan (2002),”Impedance-Analyzer Measurement of High-Frequency Power Passives: Techniques for High Power and Low Impedance”,Found in IEEE Industry Applications Society Annual Meeting, Oct. 2002, pp. 1360–1367.

[8] Rudy G. H. Eschauzier, J ohan H. Huijsing,”Frequency Compensation Techniques For Lowpow Er”,springer science, 1995.

[9] Behzad Razavi,“CMOS Circuit Design , Layout And Simulation”, Professor of Electrical Engineering University of California, Los Angeles, McGraw-Hill Publication 2000.

[10] New Technologies for Accurate Impedance Measurement (40 Hz to 110 MHz), Agilent Technologies, 1999,2000

[11] The metrology of electrical impedance at high frequency: a review, Luca Callegaro, Istituto Nazionale di Ricerca Metrologica (INRIM), Strada delle Cacce 91, 10135 Torino, Italy

[12] Keysight Technologies, “Impedance Measurement Handbook, A guide to measurement technology and techniques”, 6th Edition

[13] Charles R. Sullivan, Yuqin Sun, and Alexandra M. Kern, “Improved distributed model for capacitors in high-performance packages”, in Conference Record of the 2002 IEEE Industry Applications Conference 37th IAS Annual Meeting, 2002

[14] Satish Prabhakaran, Daniel E. Kreider, Yu Lin, Charles R. Sullivan, and Christopher G. Levey, “Fabrication of thin-film V-Groove inductors using composite magnetic materials”, in International Workshop on Integrated Power Packaging, June 2000.