Design and Layout of Open Drain IO buffer with emphasis on ESD Reliability in CMOS 28nm Technology

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Abstract- *In an Integrated Circuit (IC), the Input / Output (IO) circuits are used to enable the interface between the core circuitry and external world. The IOs are also used to isolate the circuits from unsafe and noisy surroundings. In this paper, overvoltage tolerant Open Drain (OD) IO buffer is designed in 28nm CMOS technology The OD transmitter (TX) can drive at least 16mA of current into the PAD with enable feature for transmitter and receiver (RX). The operating voltages are 0.9V and 1.8V for core and IO devices respectively. However, the PAD voltage can go up to 3.3V. Hence, overvoltage protection is provided in the driver with focus on addressing the reliability issue. An ESD hardness of 2kV HBM is targeted for the IO buffer.*

Keywords- CMOS, ESD, Open Drain, Overvoltage

I. INTRODUCTION

The design of Input / Output (I/O) circuits persists to grow than ever as they enable the interface between the core of a chip and the external world. With the advancement in the speed and efficiency of the internal circuitry, the processing becomes faster. Faster chips demand for the compatible interfacing circuitry for the optimal performance. Open Drain (OD) is one among the IOs that is widely used in many chips. In the OD IO pad, one of the output states (logic LOW) is activated by the driver NMOS, but the complimentary state (logic HIGH) is defined by the external pull up resistor. One of the challenges is to design the IOs with the overvoltage tolerance in which the IO PAD voltage is beyond the normal operating voltage of the chip devices. The over voltage requirement arises from the fact that the IOs are exposed to external environment and need to operate in the uncontrolled conditions.

II. GENERAL PURPOSE IOs

A General Purpose IO (GPIO) buffer is an interfacing circuitry for the communication (either transmission or reception). The Integrated Circuits (IC's) have to communicate with each other for data transfer. For example, CPU has to fetch data from memory for instructions. In response to this, the RAM has to receive and interpret the request of CPU and provide the data requested by the CPU. Thus, both CPU and RAM need to have transmitter and receiver modules. The functionality of IO is not just transmitting and receiving data. It should also provide ESD robustness for the pins that are exposed to the external world operating with different voltage levels. The GPIOs can be classified into rail-to-rail buffer and Open Drain buffer. In the rail-to-rail buffer, the signaling will be from ground (vss) to the power supply (vdd). The logic levels HIGH and LOW are defined by the PMOS and NMOS devices present in the driver block. LVCMOS uses the rail-to-rail signaling. In the Open Drain buffer, PMOS is not present in the driver circuit. The logic high is determined by the external pull-up resistor. Open drain buffers are used in the voltage translation applications and in the systems where multiple devices are connected to a common bus.

Design of OD buffer

The block diagram of OD TX is shown in Fig.1. Design of each of the blocks is explained below.

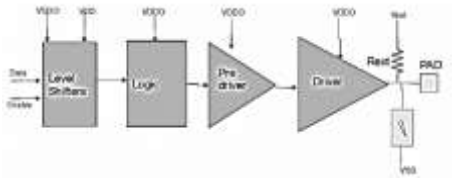

Fig.1 Block diagram of OD Transmitter

The input signal 'Data' comes from the core of the chip in the VDD domain. Contention mitigated architecture is used for the level shifters that translate the VDD domain signal to the VDDO domain for data and enable signals. Duty Cycle Distortion (DCD) is one of the critical transient specifications for the level shifter and it is verified across the process corners. The DCD is within + / - 5% in the TX.

PAD signal is the output of the TX when the Enable pin is logic LOW. When the enable spin is logic HIGH, the TX would be disabled. This logic operation is achieved in the pre-driver circuit. The design of pre-driver is crucial in TX, as

turning ON / OFF of the driver is influenced by the slew rate of pre-driver signal. Pre-driver circuit also as acts as an interface between small sized logic and large capacitive driver is required to drive a strong and geometrically large driver. The sizing of the pre-driver is dependent on the gate capacitance of the driver. As per the truth table of the IO buffer as shown in Table 1 below and the drive strength of the driver, 'NG' signal is generated.

Table 1 Truth Table of OD Buffer

OUTENB	I	NG	PAD
0	0	1	0
0	1	x	Hi-Z
1	x	x	Hi-Z

The output of the pre-driver is fed as input to the driver stage. The driver consists of large sized NMOS transistors. Since the OD buffer has to support the overvoltage condition, stacked architecture is used for the driver. The schematic of the driver is as shown below in Fig.2.

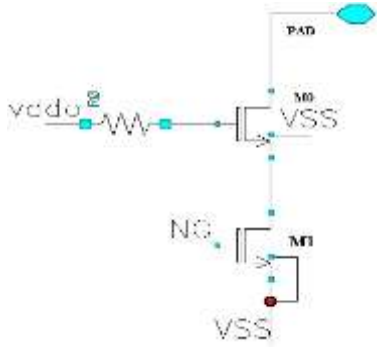

Fig.2 Schematic of Stacked OD Driver

The NMOS device M1 is the main driver and NMOS device M0 acts as the protection MOSFET. As the devices operate at 1.8V but the PAD can go up to 3.3V, a single NMOS between 3.3V PAD and 0V VSS would see high junction stress. Hence protection device is introduced. The reliability analysis for different combinations of PAD and NG signals is presented below.

Table 3. Reliability Analysis

Sl. No.	NG	PAD
Case-1	0	0
Case-2	0	3.3V
Case-3	1.8V	0
Case-4	1.8V	3.3V

Case-1: Since PAD is low, all the terminal voltages are at nominal conditions and no overvoltage stress on any junctions and hence no concerns.

Case-2: NG is low. Hence, lower NMOS is OFF. For the protection device, gate is at 1.8V. Drain to gate voltage will be 3.3 - 1.8 = 1.5V. Further, the source of the protection device is open hence no current in the source to drain path implies that the Vgs should be zero. Thus source voltage is ~1.8V; Vds = 3.3-1.8=1.5V. Thus there is no reliability issue.

Case-3: Since PAD is low, all the terminal voltages are at nominal conditions and no overvoltage stress on any junctions and hence no concerns.

Case-4: NG is high. Hence, lower NMOS driver is ON which tries to pull the intermediate net to vss. As the protection devices is also ON, the PAD signal would be pulled down to logic low. Hence PAD voltage would not be 3.3V. Thus, no reliability concern for any junctions.

From the above analysis, it can be confirmed that, with the stack devices and proper biasing conditions, there are no reliability concerns for the driver and protection NMOS. Also, the gate of the protection transistor is biased using a simple resistive network. The size of the driver is decided based on the current drive strength and the load capacitance. For the proposed OD buffer, driver strength of 20mA for load cap of 400pF is achieved across the process corners.

As the PAD pin is exposed to the external environment, it requires the ESD protection. A typical dual–diode ESD cannot be used in the Open Drain architecture because the diode added between PAD to VDDO gets forward biased in normal operation as PAD signaling can go up to 3.3V but VDDO is 1.8V. Hence, for the ESD zap between PAD (+) to VSS (-), a snap clamp is used. The snap clamp operates in the BJT mode triggered by the avalanche breakdown caused by the high electric field of the ESD. The snap clamp is designed for 2kV HBM. (~1.3A of peak ESD current.)

The block diagram of OD RX is shown in Fig. 3

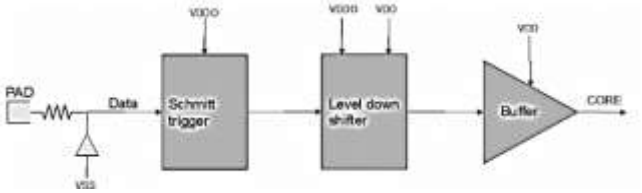

Fig. 3 Block Diagram of OD RX

The receiver consists of Schmitt trigger as the level detecting block with hysteresis property to achieve higher noise

margins. The schematic of the Schmitt trigger is shown below in Fig.4.

In the RX, the PAD connection has a series resistance of 200Ω as the secondary ESD protection. The voltage clamping block is added for reliability purpose. The clamping circuit limits the PAD voltage to VDDO.

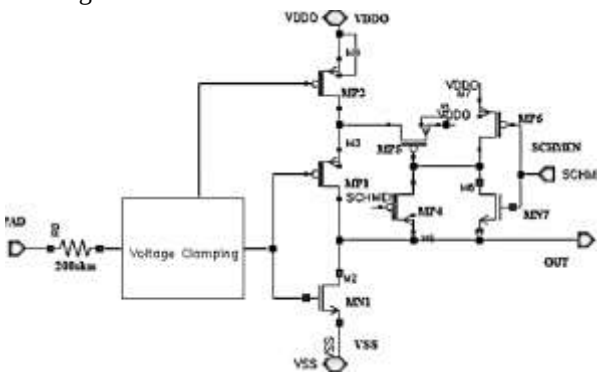

Fig.4 Schematic of Schmitt Trigger

TX		Achieved Specs			
		Min	**Typ**	**Max**	**Units**
Transient Specifications	t_r	280.7	277.9	297.1	ns
	t_f	8.13	13.38	25.8	ns
	t_{dr}	222.1	225.7	232.01	ns
	t_{df}	12.8	21.22	37.7	ns
	dcd	184.4	204.5	219.1	ns
DC Specifications	I_{OL}	21.3	34.4	59.4	mA
	V_{OL}	174.3	194.1	366.5	mV
	I_{dd}	2.19p	20n	535n	A
	I_{ddq}	0.41n	30n	1.02u	A
	I_{oz}	9.8p	26p	1.8n	A
	R_{PD}	11.7k	17.6k	22.8k	ohm

RX		Achieved Specs			
		Min	**Typ**	**Max**	**Units**
Transient Specifications	t_r	0.023	0.031	0.042	ns
	t_f	0.045	0.059	0.083	ns
	t_{dr}	0.64	0.822	1.2	ns
	t_{df}	0.61	0.718	0.884	ns
	dcd	-0.39	-0.103	0.079	ns
DC Specifications	V_{IH}	0.49	0.56	0.62	mV
	V_{IL}	0.36	0.42	0.47	mV
	V_{HYS}	0.12	0.135	0.16	mV

The devices MP2, MP4 and MP5 determine the regenerative feedback for the input stage devices and decide the threshold levels VIH, VIL and the hysteresis VHYS. For the proposed OD buffer, VIL of 0.3 and VHYS of 0.1 is achieved.

The level down shifter converts the VDDO signal to VDD domain and the signal OUT is the final output of the receiver. In this section, the design of overvoltage tolerant IO is discussed. The design is implemented in 28nm CMOS process.

Simulation Results

The OD buffer designed here targets the Fast Mode of the I2C protocol. Maximum data rate is 400 kbps with 400pF of load capacitance. All the simulations are carried out across the process, voltage and temperature corners. Fig.5 shows the transient waveforms obtained for the proposed TX. All the waveforms switch to their respective HIGH and LOW logics ensuring the functionality. The transient waveforms for the RX is shown if Fig. 5. The drive strength results are shown in Fig.6. A minimum of 21.34mA is achieved across the PVT corners.

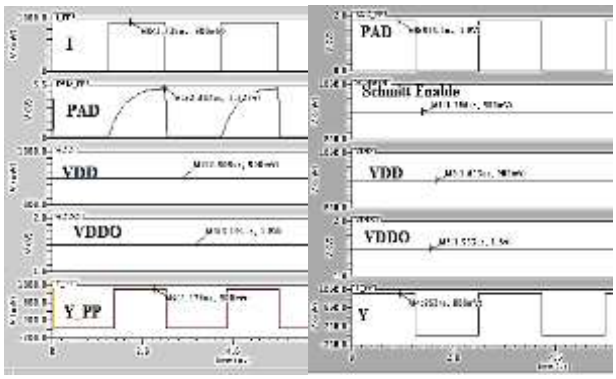

Fig.5 TX and RX transient waveforms

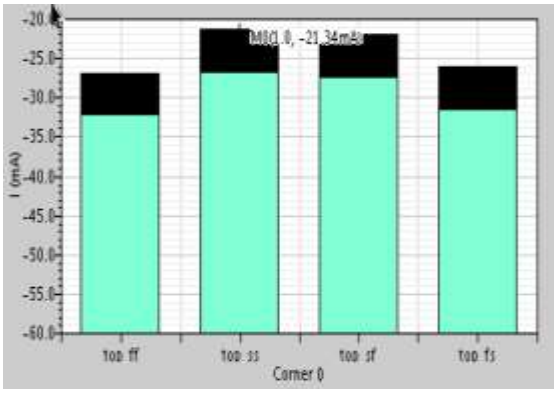

Fig.7 Drive Strength of OD Buffer.

Layout is implemented as per the PDK technology rules. The OD buffer is LVS, DRC and density clean. Post-layout simulations are carried out and the design is verified across the corners. The simulations results are tabulated in the below Sim Compliance Matrix (SCM).

III. CONCLUSION

In this paper, overvoltage tolerant Open Drain IO buffer is designed. The ESD reliability ensured in different cases. The proposed design meets the transient and DC specifications of the I2C protocol for Fast Mode (up to 400kbps data rate) with PAD voltage ranging from 0 to 3.3V. The leakage current for the core supply, IO supply and PAD are 0.5uA, 1.05uA and 1.5nA respectively ensuring the low power design. The physical layout is dense and one of the compact sizes possible in 28nm. The physical design meets all the design requirements and technology rule checks.

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