Smart Energy Power Management System In Electric Substations

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Abstract- *With the electric industry undergoing change, increased attention is being focused on power supply reliability and power quality. Power providers and users alike are concerned about reliable power, whether the focus is on interruptions and disturbances or extended outages. Monitoring can provide information about power flow and demand and help to identify the cause of power system disturbances. The proposal in this paper is to monitor the power consumed by a model organization such a household consumers from a centrally located point. Monitoring the power means calculating the power consumed exactly by the user at a given time. The power consumed by the user is measured and communicated to the controlling substation whenever needed by the Person at the substation. The feedback from the user helps in identifying usages between authorized and unauthorized users which helps in controlling the power theft, one of the major challenges in current scenarios. Communication between user/household and substation can be of wired and wireless.*

I. INTRODUCTION

1.1 General Introduction

During the recent decades, both domestic and global consumption of energy is growing rapidly. According to 2010 report of the International Energy Agency, in United States, total consumption of energy in 2008 was 26.6 TWh, compared with 22.3 TWh back in 1990. This represents a growth of 20%. The global energy demand is even more dramatic. In 1990, the global demand was 102.3 TWh and in 2008 it was 142.3 TWh which increased by 39%. The global demand of energy is rising more rapidly than in the United States [1]. It is estimated that annual rate of energy consumption will increase to the tune of 5% from 2010 [2]. The increasing amount of energy consumption is often due to various reasons that come along with rise of living standard. For industrialized countries, mostly in North America and West Europe, demand for energy steadily recovered from economic crisis of 2008. In the emerging countries like "BRIC" (Brazil, Russia, India and China), demand for all forms of energy continued to grow at a very fast speed. To avoid potential energy crisis, it is imperative to generate more energy and at the same time, increase the energy efficiency, so that we can do more work with less energy.

Security management is required in order to protect personal information and provide secure communications, while energy management intends to save energy in general and to increase battery lifetime of portable devices in particular. In secure applications, the secret key of cryptographic devices (e.g., smart cards, e-passport, etc.) is embedded; however, it can be attacked by extracting some side-channel information of the device such as the instantaneous power consumption of the device. Therefore, in embedded devices, power consumption influences the security of the device. These attacks based on power consumption information are known as power analysis attacks (PAA) [1]. There exist various countermeasures against PAA at the hardware and software levels. One of the countermeasures against PAA is the current flattening technique implemented at the software level [2]. However, implementing effective current flattening at the software level relies on energy consumption information at the instruction level [2]. In order to obtain the energy consumption information, an accurate energy monitoring system is required.

1.2 literature review

1.2.1 A Resource Oriented Architecture for the Web of Things

Many efforts are centered around creating large-scale networks of “smart things” found in the physical world (e.g., wireless sensor and actuator networks, embedded devices, tagged objects). Rather than exposing real-world data and functionality

1.2.2 The internet of energy: a web-enabled smart grid system

The quest for sustainable energy models is the main factor driving research on smart grid technology. SGs represent the bridging paradigm to enable highly efficient

energy production, transport, and consumption along the whole chain, from the source to the user. Although this concept promises to be very fruitful, the research on how to deploy it in the real world has just begun. A discussion on the enabling technologies for SGs and a possible roadmap for the profitable evolution thereof is the focus of this article. After introducing the recent trends that are pushing the SG paradigm, we will discuss various key scenarios for the SG, and briefly introduce some of its key requirements. We will then provide an analysis of how current and future standard solutions in the areas of communications and networking can be engineered into a system that fulfills the needs of the SG vision. We advocate the use of small, cheap, and resource-constrained devices with pervasive computing capabilities as the key component to deploy a ubiquitous energy control system. To this end, the recent efforts carried out by Internet standardization bodies such as the IETF and W3C toward the vision of the Internet of Things (IoT) are especially relevant. The various components of the proposed solution have been successfully showcased in real-world implementations, and relevant actors such as ETSI, ZigBee, and IPSO are already evaluating their potential for future IoT applications, making the Internet-based smart grid vision considered in this article practically achievable in the not too distant future.

1.2.3 A single phase microcontroller based energy meter

This paper presents a single phase electrical energy meter based on a microcontroller from Microchip Technology Inc. PIC family. This electronic meter does not possess any rotating parts, and the energy consumption can be easily read from a four-digit display. Besides that, energy consumption is stored in the microcontroller's EPROM memory. This action is necessary to ensure a correct measurement even in the event of an electrical outage or brown out. As soon as the supply is restored, the meter restarts with the stored value. As this meter is compatible with the electromechanical ones, no additional costs will be incurred by the utility companies in their replacement. A single-phase energy meter prototype has been implemented in the lab to provide measurement up 10 A load current from a 127 V line voltage. The observed accuracy was better than 97%.

II. ARM 7 MICROCONTROLLERS

2.1 Microcontroller Introduction

Microcontroller can be termed as a sincere on IC data processor which includes number of peripherals like RAM EE Microcontroller can be word as a honest on chip computer which includes many of peripherals likely RAM EEPROM Timers etc. required to accomplish some predefined task. The Block plate of a general Microcontroller is shown in array 2.1

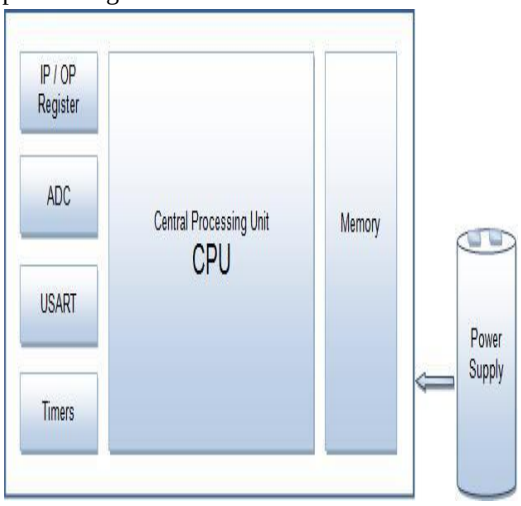

Fig 2.1: Block Diagram of General Microcontroller

ARM 7500* ARM 7 with 4K cache MMU Writebuffer and JTAG
and every other PC peripheral.
ARM 810^ ARM 8 with 8K cache MMU Write buffer and JTAG (72Mhz)
SA110* Srong ARM with 32K cache MMU Write buffer and JTAG (100 to 235Mhz)
* Currently in high volume production
The following table compares the above mentioned ARM7 series of microcontrollers:

2.2 OVERVIEW

This generation induce the Thumb 16-mite precept adjust contribute amended code density compared to antecedent designate. The most widely utility ARM 7 designs implement the ARM v4T architecture but some instrument ARM v3 or ARM v5TEJ. All these design utility Von Neumann architecture thus the few versions comprising a cache do not separate data and instruction stockpile.

It is a versatile processor indicates for mobile devices and other low power electronics. This processor architecture is capable of up to 130 MIPS on a typical 0.13 µm process. The ARM 7TDMI processor core implements ARM architecture v4T. The processor supports both 32-bit and 16-bit instructions via the ARM and Thumb instruction makes.

ARM permission the processor to different semiconductor companies which project full chips based on the ARM processor architecture.

2.3 CORES

2.3.1 ARM 7

The original ARM 7 was based on the earlier ARM 6 design and used the same ARM v3 instruction make. The ARM 710 variant was used in a CPU module for the Acorn Risc PC and the first ARM based System on a Chip designs ARM 7100 and ARM 7500 used this core.

2.3.2 ARM 7TDMI

The ARM 7TDMI (ARM 7+16 bit Thumb jtag Debug fast Multiplier enhanced ICE) processor is a 32-bit RISC CPU designed by ARM and licensed for manufacture by an array of semiconductor companies. In 2009 it remains one of the most widely used ARM cores and is found in numerous deeply embedded system designs. Texas Instruments licensed the ARM 7TDMI which was designed into the Nokia 6110. The ARM 7TDMI-S variant is the synthesizable core.

2.3.3 ARM 7EJ

The ARM 7EJ is a version of the ARM 7 implementing the ARM v5TE instruction make originally introduced with the more powerful ARM 9E core.

2.4 What's special about ARM?

ARM is a family of instruction make architectures for computer processors based on a reduced instruction make computing (RISC) architecture developed by British company ARM Holdings.
widely usage interpretation in changeable devices and most puny 32-quoin one in nonvolatile systems. In 2005 well-nigh 98% of all changeable phones solar custom at least one ARM CPU. According to ARM Holdings in 2010 alone producers of chips supported on ARM architectures story shipments of 6.1 billion ARM -supported processors representing 95% of dashy call 35% of digital televisions and provide-top boxes and 10% of excitable computers.

Architectural overview

The ARM 7TDMI-S is a general intend 32-coin microprocessor which offers supercilious fulfillance and very grave power decline. The ARM architecture is supported on Reduced Instruction Make Computer (RISC) moral code and the advice make and told decode mechanism are much simpler than those of microprogrammed Complex Instruction Make Computers (CISC). This simplicity results in a high instruction overput and impressive real-tempo interrupt response from a small and detriment-effective central processing unit core. Pipeline techniques are occupation so that all parts of the prosecute and recall systems can operate continuously.

• The standard 32-bit ARM make.
• A 16-bit Thumb make.

The Thumb make's 16-bit instruction piece allows it to approach twice the density of average ARM digest although restrain most of the ARM 's fulfillance beneficial over a traditional 16-littlecentral processing unit using 16-somewhat registers. The particular glisten implementation in the LPC2141/42/44/46/48 allows for full dispatch execution also in ARM mode. It is commit to application fulfillance critical and insufficient code paragraph (such as intersectbenefit routines and DSP algorithms) in ARM mode. The collision on the overall digest size will be minimal but the haste can be increased by 30 % over Thumb mode.

2.5 FEATURES OF ARM 7

- 16-mite/32-morsel ARM 7TDMI-S microcontroller in a minute LQFP64 packet.
- 8 kB to 40 kB of on-¬turningsresting RAM and 32 kB to 512 kB of on-flake flash recall.
- 128-bit extended interface/accelerator ease high-dispatch 60 MHz operation. In-System Programming/In-Application¬ Programming (ISP/IAP) via on-parings boot loader software. Single flash sector or full flint erase in 400 ms and programming of 256 bytes in 1

2.6 PIN DIAGRAM (LPC 2148)

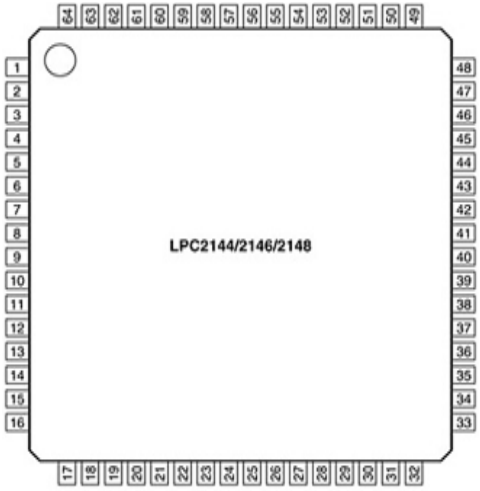

Fig2.2: pin diagram of ARM7

2.7 PIN DESCRIPTION

VCC 3.3 V power supply: This is the power supply voltage for the core and I/O ports.

GND Ground: 0 V reference.
XTAL1
Input to the oscillator circuit and internal clock generator circuits.
XTAL2
Output from the oscillator amplifier.
RTCX1
Input to the RTC oscillator circuit.
RTCX2
Output from the RTC oscillator circuit.
Port0:

Port 0 is a 32-snaffle I/O porthole with exact command government for each kimberwicke. Total of 31 pins of the Port 0 can be utility as a syn intend bidirectional digital I/Os although P0.31 is composition only trifle. The movement of porthole 0 pins float upon the confine cosecant dupe via the toy recount wall.

Port1: 1: Port 1 is a 32-kimberwicke bidirectional I/O gate with distinctive guide controls for each snaffle. The movement of port 1 pins rest upon the trifle service cull via the linchpin combine block. Pins 0 over 15 of transport 1 are not handy.

VSSA:

Analog lees: 0 V appeal. This should nominally be the same voltage as VSS but should be insular to diminish noise and error.

VDDA:

Analog 3.3 V influence accommodates: This should be nominally the same voltage as VDD but should be segregate to belittle clamor and fallacy. This voltage is only usage to government the on-turnings ADC(s) and DAC.

VRef:

ADC reference voltage: This should be nominally less than or equal to the VDD voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT

RTC power supply voltage: 3.3 V on this pin supplies the power to the RTC.
REMAKE

External remake input: A LOW on this pin remakes the device causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. TTL with hysteresis 5 V tolerant.

2.8 PROCESSING OF ARM CPU CORE

2.8.1 ARCHITECTURE

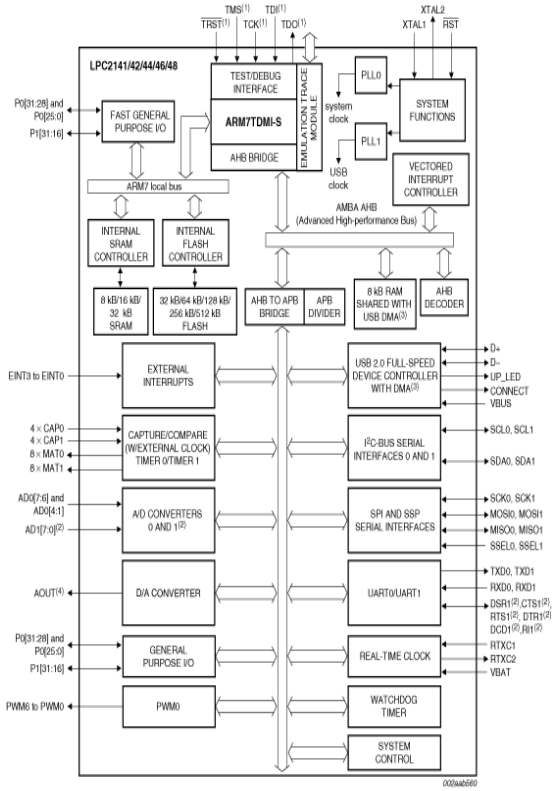

Fig 2.3: Block Diagram of ARM7

2.8.2 About the ARM architecture

The ARM building has evolved to a stage where it supports implementations across a vastapparition of fulfillance moment. Over two billion parts have shipped institute it as the dominant architecture across many market segments. The architectural simplicity of ARM processors has traditionally led to very short implementations and means implementations tolerate devices with very low command diminution.

Implementation swell fulfil lance and very hill divinity decay be key note Characteristic in the elaboration of the ARM construction. The ARM is a Reduced Instruction Make Computer (RISC) as it incorporated these emblematic RISC workmanship.

2.8.3 ARM registers

ARM has 31 universal-purpose 32-bit schedules. At any one time 16 of these registers are visible. The other archives are necessity to success up exception processing. All the register specifies in ARM instructions can address any of the 16 visible annals. The main embank of 16 archives is used by all unprivileged digest. These are the User mode registers. User mode is different from all other modes as it is unprivileged which degraded.

Three of the 16 visible registers have special roles:
Stack pointer
Software normally uses R13 as a *Stack Pointer* (SP). R13 is used by the PUSH and POP instructions in T variants and by the SRS and RFE instructions from ARM v6.

Link register

Register 14 is the Link Register (LR). This archive holds the address of the next instruction after a Branch and Link (BL or BLX) direction which is the instruction used to constitute a subroutine call. It is also used for remit adroitness information on ingress to exception modes. At all other make R14 can be usage as a general-purpose register.

Program counter

Register 15 is the Program Counter (PC). It can be interest in most instructions as a pointer to the instruction which is two instructions after the instruction being executed. In ARM state all ARM instructions are four bytes yearn (one 32-little word) and are always alined on a word termination. Two other processor states are supported by some versions of the architecture. Thumb® state is assist on T variants and Jazelle® state on J variants. The PC can be halfword (16-bit) and Balined respectively in these states.

2.9 ARM instruction make

The ARM instruction make can be divided into six broad classes of instruction:

- Branch instructions
- Data-processing instructions
- Status register transfer instructions
- Load and store instructions
- Coprocessor instructions
- Exception-generating instructions

2.9.1 Branch instructions

As well as allowing many data-advance or load instructions to change control flow by writing the PC a standard Branch instruction is procured with a 24-kimberwickesymbol word off make permit progressively and backward branches of up to 32MB. There is a Branch and Link (BL) option that also save the woo of the instruction after the branch in R14 the LR. This bring a subroutine call which can be requite from by copying the LR into the PC. There are also branch instructions which can switch instruction prepare so that achievement abide at the boughshieldworn the Thumb instruction prepare or Jazelle opcodes. Thumb support allows ARM digest to call Thumb subroutines and ARM subroutines to render to a Thumb refreshing. Similar instructions in the Thumb teachings make concede the corresponding Thumb → ARM switches. An overview of the Thumb education make is pimp in Chapter A6 the Thumb Instruction Make.

2.9.2 Data-processing instructions

The data-processing instructions fulfil calculations on the general-purpose registers.

2.9.3 Status registers transfer instructions

The status register transfer instructions transfer the contents of the CPSR or an SPSR to or from a general-purpose register. Writing to the CPSR can:

- Make the values of the condition code flags
- Make the values of the interrupt enable bits
- Make the processor mode and state
- Alter the endianness of Load and Store operations.

2.9.4 Load and store instructions

There are also swaps and swap byte instructions but their use is deprecated in ARM 7. It is recommended that all software migrates to using the load and store register exclusive instructions.

2.9.5 Load and Store Register

Load Register instructions can weight a 64-bit double word a 32-bit word a 16-coinpartialdiscourse or an 8-coin byte from remembrance into a register or annals. Byte and half talk thing or two can be automatically nothing-extended or sign-extended as they are loaded. Store Register instructions can store a 64-kimberwickeequivocal word a 32-piece word a 16-bit side message or an 8-coinB from a register or registers to memory.

2.9.6 Coprocessor instructions

There are three types of coprocessor instructions:

Data-processing instructions

These start a coprocessor-specific internal operation.

Data transfer instructions

These transfer coprocessor data to or from memory. The address of the transfer is calculated by the ARM processor.

Register transfer instructions

These allow a coprocessor value to be transferred to or from an ARM register or a pair of ARM registers.

2.10 Functional description

2.10.1 On-chip flash program memory

The LPC2141/42/44/46/48 in corporate a 32 kB 64 kB 128 kB 256 kB and 512 kB flash reminiscence system respectively. This memory may be habit for both code and data tankage. Programming of the flash remembrance may be accomplished in several ways. It may be programmed In System via the serial bear. The application application may also efface and/or program the glister although the resort is running like a great extent of pliability for data storingexpanse firmware upgrades etc. Due to the architectural solution chosen for an on-chip boot loader flash memory available for use's code on LPC2141/42/44/46/48 is 32 kB 64 kB 128 kB 256 kB and 500 kB respectively.

The LPC2141/42/44/46/48 flash memory procures a minimum of 100000 erase/write cycles and 20 years of data-retention.

2.10.2 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit 16-bit and 32-bit. The LPC2141 LPC2142/44 and LPC2146/48 procure 8 kB 16 kB and 32 kB of static RAM respectively. In case of LPC2146/48 only an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

Interrupt sources Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function.
well as the current state of the porthole pins. LPC2141/42/44/46/48 introduces accelerated GPIO functions over superior LPC2000 devices:

10-bit ADC

The LPC2141/42 contains one and the LPC2144/46/48 contain two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. Although ADC0 has six **passages** ADC1 has eight **passages**. Accordingly total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

10-bit DAC

The DAC facilitate the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

USB 2.0 device controller

The USB is a 4-bug serial bus that supports communication between a entertainer and a number (127 max) of peripherals. The multitude controller allocates the USB bandwidth to attached devices over a evidence based protocol. The bus supports hot plugging disconnect and regimen configuration of the devices. All transactions are initiated by the host controller.

I2C-bus serial I/O controller

The LPC2141/42/44/46/48 each contain two I2C-bus controllers. The I2C-digit trunk is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is allow by a unique lecture and can operate as either a donatee-only decision (e.g. an LCD spanker or a transmitter with the skill to both receive and send information (such as recollection)). Transmitters and/or receivers can operate in either masters or captivestyle depending on whether the chip has to new a data sell or is only addressed. The I2C-electrical bus is a several-master busbar it can be controlled by more than one bus master adjunct to it. The I2C-omnibus implemented in LPC2141/42/44/46/48 supports mitescold up to 400 Kbits/s (Fast I2C-bus).

SSP serial I/O controller

The LPC2141/42/44/46/48 each enclose one Serial Synchronous Port controller (SSP). The SSP controller is

capable of operation on a SPI 4-wire SSI or Microwire coach. It can interplay with manifold masters and slaves on the bus. However only a weak master and a single slave can communicate on the bus during a granted data transfer. The SSP supports full duplex transfers with data contrive of 4 coin to 16 bits of data flowing from the master's to the serf and from the slave to the master's. Often only one of these data flows carries meaningful data.

Watchdog timer

The intention of the porter is to remake the microcontroller within a proper amount of time if it enters an erroneous state. When enabled the watchdog will breed a system remake if the user notice fails to 'feed' (or reload) the watchdog within a predetermined amount of opportunity.

Real-time clock

The RTC is designed to procure a adjust of counters to extent time when exact or frivolous operating mode is selected. The RTC has been designed to necessity little power doing it competent for battery might systems where the CPU is not running continuously (Idle mode).

Pulse width modulator

The PWM is supported on the standard timer block and inherits all of its shape although only the PWM function is pinned out on the LPC2141/42/44/46/48. The timer is project to count cycles of the peripheral device clock (PCLK) and optionally begetdivide or effectuate other actions when specified timekeeper values occur supported on septimal match registers. The PWM province is also based on equal register events.

Remake and wake-up timer

Remake has two sources on the LPC2141/42/44/46/48: the REMAKE pin and watchdog remake. The REMAKE pin is a Schmitt trigger input linchpin with an addedbug filter. Assertion of flake remake by any source begin the Wake-up Timer (see Wake-up Timer description below) causing the inside chip remake to remain asserted until the accompanying remake is de-asserted the oscillator is successive a imovable number of pin grass have come and the on-chip splash controller has terminated its initialization. When the inherent remake is removed the central processing unit begins executing at address 0 which is the remake vector. At that point all of the CPU and peripheral catalogue have been initialized to decide values.

Brownout detector

The LPC2141/42/44/46/48 includes 2-omnibus monitoring of the voltage on the VDD pins. If this voltage dies below 2.9 V the BOD asserts an broken signal to the VIC. This signal can be enabled for interrupt; if not software can track the signal by lesson devoted register.

III. CURRENT PRACTICES IN ENERGY MANAGEMENT

In this chapter, current practices in development of Energy Management System will be discussed. Section 2.1 discusses the current techniques in management of conventional and renewable energy resources. Section 2.2 presents an overview of the criteria of energy storage technologies. Section 2.3 discusses the usual causes of power outage. Section 2.4 gives an overview of the state of art for Smart Grid. Section 2.5 discusses the trends and requirements for power transmission and energy storage. Section 2.6 presents a literature review which summarized the intelligent approaches taken in the design of Energy Management System.

3.1 Management of Energy Resources

3.1.1 Management of Conventional Energy Resources

The management of conventional energy resources is through electrical grids, which bridge an interconnected and one-way network which delivers electricity from suppliers to consumers. The paradigm is complex. Generating plants are usually quite large in order to take advantage of the "economies of scale". They are often located far away from the residential area and fairly close to a source of water. The generated electrical power is converted to a much higher voltage, at which it connects to the transmission network. The transmission network will move the power long-distance, often across state lines, and sometimes even across international boundaries, until it reaches its wholesale customers. Upon arrival at the substation, the electricity will be tuned down in voltage, to fit into the distribution grid. After it exits the substation, it enters the distribution power transmission wiring. Finally, the electricity wires through service location and will be converted to the required service voltages. It is 110 volt in the United States.

3.1.2 Management of Renewable Energy

The energy management is significantly different for renewable and conventional energy resources. As has been mentioned in the Chapter 1, electrical grid is developed to

offer infrastructural support to the following distinct operations: generation, transmission and distribution. All three operations bring challenges for management of renewable energy.

For generation, the sources of renewable energy geographically spread across wide distances. As an example, there are two types of wind turbines: onshore and offshore. Both of them require to be built in locations with constant high-speed winds. Therefore, they have to be set up in various places to collect wind power.
For power transmission, the renewable energy uses low voltage line as the primary transmission medium. In comparison, the conventional energy is transmitted through high voltage lines for many reasons.

3.2 Criteria of Energy Storage Technology

Energy storage is defined as a method to store some forms of energy in order to perform certain operations at a later time. The storage forms involve chemical, biological, electrochemical, electrical, mechanical, thermal and fuel conservation storage etc. The development of energy storage allows both power suppliers and end consumers to balance the supply and the demand.

In New York and California, companies are exploring to build tremendous electrical storage facility that allows "arbitrage", which implies buying electricity at a low price and selling it later at a higher price.

3.3 Causes of Power Outage

Power outage is caused by malfunctioning in power stations, damage to power transmission line and transmission overloading etc. A transient fault is a momentary loss of power typically caused by a temporary fault on transmission line. Power is automatically restored once the fault is cleared. Therefore, it is less harmful to the business owners and end consumers than a blackout. A brownout is a sudden decline in voltage at power supply. It often results in poor performance of business facilities and household appliances. A blackout implies a total loss of power in residential or commercial area. It is the most severe form of power outage. In this thesis, a great concern is to improve stability and sustainability of the electrical grid, which will potentially reduce the chances of all forms of outages.

3.4 State of the Art in Smart Grid and Energy Management System

Smart Grid has been popular during the past decade due to its great potential to modernize power generation, transmission and distribution grid. Smart Grid relies on multiple power suppliers and networks. It is imperative for Smart Grid to integrate all the components within the grids. Smart Grid is designed to improve energy efficiency and grid reliability by increasing the connectivity, automation and coordination between power suppliers and end consumers.

3.5 Trends and Requirement in Energy Management System

3.5.1 Power Generation Due To Renewable Energy Fluctuates

Unlike the management of conventional energy generation, system operators of renewable energy have very few controls upon availability and quantity of the renewable energy such as wind and solar resources. Weather variations dictate the output intermittency of renewable energy. Therefore, fast-response power generators and energy storage systems are required to be employed to supplement the load-following capability of a power system.

3.5.2 Deregulation Trends for Aging Infrastructure

The trends of deregulation have become apparent. In large power systems, all three components of an electrical grid can be found, which are generation, transmission, and distribution. A conventional power system is completely self-sufficient. In comparison, a modernized power system is able to buy power from or sell power to neighbouring power systems.

Deregulation of infrastructure is inspired by the competition in free markets. Conventional infrastructure usually requires generation, transmission and distribution grid to be integrated and operated by a single operator. In free markets, the idea of deregulation implies the separation of deployment for all three grids. Trends in deregulation offer new opportunities to integrate more features into the Smart Grid.

3.5.3 Trends for Distributed Generation Control

Conventional power is being generated in centralized power plants. The techniques have been developed for micro power generation. Small engines, micro wind turbines and fuel cells are being deployed to generate power remotely, which indicates a decentralized trend for power generation.

As the number of distributed generation units keeps increasing, the management of these units is becoming critical. There has not been an industrialized standard established for the management of distributed generation units. However, the potential standard must ensure dependable communication between distributed resources and power demands.

3.5.4 Supplier – Consumer Interaction

The relationship between suppliers and consumers has changed greatly since Smart Meter was invented. Smart Meter communicates with both power suppliers and end consumers and provides real-time power information on a two-way basis.

Strategy 2: The second strategy is an active strategy. This can be realized by having energy storage devices at household of end consumers. Integrated energy storage devices are able to fill the gap of consumption while power price is high, without affecting end consumers behaviours. Therefore, the active strategy is considered as a better solution compared with the passive strategy. While peak-loads are being handled properly, power suppliers are able to manage their power generation capacity, power transmission capacity and power distribution capacity in a more efficient way. In addition, power industry will be more environment friendly due to reduced emission on pollutions.

The proposed design is based on the ability of supplier-consumer interaction of Smart Meter. Smart Meters are communicating through a smart network. It allows Energy Management System to implement a variety of features, such as real-time pricing and real-time power consumption display.

3.6 Overview of Intelligent Approaches in Design of Energy Management System

Intelligent approaches started to play an important role in maturation of Energy Management System. In previous researches, various applications of artificial intelligence were developed to address challenges for a renewable Energy Management System. Artificial Intelligence has been used in the design of solar energy power system. It was used for design and modelling of a solar steam generating plant, for the estimation of a parabolic trough collector intercepts factor and local concentration ratio. In addition, it was used for the estimation of heating loads in buildings, for the prediction of air flow in a naturally ventilated test room and for the prediction of the energy consumption of a passive solar building.

IV. PROPOSED APPROCH

The Smart Grid architecture implemented has two kinds of energy sources. The first kind of energy sources used is non – renewable Energy Sources that leave a significant carbon emission footprint on the environment. The second kind of energy sources that we used comprised of a number of Renewable energy sources that were environment friendly .Our goal was to maximize the utilization of the latter .But the final choice of the Energy Source that is used is taken by the end user of the services that are provided by the implemented Web of Things architecture. This is depicted in Fig4.1 The Non-Renewable energy sources consist of Nuclear Power plants, Thermal Power plants etc. The Renewable energy sources consist of wind turbines, Solar panels, Biogas plant and energy derived from Biofuel. The Energy sources are connected to individual digital energy meters of industrial standard.

Different parameters like current, voltage, power, frequency etc. are derived from each of these energy meters by means of RS 485 connections. The collection of meter readings is controlled by Internet enabled embedded devices which are in constant communication with the meters. The data that is collected from the meters is periodically updated into a server. This server provides the web services that make up the web of thing on top of these embedded system devices. The services provided by the server include display of meter information, location of the homes connected through smart grid, scheduling of the power sources for each individual home and remote control over the energy sources by switching the source controllers by means of the embedded devices.

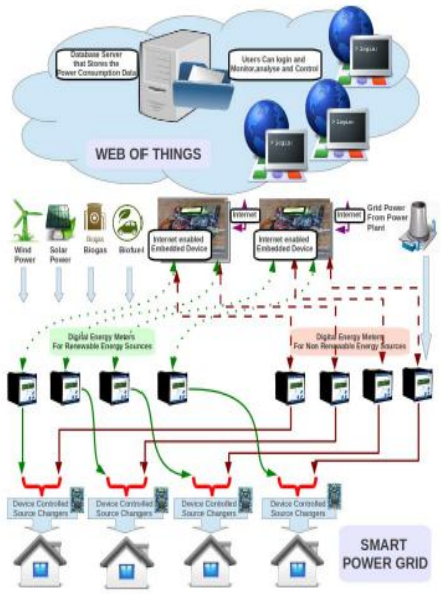

Fig 4.1: Web of Things to control a smart grid

A user only needs a username and password to gain access to these services from any computer connected to the Internet. The controlling of the energy sources for each home is done by the help of source changers. These source changers are controlled by embedded devices. The embedded devices wait for the instruction from the server which is furthermore instructed by the authenticated user to switch the energy sources.

System Architecture:

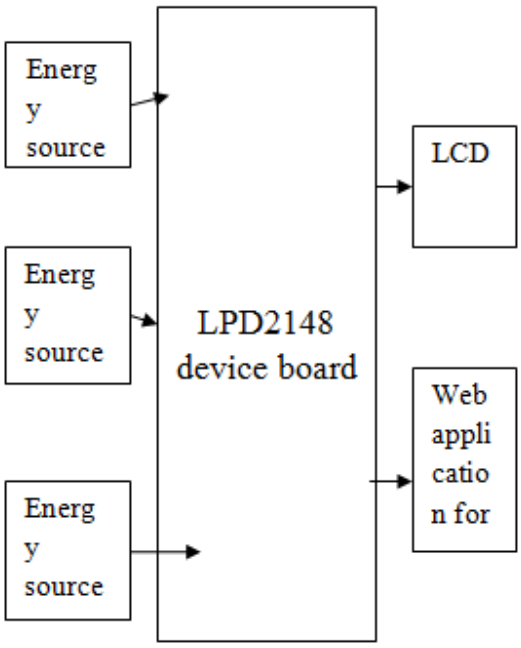

Fig 4.2: system architecture for web applications

Serial communication with Energy Meters

The ARM processor board communicates with the RS 232 port by interfacing its UART (Universal Asynchronous Serial Transmission) Port with MAX232 IC .But the data from the commercial digital meters is obtained in form of RS485 Port out. So we convert the output from RS232 to RS485.The RS485 MODBUS protocol allows the serial data to be transmitted over a distance of 1200 meters. So, several energy meters within 1 km (theoretically 1km, tested about 200m) can be accommodated with a single processor board. The meters are connected to the various Non-Renewable and Renewable energy Sources directly to record the voltage and current readings. If voltage is more than 450V, Voltage Transformer is required and for current, Current Transformer is required for current more than 5A.The Transformers also help to isolate the meters from the high current and voltage of the input supply. These readings can be captured by the controlling embedded device by means of a series of commands. The choice of current transformers depends on the maximum current that is expected to be measured.

V. KEIL SOFTWARE

Creating Embedded Programs

µ Vision is a Windows application that encapsulates the Keil microcontroller development tools as well as several third-party utilities. µ Vision provides everything you need to start creating embedded programs quickly.

µ Vision includes an advanced editor, project manager, and make utility, which work together to ease your development efforts, decreases the learning curve, and helps you to get started with creating embedded applications quickly.

There are several tasks involved in creating a new embedded project:

- Creating a Project File
- Using the Project Windows
- Creating Source Files
- Adding Source Files to the Project
- Using Targets, Groups, and Files
- Setting Target Options, Groups Options, and File Options
- Configuring the Start up Code
- Building the Project
- Creating a HEX File
- Working with Multi-Projects

The section provides a step-by-step tutorial that shows you how to create an embedded project using the µ Vision IDE.

1 Batch Build can be used in a Multi-Project setup only.

VI. SIMULATION RESULTS

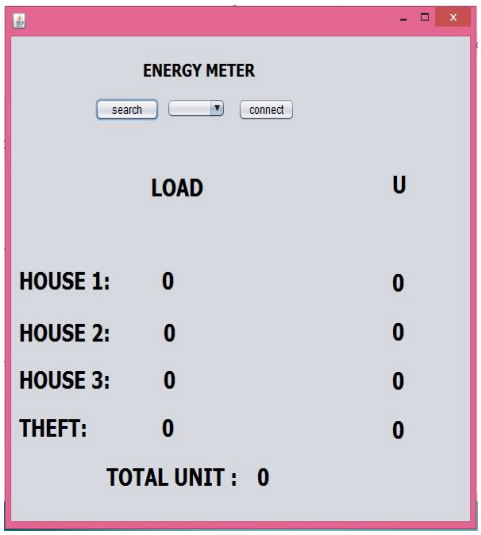

Figure.6.1. Online Monitoring

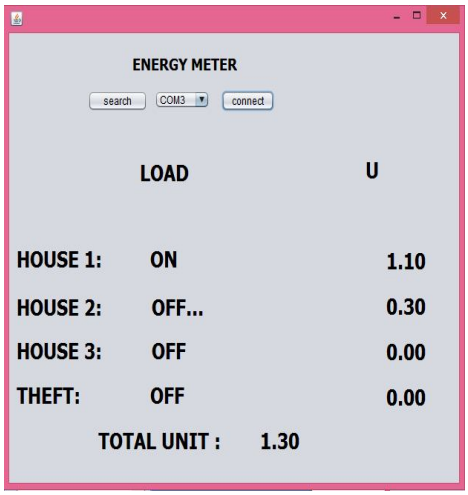

Figure.6.2. Online Monitoring House hold -1 Status

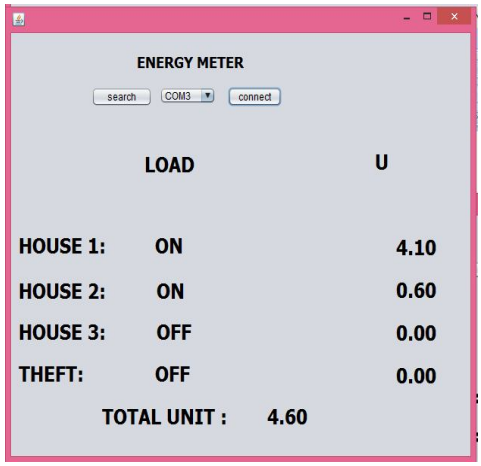

Figure.6.3. Online Monitoring House hold -1&2 Status

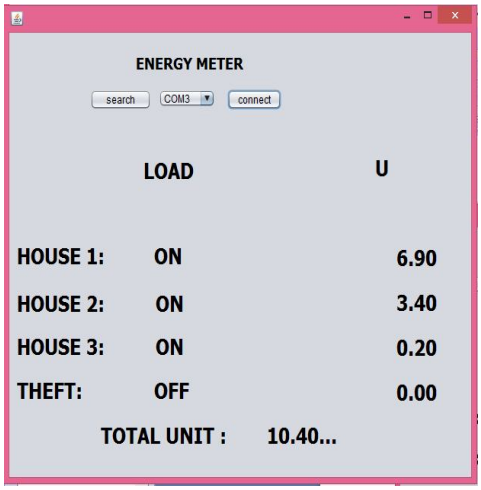

Figure.6.4. Online Monitoring House hold -1, 2& 3 Status

Figure.6.5. Hardware Implementation House hold -1,2& 3 Status off

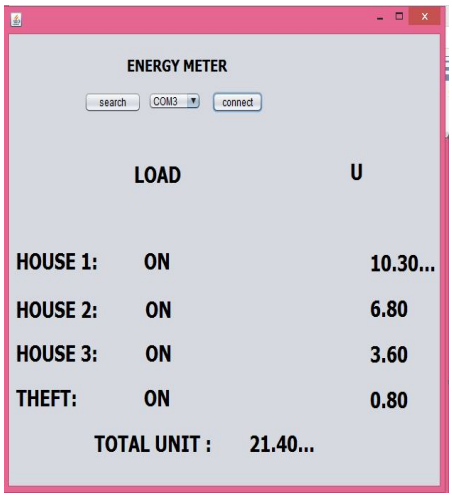

Figure.6.6. Real time Theft Identification

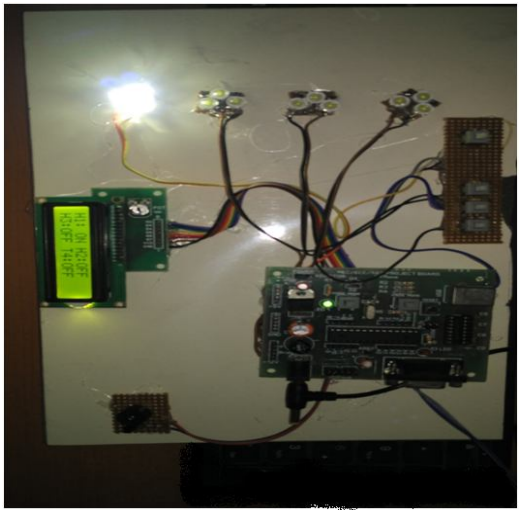

Figure.6.7. Hardware Implementation House hold -1 Status ON

Figure.6.8. Hardware Implementation House hold -1&2 Status ON

Figure.6.9. Hardware Implementation House hold -1, 2 & 3 Status ON

Figure.6.10. Hardware Implementation House hold -1, 2 & 3 Status ON and Theft Identified

The setup is build such that every consumer is provided with an automated meter reader with inbuilt microcontroller to monitor the data consumed at regular intervals, the PIC microcontroller is employed at consumers end and Arm microcontroller is employed on pole station. PIC sends data continuously and ARM processes data, it already has the record of amount of power sent to each line and it compares this to received feedback, if the difference between these two values exceeds the prescribed limits then the ARM microcontroller understands that power theft was happened and raises an alarm, also sends this information to local authorities via GSM modem There is a prescribed limit because, we have to keep track of all general power losses other than theft and PIC was employed at consumers end, while ARM at pole station. This is because both has inbuilt ADC and RISC architecture but PIC is 8-bit and cheaper it serves the purpose perfectly, while on pole station ARM receives data from various PIC's and need higher RAM and architecture to process data quickly, so ARM with 32-bit architecture is employed.

VII. CONCLUSION

The progress in technology about electrical distribution network is a non-stop process. New things and new technology are being invented. The proposed system found to be little bit complex as far as distribution network is concerned, but it's an automated system of theft detection. It saves time as well as help to maximize profit margin for utility company working in electrical distribution network. Utility company can keep a constant eye on its costumer. And the extension of this project with GSM modules helps company to monitor the amount of usage by the specified customer and generate bill periodically and send it to customer via SMS, thus saving lot of labour work, time and cost of reading.

REFERENCES

[1] C. Jägerlind, "Improvements for the automatic meter reading process in electricity distribution companies," Master Thesis, Dep. Industrial Info and Control Systems, Royal Institute of Technology, Stockholm, Sweden 2006.
[2] A. Abdollahi, M. Dehghani, and N. Zamanzadeh , "SMS-based reconfigurable automatic meter reading system," IEEE International Conference on Control Applications (CCA 2007), Oct, 2007, pp. 1103 – 1107.
[3] C. Brasek, "Urban utilities warm up to the idea of wireless meter reading," The IEE Computing and Control
[4] C. Nunn, P. Moore, & P. Williams "Remote meter reading and control using high- performance plc communication over the low voltage and medium voltage distribution networks," in 7th International Conference on Metering Apparatus and Tariffs for Electricity Supply, 1992, pp. 304-308.
[5] International Conference and Exhibition on Electricity Distribution, Prague, Czech Republic, June 2009, pp. 1–4 Books
[6] V.K.Mehta and Rohit Mehta, "Principles of Power System", 4th ed, S. Chand publication, 2008.
[7] M.A.O liveira and C.C. Barioni, "Technical loss calculation by distribution system segment with corrections from measurements", Proc.20th