OPTIMAZATION OF DIFFERENT PARAMETER OF FinFET BASED PRIORITY ENCODER

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Abstract- *For better performance and lower leakage parameters we can use FinFET either be shorted gates or independent gates. DELTA gates has good Short Channel Effects (SCE's) compared to conventional based CMOS. In this paper, determination of energy efficient techniques for Priority Encoder using Multi-threshold Complementary Metal Oxide Semiconductor (MTCMOS) MTCMOS is an effectual circuit level technique that accommodate an excessive performance and low power design by requiring both low and high threshold voltage transistors. It is also called power/ground gating technique and is conventionally used for leakage power reduction. Simulation occurs at 45nm technology using CADENCE Software and measure leakage current of FinFET based Priority Encoder compare with MTCMOS technique. MTCMOS act as leakage reduction techniques. Using MTCMOS leakage power reduces 10-15% and Leakage Current reduces 10-15% in the simple FinFET based Priority Encoder. And average power consumption is also reduced to 15-20% in MTCMOS on FinFET based Priority Encoder.*

Keywords- Short Channel Effects, FinFET, Priority Encoder, MTCMOS.

I. INTRODUCTION

Priority Encoders (PE) is commonly used in computer systems. Priority Encoder algorithm are used in number of computing components, such as comparators, fixed and floating point units[1], increments, decrements[2] and interconnection network routers[3], sequential address encoder of content addressable memories[4] are important sub-systems located on-chip or off-chip, which predominantly utilize the priority encoder function. As the computer systems data width gets longer and computer system become fasten, the speed of the Priority encoder becomes a key parameter in the performance of the computer system. At the same time, the overwhelming demand for compact electronics encourages the development of a power optimized Priority EncoderDue to aggressive scaling of technologies and devices, leakage is increasing to an unavoidable extent. So efforts are being made to design such circuits which have reduced power consumption with leakage reduction techniques. There are many popular ways of designing such circuits. One such method is to reduce the power supply around or below threshold voltage [5]-[6]. But lowering the nominal voltage has to sacrifice its functioning to some extent and consequences of lowering the supply voltage are mortification in stability of cell, noise margin, on current to off current ratio and strong sensitivity to PVT (process voltage temperature) variations [7]. There are various leakage reduction approaches for both during standby mode and run time that is when the circuit is in operation. For standby mode MTCMOS technique can play an important role for the reduction of leakage as it has one of the main advantage of implementing the technique with the existing circuit whereas for run time dynamic scaling of power supply VDD and (Vth also known as Vth Hopping) can help in reducing the leakage.

MOSFET are facing problems due to continuous scaling of devices [6]. Emphasis is given on high speed, leakage reduction techniques in fully depleted SOI devices.
In recently, MTCMOS is the most prevailing methodology in industry. It is reliable and energetic method for decreasing stand by leakage is power gating [8]. Power and ground allocation network, noise originated during sleep to active mode transitions is an outstanding reliability applied in MTCMOS circuit [9]. This technology is the used for reducing sub threshold current in standby mode while preserving circuit performance [10].

II. FINFET

Multiple gate devices for 45nm technology node are FinFET, ΩFET, cylindrical FET [11]. A critical Emerging Research Devices (ERD) to improve interconnects, connects, control embedded interface, thermodynamic stability and limit this phenomena [12]. All this effects and phenomena improvement is noticed in International Technology Roadmap for semiconductor (ITRS) research issue table of ERD in 2013 [13]. Now a day, research in VLSI domain facing tremendous problem to achieve this technological challenges associated with double gate transistors [14].

Multiple gates have many advantages and disadvantages. To reduce disadvantages we are examine

Priority Encoder using (DG) FinFET [15] in this paper and studied improvement in leakage power and FinFET has two broad divisions in SOI and bulk FinFET. Short channel effect and high doping cons. Found in bulk FinFET compare to SOI FinFET [16]-[17]. So, FinFET on silicon on insulator is preferred over bulk FinFET [18].

Double gate MOSFET and MuGFET are floating body devices into which charge trapping occurs in body this causes leakage due to radiation. Charge trapping occurs due to 'back channel interface' and 'total dose latch effect' [19].
Trapping in buried oxide potential of body modulates, when depletion between source and body is lower than electrons injected into the body and drain region collect it [20]. If electric field is high to cause impact ionization in drain occur and lead to current runaway causing snapback [21].

III. SIGNIFICANCE OF MTCMOS

MTCMOS is a multi-threshold CMOS technique. It is a technique where a high Vt (threshold voltage) transistors are inserted between the power supply and logic circuit or between logic circuit and ground or both. This results in creation of virtual supply or virtual ground respectively [22]. The logic circuit blocks consist of low Vt transistors. The reason for imposing low Vtcomponents in logic blocks is fast switching speed and high Vt header and footer to minimize the leakage. This technique is most effective in reducing standby leakage.

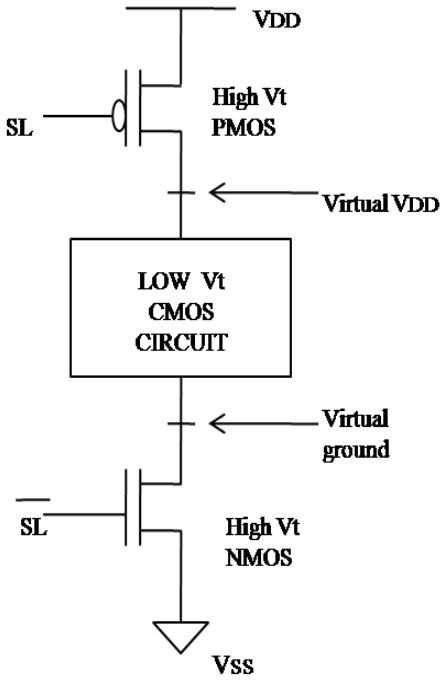


Fig1. MTCMOS circuit diagram

MTCMOS [23] (Multi-threshold CMOS) (S.Mutoh et al. 1996) and its equivalent representation offlow of current through low and high Vt transistors.

During normal mode both the high Vt PMOS and NMOS transistor are kept ON by applying signal to the gate of the transistors also denoted as SL and SL bar (sleep signal). The current flowing through this circuit will depend on the component with low threshold voltage and thus creates a virtual VDD above the logic circuit block and a virtual ground below the logic block circuit whereas in case of sleep mode both the high Vt PMOS and NMOS transistor are kept OFF and both virtual power supply rail and virtual ground rail does not exist any longer. Thus, the current that will flow through this circuit will depend on the lower of two currents as they are connected in series. Hence high Vt transistors have lower leakage current when the circuit is in standby mode. So in standby mode high Vt transistors are made OFF leading to smaller leakage current. In minimizing the leakage parameters during the run time, the key factor is threshold voltage (Vt) which is defined as the minimum voltage at which current starts flowing. This indicates smaller Vtleads to faster operation and smaller delay. To reduce the power dissipation supply voltage is scaled down and to maintain the high performance threshold voltage is scaled down.

PD = VDD2 CF (1)

Low Vt provides high performance and high Vt reduces sub threshold leakage and this can be observed clearly in coming sections the power consumed by Priority Encoder both with and without MTCMOS[24] technique.

IV. EFFECT OF LEAKAGE CURRENT AND POWER

Power dissipation occurs due to charging and discharging of load capacitances it refers to as the dynamic power dissipation. Dynamic power is consumes when switching in bits going on either "0" to "1" or "1" to "0". It provides the region of transistors works in active region and cutoff region, the current is:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right) (1)$$

For active region, the current equation is:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS}\right) \quad (2)$$

For saturation region, the current equation becomes:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(\frac{{V_{DS}}^2}{2}\right) (3)$$

Scaling down technology to a significance value increases the performance but total power consumption in some portion not decreases due to leakage parameters [25] due to reduced

threshold voltage and high packaging density [26]. ITRS in 2014 that 13% of feature size shrinks per year. The cost of memory also reduces because of bulk production of units. The gate oxide thickness reduces drastically as feature size reduces then gate tunneling leakage current increases [27].
Power dissipation has four components in digital circuits:

$$P = P_{ds} + P_{sc} + P_{sb} + P_{leakage} (4)$$

In which P is the total power dissipation, P_{ds} is the dynamic-switching, P_{sc} is the short circuit, $P_{sb}$is the static-biasing and $P_{leakage}$is the leakage power.
The power dissipation in dynamic-switching depends upon frequency, capacitor and supply voltage i.e.

$$P_{ds} = CV^2 f \quad (5)$$

The short circuit power dissipation is depends on τ rise time or fall time, and clock frequency f.
The formula is:

$$P_{sc} = K(V_{dd} - 2V_{th})^3 \tau f \quad (6)$$

The flow of static current towards ground from Vdd without input degradation is leakage power.
Three leakage mechanismsare: Sub threshold, band to band tunneling (BTBT) and gate oxide [27].

$$I_s = I_o W e^{\frac{V_{gs}-(V_{t0}-\eta V_{ds}-\gamma V_{bs})}{nV_T}} \left[1-e^{\frac{-V_{ds}}{V_T}}\right] \quad (7)$$

Where $I_s$is the sub threshold leakage current, $V_{t0}$the zero bias thresholds, n isis the sub-threshold slope coefficient, $C_{ox}$is the gate oxide capacitance.

Band-to-Band-Tunneling is small and can be ignored and sub-threshold leakage current and gate tunneling leakage currents is taken into measure.

Priority Encoder

Priority as the name suggests means something that is more important than other and should be dealt with first (high /low priority). Priority Encoder does the same thing, whose way of providing output is similar to simple encoder with one advantage of selecting the operation with the priority function. With this facility of priority function, the input having highest priority is served first whenever choice has to make among more than one output.

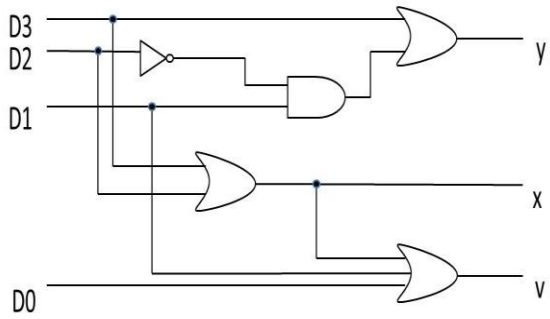


Fig.2 Circuit diagram of Priority Encoder

As we construct SG FinFET by shorting two P-types MOSFET and two N-type MOSFET to form P-type and N-type FinFET respectively. The Priority Encoder is realized using the virtuoso tool of cadence. The spectra simulator of cadence is used to simulate the output. The gate of two PMOS or NMOS transistors are connected together to formed a FinFET like structure. Then FinFET using Priority encoder circuit is firstly simulated without any technique and then with MTCMOS technique by applying different voltages such as 0.5 V, 0.6 V 0.7V and 0.8 V respectively at 45 nm technology.

V. SIMULATION AND RESULT

In this section, we present the comparison between FinFET based Priority Encode with MTCMOS technique and simple FinFET based Priority Encoder under Different Voltages at 45 nm technology from Virtuoso tools of Cadence. In this analysis we observed that Average Power, Leakage Power and Leakage Current of FinFET based Priority Encoder with MTCMOS technique is decrease in comparison with FinFET based Priority Encode without any technique and this is shown in the table number 1.

TABLE1. Results of Priority Encoder without MTCMOS technique

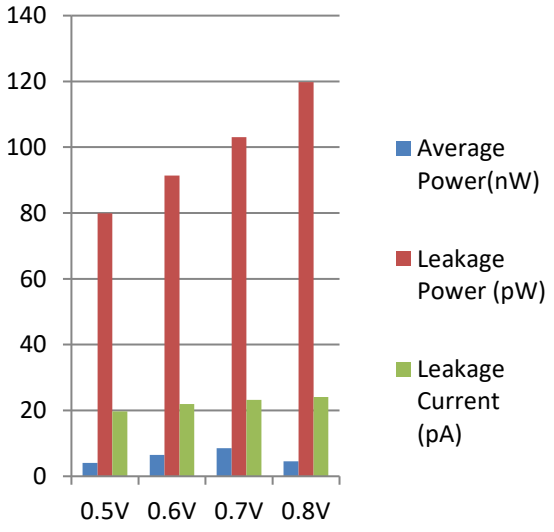
Voltage	Priority Encoder without MTCMOS Technique		
	Average Power (nW)	Leakage Power (pW)	Leakage Current (pA)
0.5V	5.368	94.35	20.97
0.6V	7.864	104.76	25.86
0.7V	11.04	117.07	28.39
0.8V	12.49	132.8	30.08

TABLE2. Result of Priority Encoder using MTCMOS technique

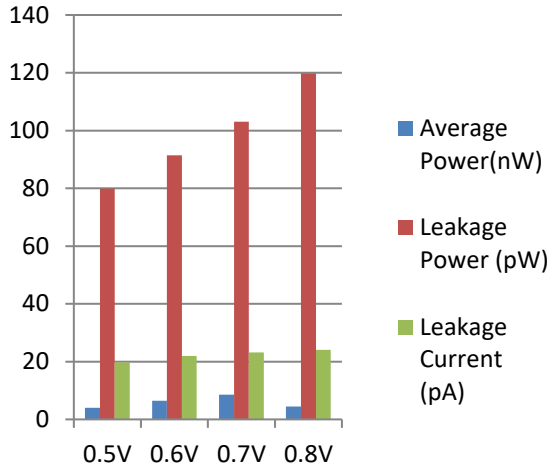
Voltage	Priority Encoder with MTCMOS Technique		
	Average Power (nW)	Leakage Power (pW)	Leakage Current (pA)
0.5V	4.032	79.95	19.71
0.6V	6.499	91.4	21.96
0.7V	8.56	103.1	23.19
0.8V	10.61	119.8	24.08

VI. CONCLUSION

There has become a vicious circle of supply voltage VDD, threshold voltage Vt, power dissipation and sub-threshold current but to judiciously utilize low Vt and high Vt devices so as not to compromise between low leakage and performance MTCMOS comes into picture. It is one of the techniques to reduce the standby leakage but now days run time leakages are also not negotiable, they do also contribute a significant part in leakage and degradation of performance of device. It has been observed that the Priority Encoder using MTCMOS technique gave efficient results as compared to the simple conventional one. Among all the supply voltages of 0.5V, 0.6V, 0.7V and 0.8V, 0.5V gave the best results of all.



Graph1.Comparison of Leakage Parameter of Priority Encoder using MTCMOS



Graph2. Comparison of Leakage Parameter of Priority Encoder without MTCMOS

ACKNOWLEDGEMENT

This work has been supported by ITM University, Gwalior along with the calibration cadence design system, Bangalore for providing the tools and technology for the work to be completed.

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