

A Review On Low Power Operational Amplifier

Priyanshi Dhupiya¹, Prof. UBS Chandrawat ²

^{1,2}Dept of Electronics & Communication

^{1,2}AITR Indore

Abstract- *The Operational Amplifier (OA) is the basic building block in any analog - mixed signal system. The architecture of the operational amplifier plays a vital role in designing low voltage, low power integrated circuits. The challenge lies in designing IC with reduced supply voltage and power to realize portable equipment with a minimum number of battery cells and a longer life period. This manuscript depicts the review of existing designs for low power two stage operational amplifier using miller compensation technique to increase the voltage gain. A comparative analysis is also shown in this paper.*

Keywords- OPAMP, Miller Compensation, Gain, Bandwidth.

I. INTRODUCTION

The operational amplifier is undeniably one of the most advantageous maneuvers in analog electronic circuitry. Op-amps are fabricated with massively dissimilar levels of intricacy to be used to grasp functions fluctuating from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the utmost broadly used electronic devices nowadays, being used in a vast array of customer, engineering, and technical devices. Operational Amplifiers, more frequently known as op-amps, are among the most extensively used edifice blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. [1, 2]

Op-amps are linear expedients which has closely all the belongings mandatory for not only ideal DC intensification but is used expansively for signal conditioning, filtering and for execution mathematical operations such as addition, subtraction, integration, differentiation etc. Generally an Operational Amplifier is a 3-terminal device. It contains chiefly of an Inverting input represented by a negative sign, ("-") and the other a Non-inverting input designated by a positive sign ("+") in the symbol for op-amp. Both these inputs have very high impedance. The output signal of an Operational Amplifier is the extravagant difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier [3].

A perfect operational amplifier having a single ended out is portrayed by a differential input, infinite voltage increase, interminable input resistance and zero output obstruction. In a genuine operational amplifier anyway, these

characters can't be produced however their execution must be adequately useful for the circuit conduct to firmly rough the characters of a perfect operational amplifier in many applications. With the presentation of each new age of CMOS advancements structure of op-amp keeps on acting further difficulties like the supply voltages and transistor channel lengths downsize.

In this paper, three stage RC miller compensated op-amp is compared with another similar op-amp which uses double cascade telescopic input in the first stage and common source amplifier in the second stage. Also the load capacitor improves the phase margin of the Miller compensated op-amp.

II. LITERATURE REVIEW

Priyanka Kakoty et. al. [4], a technique is offered in this paper for the proposal of a high frequency CMOS operational amplifier (Op-Amp) which operates at 3V power supply using TSMC 0.18 micron CMOS technology. The Op-Amp designed is a two-stage CMOS Op-Amp trailed by an output buffer. This Operational Transconductance Amplifier (OTA) pays a Miller capacitor and is remunerated with a current buffer compensation technique. Design has been agreed out in Tanner tools. Simulation results are verified using S-edit and W-edit.

J. Mahattanakul [5], the intention technique of the two-stage CMOS operational amplifiers retaining Miller capacitor in combination with the common-gate current buffer is presented.

R. Chatterjee et. al. [6], in this manuscript a CMOS two stage operational amplifier has been discussed which operates at 2.5 V power supply at 0.18 micron (i.e., 180 nm) technology and whose input is be contingent on Bias Current. The supply voltage has been scaled down to reduce overall power depletion of the system.

N Sachdeva et. al. [7], with the incessant emergent development towards the condensed supply voltage and transistor channel length, designing of high performance analog integrated circuits such as operational amplifier in CMOS (complementary metal oxide semiconductor) technology develops more perilous. In this research, the two stage CMOS Operational amplifier (op-amp) has been

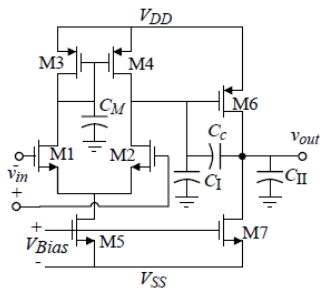


Figure 3: Miller compensated two stage op amp

VI. COMPENSATION TECHNIQUE

Operational amplifiers are generally used in a negative feedback configuration. In this way the relatively high, inaccurate forward gain can be used with feedback to achieve a very accurate transfer function that is a function of the feedback elements only [11]. To achieve the stable operation of op amps, compensation techniques are used. There are three types of compensation techniques, which are discussed as follows:

1. Miller Compensation - Usage of a capacitor feeding back around a high-gain, inverting stage.
 - a. Miller capacitor only
 - b. Miller capacitor with a unity-gain buffer to block the forward path through the compensation capacitor. It can eliminate the RHP zero.
 - c. Miller with a nulling resistor. Analogous to miller but with an additional series resistance to gain control over the RHP zero.
2. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.
3. Self-Compensating - Load capacitor compensates the op amp.

V. CONCLUSIONS

Here, we have reported the review of a low power op-amp topology. On the basis of above literatures low power operational amplifier can be implemented using 45 nm technology or below this technology like 25 nm, 22 nm etc. We can reduce the power supply voltage for the operational amplifier or use of 4 terminal CMOS can reduce the power. According to the above manuscript, the proposed design will be implemented using Tanner EDA tool.

REFERENCES

- [1] W. T. Holman, J. A. Connelly, J. O. Perez, "A Low Noise Operational Amplifier in a 1.2 μ M Digital Technology", IEEE Journal 2007

- [2] Maryam Borhani, Farhad Razaghian, "Low Power Op-Amp Based on Weak Inversion with Miller-Cascoded Frequency Compensation", IEEE Journal 2009.
- [3] Ming-Dou Ker; Jung-Sheng Chen, "Impact of MOSFET Gate-Oxide Reliability on CMOS Operational Amplifier in a 130-nm Low-Voltage Process", IEEE Journal 2008.
- [4] P. Kakoty, "Design of a High Frequency Low Voltage CMOS Operational Amplifier, International Journal of VLSI Designs Communication Systems 2 (2011), no. 1.
- [5] J. Mahattanakul, "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer", IEEE Transaction on Circuits and System II 52 (2005), no. 11, 1057-7130.
- [6] R. Chatterjee, S. Bandyopadhyay, D. Mukherjee, "Design of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power And High CMRR", Int. Journal of Recent Trends In Engineering Technology 2 (2014), 134- 155.
- [7] N. Sachdeva S. Goyal and T. Sachdeva, "Analysis and Design of a Two Stage CMOS Op-Amp with 180nm Using Miller Compensation Technique", International Journal on Recent and Innovation Trends in Computing and Communication 3 (2015), 2255-2260.
- [8] D. J. Moni, D.S. Shylu and B. Kooran, "Design and Analysis of a Two Stage Miller Compensated Op-Amp Suitable For ADC Applications", International Journal of Research in Engineering and Technology 3 (2014), no. 7, 2321- 7308.
- [9] K. A. Shah P. D. Patel, "Design of Low Power Two Stage CMOS Operational Amplifier", International Journal of Science and Research (IJSR) 2 (2013), no. 3, 2319-7064.
- [10] Manash Pratim Sarma, Nilotpal Kalita, Nikos E. Mastorakis "Design of an Low Power Miller Compensated Two Stage OP-AMP using 45 nm Technology for High Data Rate Communication", 4th International Conference on Signal Processing and Integrated Networks (SPIN), IEEE 2017
- [11] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design", 1st Indian Edition, Oxford University Press, 2010