Design Of Low Power Three Stage Miller Compensated Operational Amplifier Using 25nm Technology

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Abstract- *This manuscript depicts the implementation of new design for low power three stage operational amplifier using miller compensation technique to increase the voltage gain. Here the circuit is designed and simulated by Tanner EDA tool using 25 nm CMOS technology. A substantial increase in DC gain and Unity gain bandwidth is obtained. A comparative analysis is shown in this paper to found the effectiveness of the design.*

Keywords- OPAMP, UGB, Tanner, CMOS

I. INTRODUCTION

The complexity of integrated circuit is continuously increasing, with time. This is primarily due to the rising performance of new generation MOS transistors. The reduction in component sizing is one of the prime reasons for integrating millions of transistors into a single chip. There is a great demand for battery powered equipment like laptop, wireless communication and implantable devices. In all these devices, it is essential to maintain low power dissipation to achieve good battery life and weight. Hence, designing high performance analog circuits with reduced supply voltage and low power continues to remain a challenge. The advancement in process technology also increases the complexity in designing the integrated circuits (IC). Hence, in all modern electronic systems, low power and low voltage circuit techniques are in demand today.

In telecommunications, wireless communication can be used to transfer information over short distances (a few meters as in television remote control) or long distances (thousands or millions of kilometers for radio communications). The term is often shortened to "wireless". It comprehends numerous kinds of fixed, mobile, and handy two-way radios, cellular handsets, personal digital assistants (PDAs), and wireless networking. RF (radio frequency) is a circuit design that operates in a range of electromagnetic frequencies above the audio range and below the visible light. All broadcast transmission, from AM radio to satellites, falls within a range of 30 kHz to 300 GHz. Several wireless devices make usage of RF fields: radio, television, cordless headsets, cell phones, satellite communication structures, quantifying and instrumentation manufacturing systems. In all these systems, the signals are received through the front end architecture of the RF wireless receiver.

The two stage op-amp contains of a telescopic op-amp phase and a common source output rail-to-rail phase. Conniving of high speed op-amp is the stimulating part of the pipelined ADC. As per Liang and Gulati, the main bottleneck is that there is a tradeoff between speed and gain, because high dc gain demands a multistage design with long channel devices and a low bias current intensities, while the high speed demands single stage design, short channel devices and a high bias current levels [1-2]. The telescopic op-amp is mainly used because of its simplicity over other circuit designs and it allows high speed operation and low power consumption. The op-amp circuit uses RC Miller recompense in order to attain maximum bandwidth and stability. To attain great gain and high bandwidth the well-known differential topology is used. The main advantage of the differential topology is the higher immunity towards the environmental noise.

In this paper, three stage RC miller compensated op-amp is designed and compared with another similar op-amp which uses double cascade telescopic input in the first stage and common source amplifier in the second stage. As per Nagaraj, the op-amp with double cascade telescopic input provides low output resistance and minimum output signal loss [3]. Also the load capacitor improves the phase margin of the Miller compensated op-amp.

II. OPERATIONAL AMPLIFIERS

The operational amplifier, which has become one of the most multipurpose and significant building blocks in analog circuit design. An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with a rather high gain. In utmost universal tenacity op-amps there is a single ended output. Generally an op-amp generates an output voltage a million times larger than the

voltage difference athwart its two input terminals. For best universal applications of an op-amp a negative feedback is used to govern the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed-loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal opamp is considered by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier.

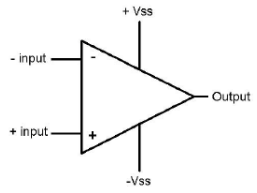
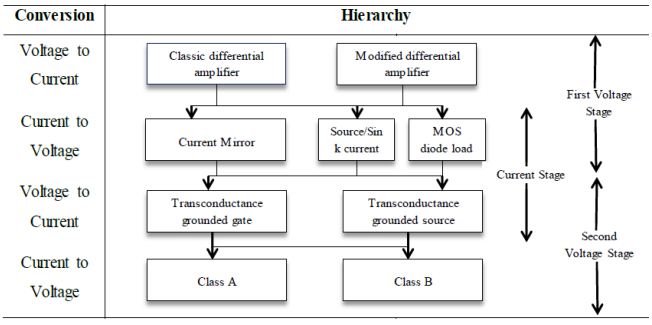


Figure 1: General purpose opamp

An perfect Operational Amplifier is a 3-terminal linear device. It consists of two input terminals with very high impedance. Basically the Operational Amplifier output signal is nothing but the difference of the two input signals being applied at the high impedance terminals magnified by a constant gain [4].

In order to understand the design of CMOS op amps it is worthwhile to examine their classification and categorization. Table 1 explains the classification in detail.

Table 1: Categorization of CMOS Op Amps



The full op-amp schematic designed using the previous designed current mirror and differential amplifiers and the common source amplifier circuit is as shown in figure 2 below:

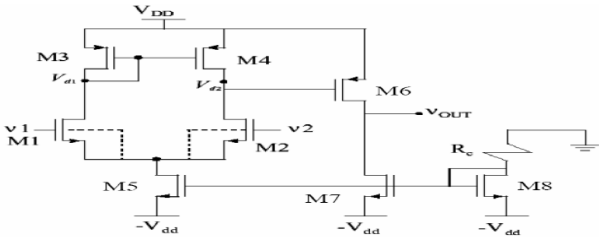


Figure 2: Block diagram for practical operational amplifier

III. DESIGN SPECIFICATION

The designing of op amps can be divided into two distinct design-related activities that are for the most independent of one another. The first of these activities involves choosing or creating the basic structure of the op amps. Once the structure has been selected, the designer must select dc currents and begin to size the transistors and design the compensation circuit. Most of the work involved in completing the design is associated with this second work [5].

Typical Specification	**Design Factors**
DC Gain (Av)	Frequency Response
Unity Gain Bandwidth	Phase Margin
Power Dissipation	Load Capacitance
Slew Rate	Compensation
Input Offset Voltage	Device Dimensions
Output Voltage Swing	
CMRR	

Specifications	
Open loop Gain	40 dB
Gain B/W at -3 db gain	5 MHz
Load Capacitance (CL)	10 pf
Slew Rate	10 V/Us
Mirror Pole kept at	>=10GB
Maximum Power Dissipation	≤ 2mw
Phase Margin	>=60
Channel Length	22 nm
CMRR	>=60 dB
PSRR	>=60 dB
Power Supply	0.8 Volt

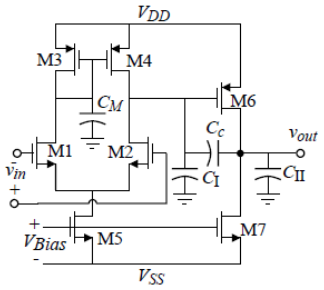


Figure 3: Miller compensated two stage op amp

IV. SIMULATION AND RESULTS

The designed op-amp was simulated to find the different characteristics of the designed op-amp. Further the layout of the designed op-amp was created and the parasitic capacitance and resistance was extracted.

The following table represents the value of parameters taken for the simulation of three stage opamp.

Table 2: Design specifications used

Parameter	Expected
Open loop Gain	40 dB
Unity Gain BW	50 MHz
Load Capacitance (CL)	10 pF
Phase Margin	>=60
Channel Length	25 nm
Power Supply	1.5 Volt

Table 3: Design parameters used

		Region	W	L
M1	NMOS	SAT	62	0.1
M2	NMOS	SAT	62	0.1
M3	PMOS	SAT	5	0.1
M4	PMOS	SAT	5	0.1
M5	PMOS	SAT	24.55	0.2
M6	NMOS	SAT	2.4	0.2
M7	NMOS	SAT	1	0.4
M8	NMOS	SAT	0.6	0.2
M9	NMOS	SAT	8	0.2
M10	NMOS	SAT	8	0.2
M11	PMOS	SAT	35	0.2
M12	PMOS	SAT	35	0.2
Mb	NMOS	SUB	1	0.2

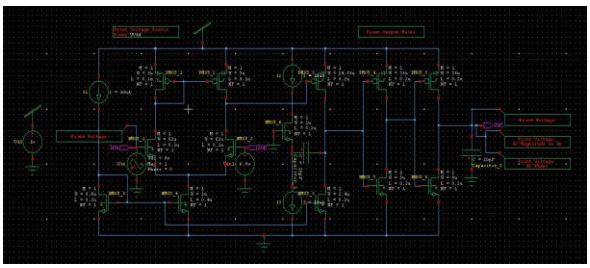


Figure 4: Schematic of three stage op amp

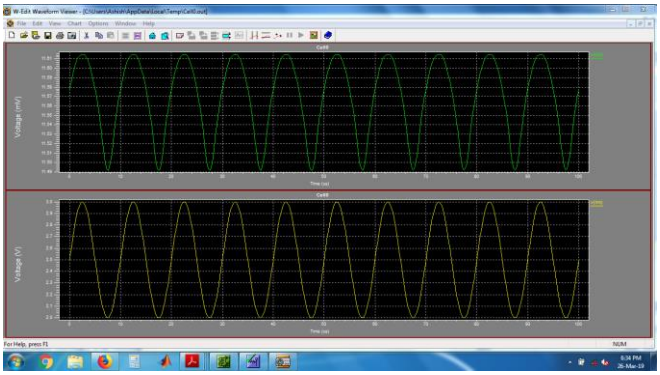


Figure 5: Result of transient Analysis

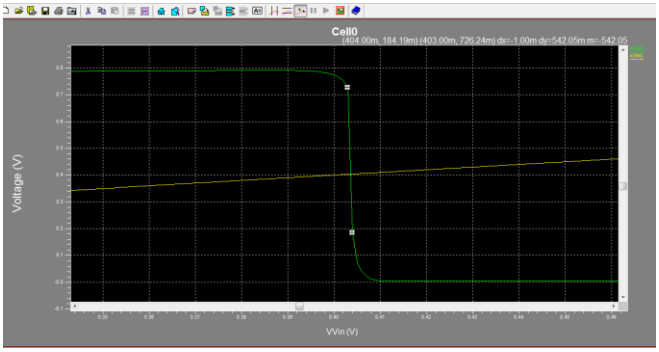


Figure 6: Result of DC Analysis

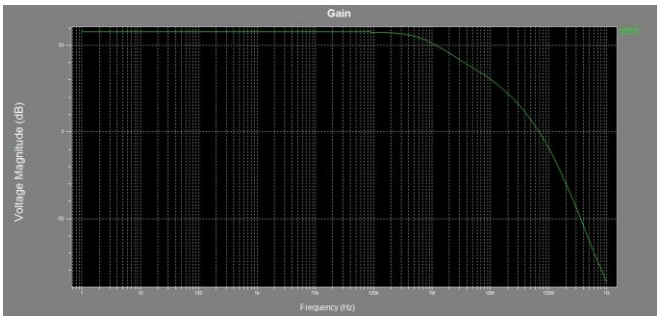


Figure 7: Magnitude Graph

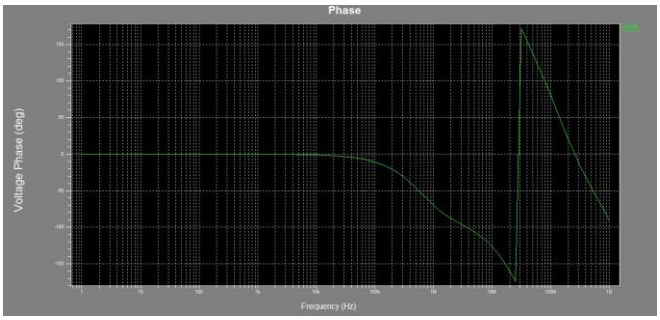


Figure 8: Phase Plot

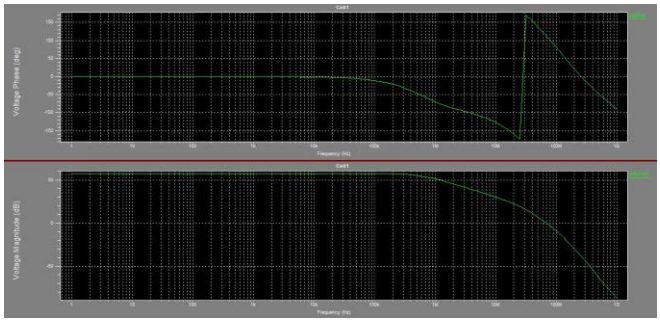


Figure 9: Combined Graph of Magnitude and Phase

Table 4: Comparison between various literatures

Parameters	[6]	[7]	[8]	[9]	[10]	[11]	[5]	Proposed
Tech (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.045	0.025
V_{dd} (V)	3	2.5	2.5	1.1	1.8	1.8	1	1
DC Gain (dB)	49	81	36.7	48.27	60	55.5	49.15	57.86
Phase Margin (degree)	60	65	48.1	86.4	50	60	60.4	40.1
Power (µW)	396	378	804	-	1.03m	300	70	676
Unity Gain (MHz)	477	5	16.5	11.2	26.02	12.6	533.1	70.78M

The above table shows the simulation results of implementation of proposed design. For transient analysis stop time taken is 10^5 ns, while the masimum step size is 100 ns. For AC analysis, stop frequency is 1 GHz with number of frequency is 10 on decade scale. Our simulated results shows better DC gain for 1V V_{DD} on 25 nm technology.

V. CONCLUSIONS

Here, we have reported the plan of a low power op-amp topology simulated utilizing Tanner EDA device that gives a huge decrease in power prerequisite and increases the gain bandwidth product extensively than recently revealed works. The structure is done utilizing 25 nm technology and shows better solidness. Further, from the transient response, clearly the proposed plan has a stability low latency in achieving the required threshold. It makes the proposed structure reasonable for high data rate communication. The proposed design has been able to satisfy most of the specifications provided for the op-amp. The proposed op-amp is a three stage single output op-amp.

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