Analysing The performance of Low Power High Speed Full Adders Using Strained Silicon CMOS Technology

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Abstract- *In most of the digital circuits, communication systems and digital signal processing, Adders play a major role since they are the basic blocks. In this paper, the performance of full-adder (FA) circuits has been studied. The full adder circuits were designed using 22 nm Strained Silicon CMOS Technology. The circuits are analyzed in terms of power consumption and delay. To analyze the full adder circuits, we have used Spice tools. The power consumption and delay varies with respect to temperature. These full adder circuits are analyzed with a power supply of 0.8 V.*

Keywords- Delay, Full-adder (FA), Power consumption.

I. INTRODUCTION

TODAY, electronic systems have become an in-separable part of our day-to-day life. Digital circuits such as microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As the technology develops the scale of integration keeps on increasing hence the usability of such digital circuits is restricted by the amount of area and power consumption. Arithmetic operations play a vital role in various digital systems. Adders are the basic logic circuits used to perform various arithmetic operations such as addition, subtraction, multiplication and division. The fast and accurate operation of a digital system depends upon the performance of the adder. Hence it is essential to design adder with less area and low power consumption. The adders are found not only in Arithmetic Logic Unit but also in various computer processors. The adders can be used to design various high speed multipliers for high performance applications.

In this paper various full-adder circuits has been designed and simulated. Their simulation results has been analysed and verified. The delay and power consumption of these proposed full-adder circuits has been investigated. It is found that the delay and power consumption varies with respect to temperature, such that the delay increases with increases in temperature and power decreases with increase in temperature. The power supply used for the simulation of these various full-adder circuits is 0.8V. The simulation is performed using the Spice tools. The simulation result of these full-adder circuits are analysed to determine their delay and power consumption.

The delay and power analysis of these various full-adder circuits are compared to determine the efficient full-adder. Since, delay and power consumption varies with respect to temperature; delay and power are always indirectly proportional to each other.

II. 20-T HYBRID FULL-ADDER (HFA-20T)

This hyrid full-adder circuit consists of 20 transistors. Out of those 20 transistors, some transistors are used as pass transistor model. It consists of 3 inputs and 2 outputs (SUM and Cout). The simulation is performed to analyze the full-adder circuit. High dc-signals are used. Fig. 1 shows the schematic diagram of 20-T HFA.

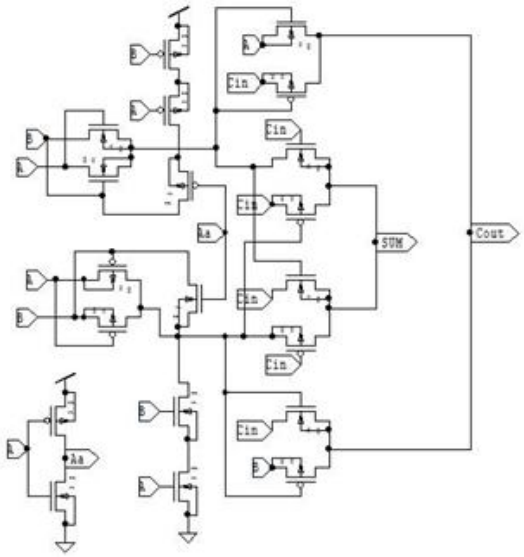

Fig. 1: 20-T Hybrid Full-Adder

The input and output waveforms for the 20-T HFA circuit is shown in Fig. 2.

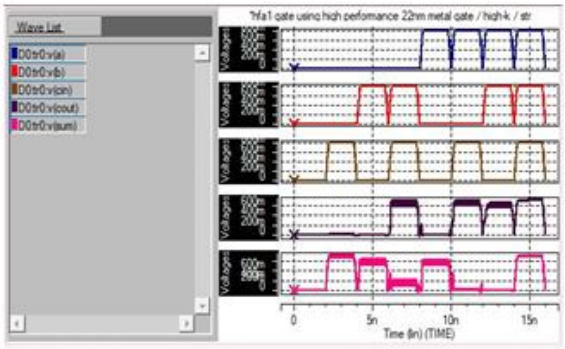

Fig. 2: Simulation results of 20-T Hybrid Full-Adder

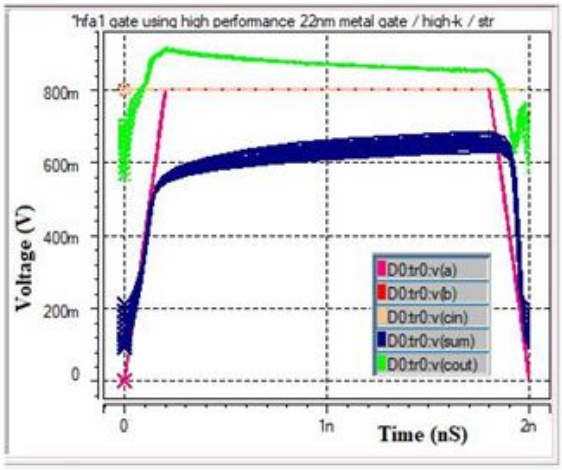

Fig. 3: The delay anlysis

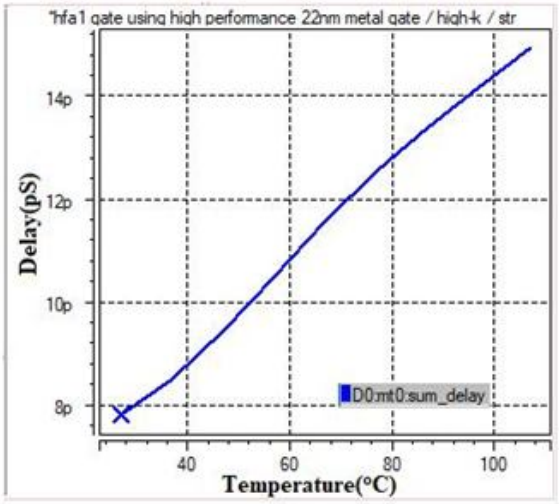

Fig. 4: Delay versus temperature analysis of 20-T Hybrid Full-Adder

The input signal A is triggered and input signnal B and Cin are taken as high dc signals. The signal varies with respect to temperatue. It is found that the delay increases as the temperature increases. The delay analysis result is represented in fig.3. Fig. 4 plots the variation of delay with temperature and from this plot it is clar that the delay of the 20-T HFA circuit increass with increase in temperature. This may be due the reduction of effective power consumption because of the increase in thermal leakage. The analysis shows that the power decreases as the temperature and delay increases. The output is represented in fig.5. From Fig. 5 it is understood that the effective power consumption of the 20-T HFA circuit decreases with increase in temperature.

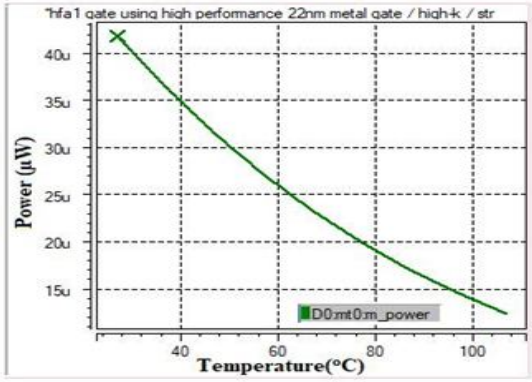

Fig.5:Power Analysis of 20-T Hybrid Full-Adder

III. 17-T HYBRID FULL-ADDER (HFA-17T)

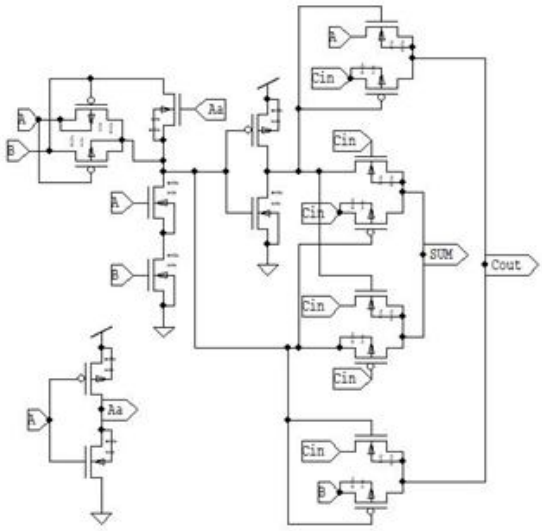

Fig. 6: 17-T HYBRID FULL-ADDER

The hyrid full-adder circuit shown in Fig. 6 consists of 17 transistors. Out of those 17 transistors, some transistors are used as pass transistor model. It consists of 3 inputs and 2 outputs (SUM and Cout). The simulations were performed at 300 K to analyze the full-adder circuit.

IV. 26-T HYBRID FULL-ADDER (HFA-26T) TYPE-I

The Type-I hyrid full-adder circuit (Fig. 7) consists of 26 transistors. Out of those 26 transistors, some transistors

are used as pass transistor model. It consists of 3 inputs and 2 outputs (SUM and Cout). The simulation is performed to analyze the full-adder circuit.

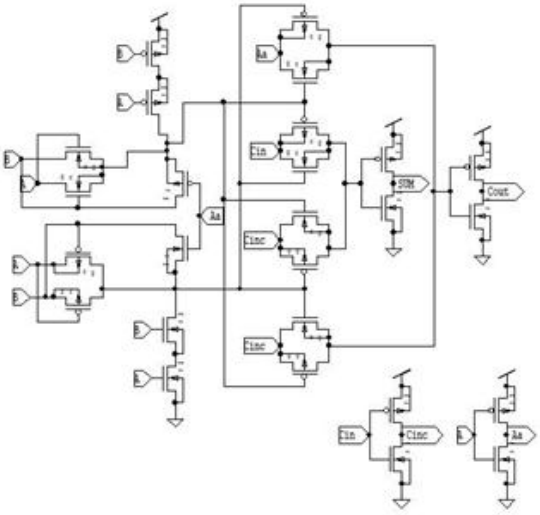

Fig. 7: 26-T HYBRID FULL-ADDER TYPE-I

V. 26-T HYBRID FULL-ADDER (HFA-26T) TYPE-II

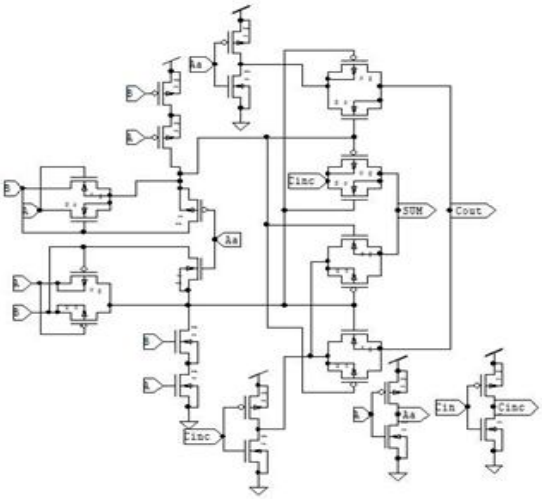

Fig. 8: 26-T HYBRID FULL-ADDER TYPE-II

The Type-II hyrid full-adder circuit shown in Fig. 8 consists of 26 transistors. Among all the 26 transistors, some transistors are used as pass transistors. It consists of 3 inputs and 2 outputs (SUM and Cout). The simulation is performed to analyze the full-adder circuit. High dc-signals are used.

VI. 22-T HYBRID FULL-ADDER (HFA-22T)

The 22-T hyrid full-adder circuit has the advantage of less area consumption in the chip because of the minimum number of transistors compard to the above discussed hybrid full adder architectures. The circuit diagram of 22-T HFA is shown in Fig. 9.

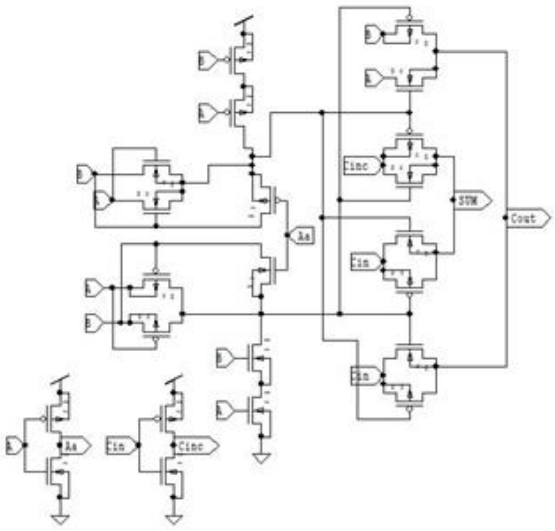

Fig. 9. 22-T HYBRID FULL-ADDER

VII. 19-T HYBRID FULL-ADDER (HFA-19T)

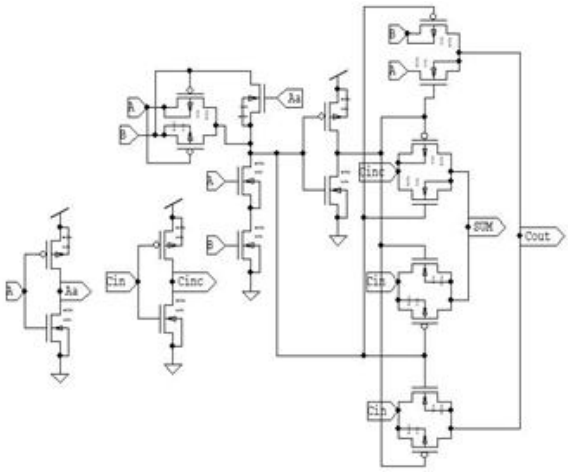

Fig. 10: 19-T HYBRID FULL-ADDER

The hyrid full-adder circuit shown in Fig. 10 consists of 19 transistors. This hybrid full adder has the least number of transistors compard to all other types of hybrid full adders discussed in this paper. Since it uses minimum number of transistors, it has the advantages of less chip area and low power consumption.

VIII. COMPARISON

Various Full-Adder circuits are simulated and analyzed their delay and power consumption. The simulation

analysis is displayed in the following table represented as TABLE I

TABLE I COMPARISION BETWEEN VARIOUS FULL-ADDER CIRCUITS

HYBRID FULL-ADDER	DELAY (S)	POWER (W)
HFA-20T	$14.944*10^{-12}$	$12.303*10^{-6}$
HFA-17T	$50.292*10^{-12}$	$13.777*10^{-6}$
HFA-26T TYPE-I	$21.069*10^{-12}$	$9.84892*10^{-6}$
HFA-26T TYPE-II	$53.373*10^{-12}$	$14.965*10^{-6}$
HFA-22T	$41.231*10^{-12}$	$16.614*10^{-6}$
HFA-19T	$52.168*10^{-12}$	$38.334*10^{-6}$

IX. CONCLUSION

Adders play an important role in various digital circuits. It is essential to design an efficient full-adder circuit with low power consumption. In this paper, various hybrid full-adder circuits has been designed and simulated using SPICE tools. The HFA circuits were designed using 22 nm strained silicon CMOS technology with a power supply of 0.8 V and the SPICE simulations were carried out at 300 K temperature. Finally, in order to investigate the influence of temperature on the circuit performance, temperature was swept from 30^0C to 110^0C with a step of 10^0C. These adders are considered to be the most suitable full adder circuits for future VLSI processors and DSP applications.

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