High Performance Partial Product Binary To Decimal (PPBD) Converter Based Multiplier

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Abstract- *Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Multipliers are vital components of any processor or computing machine. Hence better multiplier architectures are bound to increase the efficiency of the system. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. Throughput is the measure of how many multiplications can be performed in a given period of time. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. High Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier is one such promising solution. The designing can done using VERILOG and simulated, synthesized using Questa-sim.*

I. INTRODUCTION

The main objective of this paper is to design and implement a High-Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier using fast binary to BCD converter, which can be used in the application of any processor. A novel technique of High-Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier which is quite different from the conventional method of multiplication. Verilog HDL is used for the design of High-Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier, since this gives an effective utilization of structural method of modelling.

II. LITERATURE SURVEY

2.1 Multipliers

Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm

2.2 Array Multiplier

The computation time taken by the array multiplier is comparatively less because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array

2.3 Booth Multiplier

Booth multiplication is another important multiplication algorithm. Large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. Multiplication of two n-bit operands using a radix-4 booth recording multiplier requires approximately n / (2m) clock cycles to generate the least significant half of the final product, where m is the number of Booth recorder adder stages

III. PROPOSED HIGH-PERFORMANCE PARTIAL PRODUCT BINARY TO DECIMAL (PPBD) CONVERTER BASED MULTIPLIER

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. In Computer Science where more accurate data processing is demanded, decimal arithmetic plays an important role to support the most accurate data processing at the level of financial and scientific calculations where errors aren't acceptable at all. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having trade-off in terms of speed, circuit complexity, area and power consumption. Research in decimal systems has recently received renewed interest with great attention being paid to decimal multiplication. Such attention is justified by the increasing diffusion of embedded systems in everyday life application, where both tradition and legal constraints require a decimal arithmetic. A generalized design approach andarchitectural framework for the High Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier is shown in Fig 1.

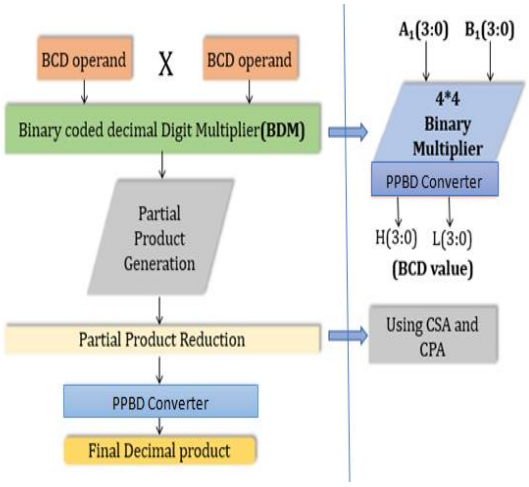

Fig 1. Block Diagram

The High Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier have the following stages:

(i) Partial product generation,
(ii) Partial product reduction, and
(iii) Final product computation.

Multiplication of digit A1 of the multiplicand with the digit B1 of multiplier has performed using the Partial Product Binary to Decimal (PPBD) Converter. Multiplication of A1 and B1 have been highlighted in Fig 2.

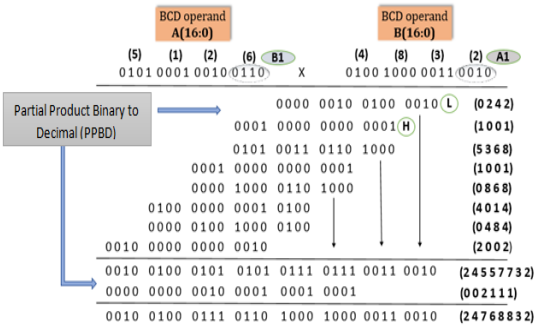

Fig 2. PPBD Model

The proposed PPBD converter, is designed using the fast BD (FBD) converter cells. The FBD cell, would accept a 4-bit binary input (bj), multiplies it by four, and then adds it to bi of 2-bits. The BDM Converter is employed in two different stages (for arrangement of Partial Product Generation, and reduction stages) of multiplicationprocess to convert the binary value into BCD value. The proposed BDM Converter is a combination of a conventional 4*4 Binary Multiplier and a Partial Product Binary-to-Decimal (PPBD) converter is shown in Fig 3.

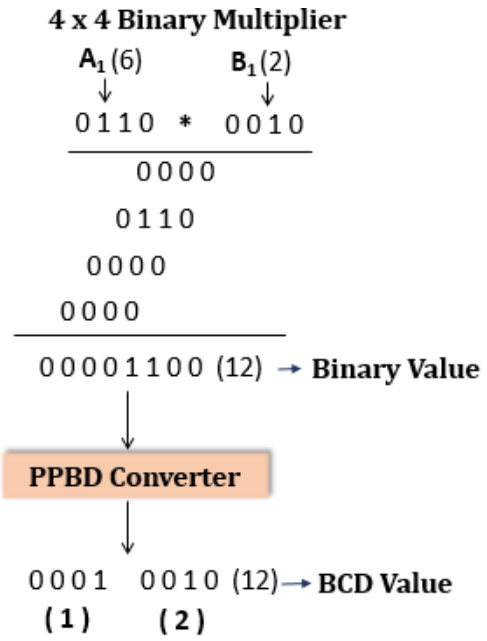

Fig 3. BCD Digit Multiplier (BDM)

The conversion from binary-to-decimal is carried out using Partial Product Binary to Decimal (PPBD) converters resulting in rows of decimal digits which are eventually compressed using a decimal adder to obtain the final product. The BCD is a binary coded decimal number, they are presented by their equivalent binary numbers.

VI. RESULTS

The High Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplier is implemented using Verilog HDL. The results are simulated using Questa – Sim.

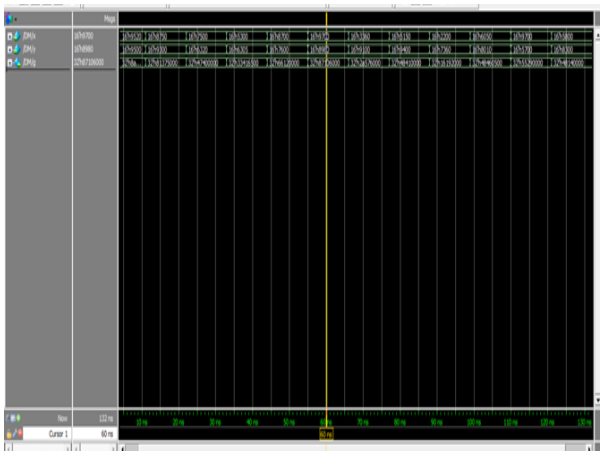

Fig 4. Simulation Output of the Proposed Design.

The RTL schematic of the proposed design High Performance Partial ProductBinary to Decimal (PPBD)

Converter based Multiplier extracted using Questa - SimEncounter file are shown in Fig. 5.

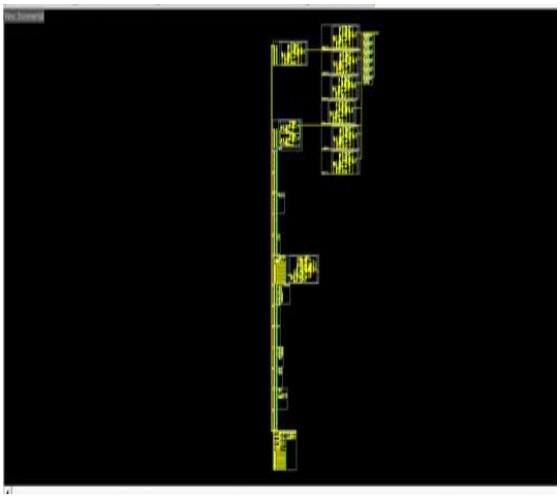

Fig 5. RTL Schematic of the Proposed Design.

The RTL schematic of the proposed design Partial Product Binary to Decimal (PPBD) Multiplier extracted using Questa - SimEncounter file are shown in Fig.6.

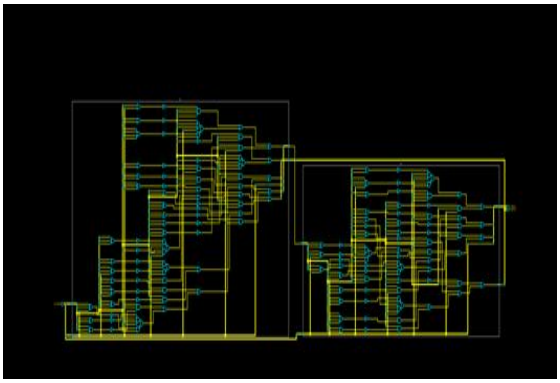

Fig 6. RTL Schematic of the Proposed PPBD Design.

V. CONCLUSION

In this paper the High-Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplieris discussed and simulated using Questa – Sim. Due to its parallel structure it is concluded that the High-Performance Partial Product Binary to Decimal (PPBD) Converter based Multiplieris better than conventional.

VI. FUTURE SCOPE

The computational speed drastically reduces if all these methods are effectively used for the hardware implementation. By using these Multiplication, world can achieve new heights of performance and quality for the cutting-edge technology device.

REFERENCE

[1] G. Jaberipur, A. Kaivani, Binary-coded decimal digit multipliers, IET Comput. Digit. Tech. (Vol:1, Issue:4), (2007).
[2] S. Gorgin, G. Jaberipur, R. HashemiAsl, Efficient ASIC and FPGA implementation of binary-coded decimal digit multipliers, Circuits, Syst., Signal Process. (Vol:33, Issue:12), (2014).
[3] L. Dadda, Multi-operand parallel decimal adder: a mixed binary and BCD approach, IEEE Trans. Comput. (Vol:56, Issue:10), (2007).
[4] L. Dadda, Some schemes for parallel multipliers, Alta Freq. (Vol:34, Issue:5), (1965).
[5] J.-D. Nicoud, Iterative arrays for Radix conversion, IEEE Trans. Comput. (Vol:20, Issue:12), (1971).
[6] M.S. Schmookler, A.Weinberger, High speed decimal addition, IEEE Trans. Comput. (Vol:20, Issue:8), (1971).