Temperature sensitivity of Band gap Reference Generator Using Two Stage Operational Transconductance Amplifier

MelroyPinto[1], Carl Fernandes[2], Komal Shinde[3]
[1, 2, 3] Dept of Electronics and Telecommunications
[1, 2, 3] Don Bosco Institute of Technology, Mumbai

Abstract- *In this paper, we will provide a research on how a 2 stage Operational Transconductance Amplifier (OTA) provides a better and effective temperature sensitivity to a Bandgap Reference Generator (BRG). The BGR with a 2 Stage OTA gives a better temperature sensitivity as compared to a BGR with an open loop single stage operational amplifier (OPAMP) or a conventional 2 stage OPAMP. This has been studied and proven using proposed design and optimized using Plackett-Burman Design Method. The proposed design is simulated using NgSpice. We have demonstrated that the temperature sensitivity can be optimized using the Plackett-Burman Design Method by carrying out a pattern variation in process parameter (Threshold Voltage) and design parameter (Width and Length of MOSFET).*

Keywords- Operational Transconductance Amplifier, Plackett-Burman Design, OTA, BRG, temperature sensitivity

I. INTRODUCTION

Bandgap Reference Generator is an essential element in many analog and mixed signal systems. A BRG must be highly structured and should produce extremely minimal changes to power supply variations and temperature variations. Reference Voltage limits the accuracy of many analog circuits such as voltage regulators, DAC, ADC etc. Hence in order to have high performance metrics such as a low temperature coefficient, high power supply rejection ratio, temperature range for effective operation etc; a good BRG is required.

A typical BRG has an output voltage around 1.25V, close to the theoretical 1.22 eV bandgap of silicon at 0 K. The basic schematic of how a reference voltage source is generated is displayed in Fig 1. The basic principle behind generation of a constant temperature dependant reference source which can be either voltage or current, is to add two different types of sources. Out of the two, one voltage source increments proportional to absolute temperature (PTAT) and the other increments with complementary proportional to absolute temperature (CTAT). As shown in Fig 1, the voltage across a forward biased p-n junction diode (V_f) exhibits the CTAT source. The voltage equivalent to temperature (V_t) shows the property of a PTAT source. But both these sources do not have the same temperature coefficient magnitude. Hence, in order to nullify the effect of V_f , V_t is multiplied by a constant factor 'K' and thus a voltage reference is procured.

The paper is structured as follows: Section II describes the operation of a conventional BRG. Section III describes the function of a 2 stage OTA and why it is preferred over a conventional amplifier. Section IV describes the design of a BRG using a 2-stage operational transconductance amplifier which has a better temperature stability as proved by the Plackett Burman Design methodology. The results are then further demonstrated based on process and design parameter variations. [1]

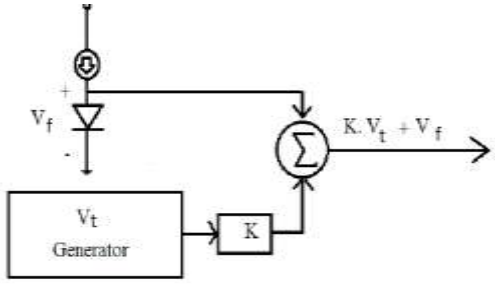

Fig. 1: Voltage Bandgap Reference Generator (Schematic)

II. BANDGAP REFERENCE GENERATOR (BRG)

A typical bandgap reference circuit is shown in Fig 2. In the circuit, the emitter area of Q2 is made larger than that of Q1 (by a ratio of 8 is to 1). When the voltage at their common base is small, so that the voltage drop across R2 is small, the larger area of Q2 causes it to conduct more of the total current available through R1. The variation or the imbalance created in the collector voltages drives the OPAMP to increase the base voltage. Alternatively, if the base voltage is high, forcing

a large current through R1, the voltage developed across R2 will limit current through Q2 so that it will be less than the current in Q1. The sense of the collector voltage imbalance will now be reversed, causing the OPAMP to reduce the base voltage.[3]Between these two extreme conditions is abase voltage at which the two collector currents match, toward which the op amp drives from any other condition. Assuming equal common base current transfer ratio for Q1 and Q2,this will occur when the emitter current densities are in theratio 8 - to - 1, the emitter area ratio.[6] When this difference in current density has been produced by the op amp, there will be a difference in V, between Q1 and Q2, which will appear across R2. This difference will be given by the expression

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{J_1}{J_2} \quad (1)$$

Now based on the above equation we can obtain the value ofΔV_{BE} . We know that the Vref we require is around 1.22V. Hence depending upon these requirements, we take anappropriate ratio of R1 to R2 to obtain that valueof Vref. We were successful in achieving a value of 1.038 Vfor R1 = 5.82 * R2, R2 = 1k,R3 = R4 = 1k.

III. TWO STAGE OPERATIONAL TRANSCONDUCATNCE AMPLIFIER (OTA)

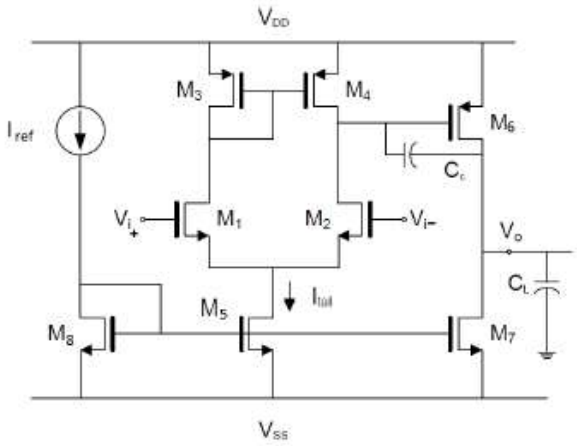

Figure 2. 2 Stage OTA

The 2 stage OTA shown in Fig.2 is designed for a gain of 5000-6000 with a tail current of 100 µA and Iref of 30 µA. The Input Common Mode Ratio (ICMR) is fixed for the range -1 V to 2 V. The design was carried out and appropriate values of W and L were obtained. [2]

The first stage in Fig.2 consists of a n-channel differential pair M1-M2 with an p-channel current mirror load M3-M4 and a n-channel tail current source M5. The second stage consists of an p-channel common-source amplifier M6 with a n-channel current-source load M7. Because the OP-AMP inputs area unit connected to the gates of MOS electronic transistor, the input resistance is essentially infinite when the OP-AMP is used in internal applications.

For identical reason, the input resistance of the second stage of the OP-AMP is also essentially infinite. The output resistance is that the resistance wanting back to the second stage with the OP-AMP inputs connected to tiny signal ground:

$$R_{out} = r_{o6} \parallel r_{07} \quad (2)$$

where Rout=output resistance and ro6 and ro7 are the internal resistance of transistor M6 and M7 respectively. Although this output resistance is sort of continually abundant larger than generally purpose bipolar OP-AMP, low output resistance is usually not required when driving purely capacitive loads. Since the input resistance of the second stage is essentially infinite, the voltage gain of the amplifier in Fig.2 can be found by considering thetwo stages separately. The overall Gain of the 2 Stage OTA is:

$$A_v = \frac{2gm_2 gm_6}{I_5(\lambda_4+\lambda_2)I_6(\lambda_7+\lambda_6)} \quad (3)$$

This high gain is used to achieve suppression that come in due to ripples in the power supply or high Power Supply Rejection Ratio (PSRR).

IV. ANALYSIS OF BRG USING TWO STAGE OPERATIONAL TRANSCONDUCTANCE AMLPIFIER

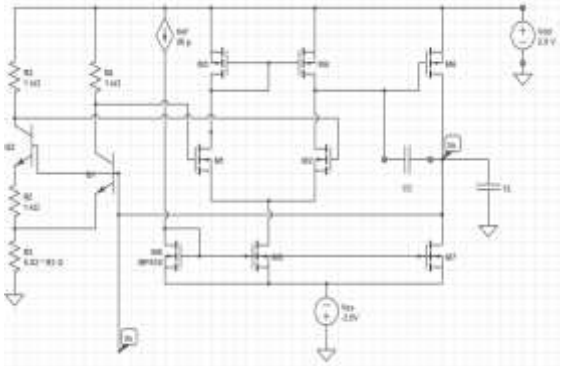

Fig 3. BRG using 2 Stage OTA

The Bandgap Reference Generator [4] shown in Fig.3 is constructed using the 2 stage OTA. In BRG using 2 stage OTA, the Vo (Output Voltage) is almost independent of temperature. Note: All transistors operate in the saturation

region. This circuit was simulated using NgSpice software. The Vref obtained was 1.038V with a temperature sensitivity of -54.42 mV/ºC . These values are highly identical to the absolute/theoretical values.

Now an analysis was carried out using Plackett Burman Design Methodology for optimization.

Table 1: Plackett-Burman DOE for 8 runs
P_1-P_2: Process Parameters, Y_1-Y_8: Responses

	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Y
1	+	+	+	-	+	-	-	Y_1
2	-	+	+	+	-	+	-	Y_2
3	-	-	+	+	+	-	+	Y_3
4	+	-	-	+	+	+	-	Y_4
5	-	+	-	-	+	+	+	Y_5
6	+	-	+	-	-	+	+	Y_6
7	+	+	-	+	-	-	+	Y_7
8	-	-	-	-	-	-	-	Y_8

The Plackett Burman Design Matrix [5] shown in Fig.4 is used for quantification of the impactof process variations on device responses such as Ion, Ioff, Iref etc. This helps to identify the most significant process parameters, which causes the variability in device and circuit performance. The Placket Burman Method or PB-DOE method as it is known, uses the orthogonal arrays to analyse the process parameter impact with minimum number of experimental runs. For example, with this method, N numbers of runs are required to estimate effects of (N-I) number of process parameters. A typical PB-DOE for 8 experimental runs with 7 process parameters is shown in Table 1. In this table, P1 to P7 indicates process parameters and "+" and "-"signs are used to represent the high-level and low-level values respectively of the corresponding process parameter. The rows in table represent the experimental run with corresponding values of the process parameter. The response or output of each experimental run is indicated by Y1 to Y8.

Table 2: Optimized Values of W/L

	M1	M2	M3	M4	M5	M6	M7	Y
1	3.3	3.3	16.5	13.5	4.95	84.6	12.6	-36.76
2	2.7	3.3	16.5	16.5	4.05	103.4	12.6	-41.88
3	2.7	2.7	16.5	16.5	4.95	84.6	15.4	-219.9
4	3.3	2.7	13.5	16.5	4.05	103.4	12.6	-248.2
5	2.7	3.3	13.5	13.5	4.95	103.4	15.4	-45.14
6	3.3	2.7	16.5	13.5	4.05	103.4	15.4	-68.69
7	3.3	3.3	13.5	16.5	4.05	84.6	15.4	-214.6
8	2.7	2.7	13.5	13.5	4.05	84.6	12.6	-184

The W/L (width to length) values for each transistor was varied by 10 percent and found out that the optimized values were appropriate for the first row of matrix. Here the W/L values for M1, M2, M3, M4, M5, M6, M7(M8 was kept constant) were 3.3, 3.3 ,16.5, 13.5, 4.95,12.6, 84.6 respectively. The Temperature sensitivity for the device parameter W/L was found to be -36.76 mV/ºC which is better than the nominal value of -54.42 mV/ºC. The Table2 indicates the runs with the various W/L values and the Y column indicates the Temperature Sensitivity in mV/ºC. Further the Temperature Sensitivity varying the process parameter (Vth) for the 1st row of Plackett-Burman Design Method was carried out. This yielded a temperature sensitivity of -34.15 mV/ºC as compared to the nominal value of -45.13mV/ºC.

V. CONCLUSION

In this paper we have successfully obtained almost the same Vref that we theoretically should have obtained using the Bandgap Reference Generator with 2 Stage Operational Transconductance Amplifier device. The Plackett-Burman Design Method was highly instrumental in optimizing the process and device parameters of Vth and W/L Respectively for optimum Temperature Sensitivity of the BGR. The optimized values of Temperature Sensitivity obtained for changes in process and device parameters are -34.15 mV/ºCand -36.76 mV/ºC respectively which were much better than the conventional BRG.

VI. ACKNOWLEDGEMENT

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