1-Bit Full Adder Based on Novel Self-Controllable Voltage Level Technique For Low Leakage Current

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Abstract- *In this work many discharge reduction techniques is studied and analyzed, once that a specific discharge reduction technique is chosen. Hand-picked technique is Self-controllable Voltage Level (SVL) technique. This method is any improved to boost the system of CMOS VLSI circuit. A full adder is that the needed CMOS circuit whose discharge current reduction is decided with the assistance of self manageable voltage level technique. Any we are going to carry our project to cut back discharge current of 4-bit adder. We are going to use Microwind 3.1 and DSCH2 package to style the circuit for coming up with the layout of one-bit adder and 4-bit adder with self manageable voltage level technique. DSCH2 is employed for coming up with the circuit with AND, OR, NOR gates and additionally with transistors. Simulation results of 1-bit adder with improved self manageable voltage level technique are much better than the previous self manageable voltage level technique.*

Keywords- Low discharge current, self manageable voltage level technique, low power. High performance, high speed.

I. INTRODUCTION

The main goals of VLSI Designer area unit to cut back the world, improve performance and decreasing the price. There is a unit many sources for the discharge current, i.e. low threshold voltage causes to sub-threshold current, terribly skinny gate oxides cause to gate discharge, and heavily-doped halo doping profile causes to band-to-band tunneling discharge. It's appeared that we've to focus to attenuate the discharge current within the range of transistors and also the massive memory substance of future SoC (System on Chip) devices. MOSFET is associate form for Metal chemical compound Semiconductor Field result semiconductor device and it's the key part in high frequency, high potency change applications across the industry. it would be shocking, however transistor technology was unreal in 1930, some twenty years before the bipolar semiconductor device. The primary amplitude transistor transistors were in-built the late 1950's whereas power MOSFETs is offered from the middle 70's. Today, lots of MOSFET transistors area unit integrated in trendy electronic elements, from microprocessors, through "discrete" power transistors. For the past twenty years Complementary Metal chemical compound chemical element (CMOS) technology has contend associate ever a lot of necessary role within the integrated circuits trade. Not that MOS FET (MOSFET) technology is new. It was already planned in 1925 by J. Lilienfield, however issues with materials prevented production makes an attempt of MOSFET semiconductor device. The analysis of MOSFETs gave birth to bipolar transistors that were easier to supply and have become the dominant semiconductor device technology for many years. Any analysis in chemical element process yielded the chemical element coplanar method that created MOSFET devices potential around 1960. Single-polarity p-type transistors were favored till the emergence of NMOS silicon-gate technology in 1971.

II. LEAKAGE CURRENT

In order to realize the prime quality current style, power consumption is that the major issue that ought to detain management. The discharge power in CMOS circuits is shown by the contribution of discharge currents in every semiconductor device. Discharge power is a vital concern in VLSI circuit style. To live the overall power in circuit, there arises a necessity to estimate the discharge power. Up to 1/2 the overall power consumption is created by discharge power in high performance microprocessors. Discharge current reduction has become a robust tool to a coffee power style. It's turning into a prime priority topic in VLSI circuit style. Now we have a tendency to take into account a basic style by considering the Boolean description of the binary adder circuit. Let A and B represent the 2 input variables (addend bits), and let C represent the carry-in bit. The binary full adder may be a three-input, two-output combinative circuit that satisfies the reality table below. The sum-out and carry-out signals are often found because the following 2 combinative Boolean functions of the 3 input variables, A, B and C.

$$\text{Sum out} = A \oplus B \oplus C$$

$$\text{Carryout} = AB + BC + CA$$

By realizing the 2 functions severally, we have a tendency to use the carry-out signal to get the sum- output; the output also can be expressed as

A	B	C	SUM_OUT	CARRY_OUT
0	0	1	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. BASIC METHODOLOGY OF 1-BIT FULL ADDER

This implementation can scale back the circuit quality and save space over the chip. Also, we have a tendency to establish 2 separate sub-networks consisting of many gates (highlighted with broken boxes) which is able to be used for the transistor-level realization of the full-adder circuit.

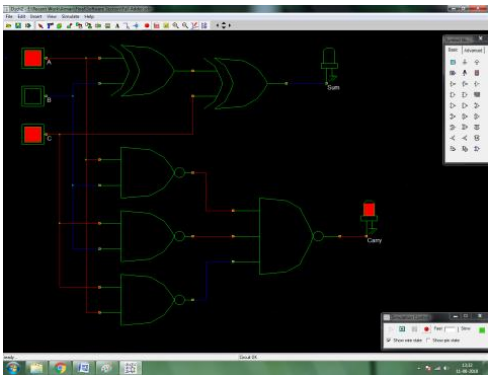

Fig 1: Gate level one bit full adder Design by using DSCH2

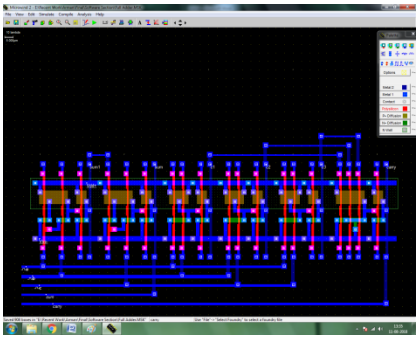

Fig 2: Transistor level schematic of the one bit full adder Design by using Microwind

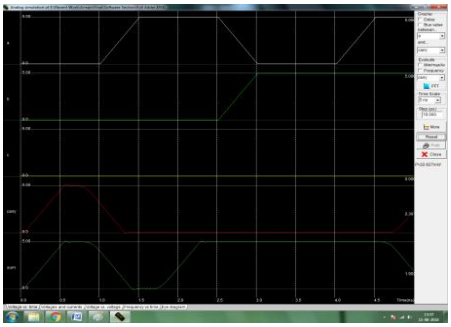

Fig 3: Output Response of the one bit full adder by using Microwind

For modifying the gate-level style into a transistor-level circuit, we have a tendency to note that each the sum-out and also the carry-out functions area unit painted by nested AND-OR- NOR structures in Figure. The AND terms area unit verified by series connected NMOS transistors, and also the OR terms area unit verified by parallel connected NMOS transistors. The input variables area unit applied to the gates of the NMOS (and the complementary PMOS) transistors. Between each the output node and also the ground the NMOS internet could encompass nested series-parallel, connections of NMOS transistors. The dual internetwork of the NMOS net is obtained once NMOS a part of a posh CMOS gate is realized, additionally with the corresponding PMOS internet, that is connected between the output node and also the power provide. The transistor-level style of the CMOS full-adder circuit is shown in Figure below. The circuit below contains a complete of fourteen NMOS and fourteen PMOS transistors, in conjunction with the 2 CMOS inverters to get the outputs. Initially, we are going to style all NMOS and PMOS semiconductor devices with a minimum transistor filler allowed during this existing technology.

Table 1: Comparison between different methods used in Full Adder

Full Adders	Peak Leakage	Average Leakage	Peak Power	Average Power
28T	388.6uW	2.46uW	7.14uW	125.2nW
Mirror	830uW	16.89uW	738.52uW	17.9uW
TG	962.28uW	439.9uW	1.29mW	973uW
Manchester	1.71mW	429.5uW	1.90mW	986.2uW
CPL	1.55mW	324.4uW	1.24mW	859.1uW
LP	732.63uW	271.2uW	1.18mW	684.8uW
LEAP	1.33mW	345.41uW	1.33mW	914.6uW
20T	1.01mW	273.6uW	804.72uW	482.0uW
14T	186.89uW	35.86uW	465.91uW	213.3uW
SERF	504.6uW	62.51uW	428.72uW	224.8uW
GDI XOR	558.42uW	4.89uW	525.34uW	7.06uW
GDI XNOR	520.14uW	4.79uW	427.76uW	6.76uW
10T	605.21uW	95.25uW	304.16uW	164.21uW
9A	480.46uW	1.77uW	429.46uW	164.2uW
9B	522.82uW	983.5nW	461.46uW	163.5uW
13A	220.6uW	173.64uW	638.20uW	383.1uW
8T	626.55uW	321.8uW	583.53uW	378.0uW
Proposed 15T	1.22mW	109.9uW	1.25mW	584.1uW
Proposed 13T	543.19uW	15.09uW	452.51uW	57.04uW
Proposed 10T	460.33uW	2.81uW	299.64uW	4.55uW

Md. Masood Ahmad had designed thirty two bit adder's using existing full adders and planned adders. Average discharge and average power consumed altogether thirty two full adders is low compared to all or any existing fifteen {transistor junction semiconductor device electronic transistor semiconductor device semiconductor unit semiconductor primarily based thirty two bit adder and planned thirteen transistor based thirty two bit adder. Venkata Ramakrishna given a paper, we've created associate elaborate discussion on the simulation results of the planned and traditional styles obtained using 90nm technology file. Fig. 6 shows the output waveforms of CMOS electrical converter circuits designed using standard, LECTOR [5] and planned techniques. It's well discovered that our planned circuit ends up in full swing output voltage kind of like the case of standard circuit. However the output of the circuit designed using the LECTOR technique [5] doesn't reach to full swing voltage.

IV. PROPOSED METHODOLOGY

Self Manageable Voltage Level Technique (SVL)

The simulation of the one-bit CMOS full adder is enforced in MICROWIND3.1 and DSCH2. The 1-bit adder during which accepts 3-bit binary numbers as input and produces the binary add at the output and carry output. Inside the MICROWIND 3.1 used a 90nm technology.

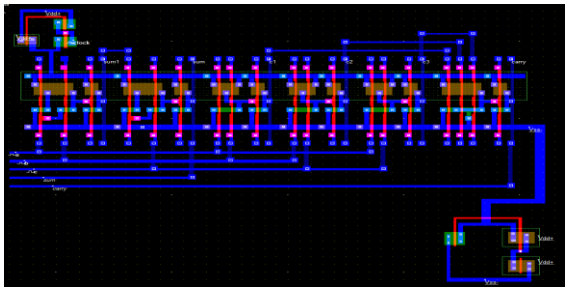

Fig 4: 1-bit Adder with self controllable voltage level technique (6T)

The designer should make sure, using associate automatic style rule checker (DRC) tool gift in MICROWIND, physical layout style rules area unit applicable during this adder layout. This is often typically done throughout the graphical entry of the layout. The back-end style of circuits is additionally supported by MICROWIND 3.1 version. User will style digital circuits and compile here using Verilog. In the above figure there's layout style of 1-bit adder enforced with the utilization of self manageable voltage level technique of six transistors in total. This layout style of 1-bit adder with SVL technique simulates the discharge current reduction but the improved SVL technique.

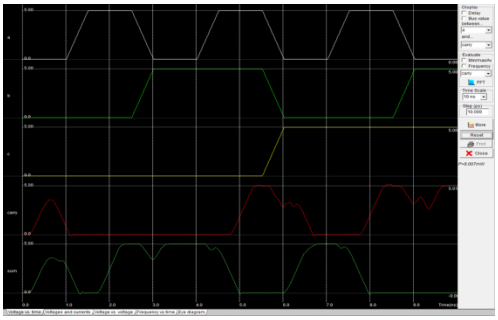

Fig 5: Voltage versus time waveform of 1-bit Adder with self controllable voltage level (6T)

Above figures show the simulation results of voltage versus current analysis and frequency versus current analysis of 1-bit adder with self manageable level technique with a complete of six transistors.

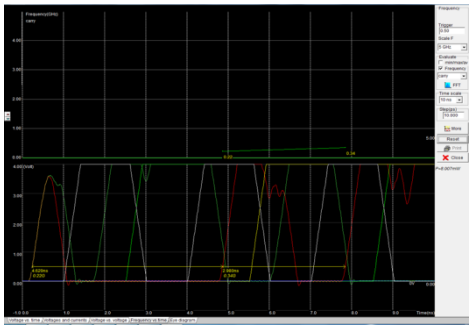

Fig 6: Frequency versus time waveform of 1-bit adder with self controllable voltage level (6T)

Following figure shows the simulation results of discharge current of 1-bit adder with self manageable voltage level technique with a use of total six transistors. Within the on top of figure it are often clearly seen the discharge current reduction is regarding 2.694 mA.

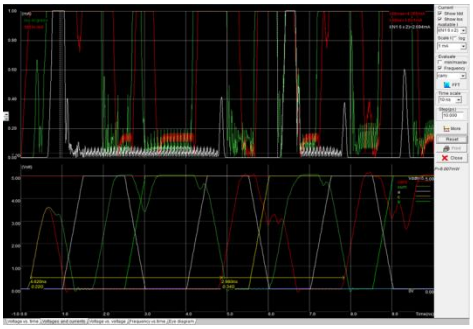

Fig 7: Leakage current 1-bit adder with self controllable voltage level (6T)

Novel Self Manageable Voltage Level Technique (NSVL)

Self manageable voltage level technique is improved by reducing the amount of transistors in higher SVL and lower SVL at the same time. Reduction of transistors from this

method can facilitate to improvise the world. Less space is employed throughout the implementation of self manageable voltage level technique over 1-bit adder.

Upper NSVL

Novel self manageable voltage level technique contains a pair of transistors in higher SVL. Reduced transistors within the existing technique ends up in NSVL technique. In higher Novel self manageable voltage level technique PMOS works in SVL mode, NMOS works in traditional mode and acts as electrical device to cut back discharge current.

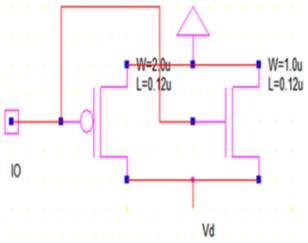

Fig 8: Upper NSVL circuit

Lower NSVL

Novel self manageable voltage level technique contains a pair of transistors in lower SVL. Reduced transistors within the existing technique ends up in NSVL technique. In lower Novel self manageable voltage level technique NMOS works in SVL mode, PMOS works in traditional mode and acts as electrical device to cut back discharge current.

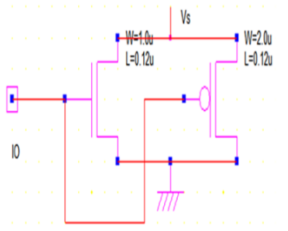

Fig 9: Lower NSVL circuit

V. CONCLUSIONS AND FUTURE WORKS

Above figure shows the simulation results of discharge current of 1-bit adder with self manageable voltage level technique with a complete use of 6 transistors. Within the on top of figure it are often clearly seen the discharge current reduction is regarding 2.694 mA. Here we have concluded that 4-bit adder is implemented with SVL technique. Here we use self controllable voltage level technique, two transistors used in upper SVL and two transistors used in lower SVL. Upper part of the SVL technique contains 1 Nmos and 1 Pmos. Lower part of the SVL technique also contains 1 NMOS and 1 PMOS. Implementation of 4-bit adder with SVL technique is done in Microwind 3.1 and $DSCH_2$ software. For layout designing Microwind 3.1 software is used and for circuit designing the $DSCH_2$ software is used. Finally simulation is done in Microwind 3.1 software.

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