4-Bit Finfet Based Priority Encoder

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Abstract- *Priority encoder converts multiple binary inputs into binary representation of the index of active input bit with the highest priority. It is used where more than one device want to access the system, it decides the priority of the device to be serve by the system. Priority encoders are used when multiple devices have to share common resources. Several researches are made on these encoders but found no research work on FinFET based Priority encoder. The FinFET device has gained very much attention on recent VLSI designs and FinFET is the substitute for bulk CMOS at nano-scale because of its high short channel effect immunity, scalability and lower leakage power consumption. In this paper, a 4 input-3output priority encoder is implemented using FinFET design.*

Keywords- FinFET, Priority Encoder, Power Delay Product, Energy Delay Product, Short Channel Effect, Sub threshold leakage current.

I. INTRODUCTION

Nowadays, priority encoders have been widely utilized in high performance applications which persistently impose special design constraints in terms of low power consumption, high-frequency and minimum area. They provide considerable time savings in the area of On-chip testing, optical communications, and computer arithmetic applications [1].Priority Encoders (PE) are commonly used in computer systems. Priority Encoder algorithm are used in number of computing components, such ascomparators[2],fixed and floating point units[3], increments, decrements[4] and interconnection network routers[5], sequential address encoder of content addressable memories[6] are important sub-systems located on-chip or off-chip, which predominantly utilize the priority encoder function. As the computer systems data width gets longer and computer system become fasten, the speed of the Priority encoder becomes a key parameter in the performance of the computer system. At the same time, the overwhelming demand for compact electronics encourages the development of a power optimized Priority Encoder. Priority encoder function is to select only one request out of number of request at is input port and then selected input is been served by the system. The proposed priority encoder accepts 4 input request lines and sets only one of the outputs that correspond to the request that has the highest priority. In this paper we simulate 4:2 Priority Encoder using FinFET circuit at different voltages and calculate different parameters of the circuit such as average power, leakage current, leakage power, delay and Power Delay product (PDP), Energy Delay Product (EDP). After comparing all simulation results at different voltage we found that on applying 0.3V to the circuit we get the better parameter in result.

1.1 FinFET

The term FinFET was invented by the University of California, Berkeley researchers to describe a non-planner, double-gate transistor built on an SOI (silicon on insulator) substrate, based on the earlier single gate transistor structure. The distinctive property of the FinFET is that the conducting channel is enfolded by a thin silicon “fin”, that is forms the body of the device. The effective channel length of the deviceis determined by the width of the fin. Due to multi gate structure FinFET has full control over the channel and thus helps in reducing the Shot-Channel effect and also helps to overcome the Sub ThresholdLeakage Current problems of MOSFET devices.

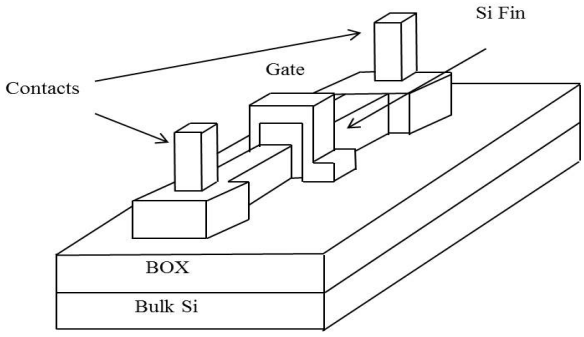

Figure1. Double Gate FinFET

The conventional Double Gate FinFET structure is shown in the figure1 [7]. The tiny slab of undoped silicone perpendicular to the structure is the channel of the FinFET.

As the gate drain and source of the FinFET is doped with same type of dopant, so there is no p-n junction formation along the channel length and reduces the leakage current. The Higher mobility in the FinFET is due to the undoped channel, which eliminates the coulombs scattering [8]. The fraction of n-type to p-type mobility is higher in FinFET. In FinFET the source-body voltage variation did not affect the threshold voltage. This improvement in mobility and also

covers the way for extended series stacked transistors in the pull-down or pull-up networks of logic gates.

Independent Gate FinFET is shown in figure 2[9-13] is the double gate device in which the two Gate electrode are not connect together (the top portion of gate is etch out) and biased with different potential.MIGFET has many special features one of them is that the threshold voltage of one of the gates can be modified by the bias applied to the other gate. Here we present Priority Encoder circuit using double gate FinFET and the symbol for double gate FinFET is shown in figure 3[14]. Here the priority encoder is simulated on virtuoso tool of cadence at 45nm technology.

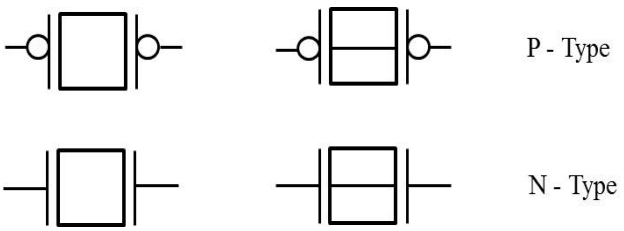

Figure3. Symbol of Independent Gate and Double Gate FinFET

II. PARAMETERS OF FINFET

2.1 Sub threshold Leakage Current

When the transistor is switches from cut-off region to saturation region (Vgs > Vth) a channel formation is occurs which allows current (I_{ds}) to flow between the drain and source. The current (I_{ds}) from drain to source is given in the below equation

$$I_{ds} = \frac{\mu_n C_{ox} W_{eff}}{L}\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2} \quad (1)$$

With μ_n the charge-carrier effective mobility, W_{eff} the effective channel width and the L effective channel length. The effective channel width W_{eff} equals the channel width in First order approximation [12].

2.2 Power dissipation

Power dissipation is an addition of static power dynamic power and leakage power. But in most of the cases power dissipation depends on dynamic power. Hence it is given by

$$P_{total} = \alpha_{in} I_{sc} V_{dd} f T_{sc} + \alpha V_{DD}^2 f C_{out} \quad (2)$$

Equation 2 is clearly shows that the Power dissipation is depends on dynamic power and for low power dissipation [16] the static power must be less.

Threshold voltage

Joining the gate work function, difference between the Gate and silicon fin, the increase in band gap and the increase in potential results in the following threshold voltage formula

$$V_{th} = V_{FB} + 2\alpha_B + \delta_w + \frac{qN_b X_{dep}}{C_{ox}\left(1 - \frac{x_n}{L}\right)} \quad (4)$$

Where V_{FB} work function difference, Φ_B surface potential at threshold voltage, δ_w is a fitting parameter introduced to take into account the changes [15, 17].

III. PRIORITY ENCODER

Priority as the name suggests means something that is more important than other and should be dealt with first (high /low priority). Priority Encoder does the same thing, whose way of providing output is similar to simple encoder with one advantage of selecting the operation with the priority function. With this facility of priority function, the input having highest priority is served first whenever choice has to make among more than one output. In addition to the two output x and y , the circuit has the third output denoted as V; this is a valid bit indicator that is set to 1 when one or more input are equal to 1, if all the input are 0, there is no valid input and V is equal to 0 and other two output are not correct and are denoted as don't care condition, the highest priority is given to the most significant bit (MSB) that is highest priority is given to the highest subscript number of the input, here we have the input D1 D2 D3 and D3 has the highest priority next is D2 and in the last D1 has the lowest priority. When D3 is 1, the output of x y is 11 (binary 3), regardless of the value so the other three lower priority input. When D2 is 1 the output xy is 10, provided that D3= 0, regardless of the value of the other two input. When D1 is 1 the output x y is 01, provided that D3 D2 = 00 and so on.

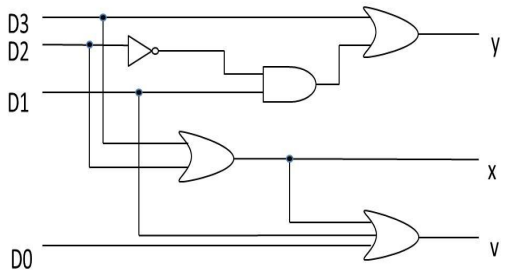

Figure.4 Circuit diagram of Priority Encoder

As we construct SG FinFET by shorting two P-types MOSFET and two N-type MOSFET to form P-type and N-type FinFET respectively and its logic diagram is shown in the figure No 3. The Priority Encoder is realized using the virtuoso tool of cadence. The spectra simulator of cadence is used to simulate the output. The gate of two PMOS or NMOS transistors are connected together to formed a FinFET like structure. Then FinFET using Priority encoder circuit is simulated by applying different voltages such as 0.3 V, 0.4 V, 0.45 V, 0.5 V, 0.6 V and 0.7 V respectively at 45 nm technology.

IV. RESULTS

In this section, we present the simulation results of Priority Encoder at 45nm technology from virtuoso tool of cadence. Figure.5 shows the comparison among Energy Delay Product and Power Delay Product curves of DG FinFET at six differentpowersupplies at 45 nm technology respectively. At 45 nm technology the 4:3Priority encoder give better result at 0.3V that is Average Power is 2.071nW, Leakage Power is 54.39pW rather than at 0.7V that is Average Power is 11.6nW, and Leakage Power is 131.1pW. So, our experimental result gives minimum Delay and Average Power at 0.3V supply.

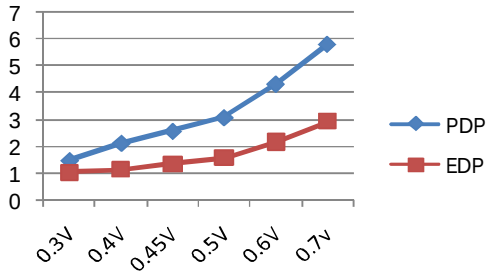

Figure 5.Veriatin of PDP and EDP with respect to voltage

V. CONCLUSION

In this paper, we work on Priority Encoder by using FinFET. FinFET is one of the emerging technology used in various applications, has replaced many conventional CMOS based devices. Low power consumption is one of the basic need in forming any electronic device and for that purpose scaling is done which leads to leakage of current but that problem is tackled by using FinFET. In this paper, Average Power, Delay, Leakage Current and Leakage Power of FinFET based Priority Encoder at different voltage was examined and better result at 0.3V power supply is obtained. The Leakage Power, Average Power and Leakage Current were found to be 2.071 nW, 54.39 pW 13.74 pA respectively. Power Delay Product is $1.4641x10^{-16}$ J and Energy Delay Product is $1.0249x10^{-22}$Js, than the 0.7V power supply in which the results are Average Power is 11.56nW, Leakage Power is 131.1pW and Leakage Current is 26.19pA, Power Delay Product is $5.8146x10^{-16}$J and Energy Delay Product is $2.9247x10^{-22}$Js. Here energy-delay product (EDP) is a useful metric for evaluating the quality of a design. As EDP is the product of PDP and Delay, PDP depends on Power supply. EDP has to be low, So EDP depends on the Delay (1/f) and the Power supply (V_{DD}), so we can reduce EDP by reducing either Delay or Power supply or we can get the tradeoff between delay and power supply.

VI. AKNOLODGEMENT

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