Delay And Power Analysis of Various Flip Flop Using Spartan 3e FPGA Kit

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Abstract- *The flip-flop has two states which are shown in the below figure. When Q=1; and Q'=0; it is in the set state . When Q=0 & Q'=1, it is in the clear state . The outputs of the flip flop Q & Q' are complements of each other and are referred to as the normal and complement outputs, respectively. The flip flop binary state is taken to be the value of the normal output. When 1 is applied to the inputs of the flip flop, both the outputs go to 0, so both the outputs are complements of each other. In a normal operation, this condition must be avoided by making sure that 1's are not applied to both the inputs simultaneously.In this work, power and delay comparison was done for different flip flops like T, D, SR and JK. Prototyping of all these multiplier Architectures has been carried out on Spartan3EFPGA.*

Keywords- FPGA(Field Programmable Gate Array),

I. INTRODUCTION

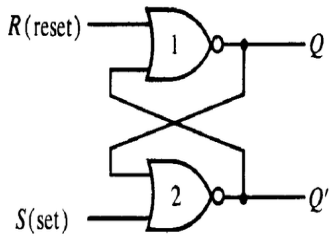
Low power issues have become an important factor in modern VLSI design. The limited power capacity systems had given rise to more power aware designs by designers. Now-a-days, power has become a crucial factor than area or speed. However, different implementation technologies present different power optimization opportunities. In technologies above 0.1m, dynamic power is the dominant contribution to the total power dissipated while in smaller technologies leakage power is gaining more importance. Dynamic power dissipation is the result of charging the load capacitances in a circuit[1]. It is given by equation where is the output capacitance, the supply voltage, E(sw)(called switching activity) is the average number of transitions and the clock frequency. Leakage power dissipation is divided in two major parts, the sub-threshold leakage and the gate oxide leakage. The sub-threshold leakage is caused by short channel effects and low threshold voltage (Vth),while the gate-oxide leakage is exponentially increasing with decreasing oxide thickness been applied in order to minimize dynamic power dissipation in arithmetic circuits, and especially in digital multipliers. Multipliers are very important devices in DSP applications, like for example FIR filters, leading to excessive power consumption. Consequently, the design of low power multipliers is a necessity for the design and implementation of efficient power-aware devices.There are two main choices for the design of a multiplier. The first is the Wallace tree form, which has the advantage of a logarithmic circuit delay, and the second is the array multiplier form, like the Carry-Save array, where the delay is linear. On the other hand the array multiplier has a regular structure, which leads to a dense layout making it ideal for fabrication. The Wallace tree has irregular structure, occupies more area on the wafer, and needs greater wiring for cell interconnections[2]. This point is crucial for present and emerging IC technologies, where interconnection plays a predominant role. This factor makes the Wallace tree inappropriate for low power applications. In this paper, we present a technique to minimize power dissipation in digital multipliers, starting from dynamic power and concentrating on the switching activity. There have been proposed a lot of techniques to reduce the switching activity of a logic circuit. In these quential world one of the most successful is clock gating, where an enable signal inhibits the clock, isolating a large block of the circuit. This technique eliminates activity and thus, power consumption. For example, in, clock gating is applied in pipelined array multipliers with significant power gains.

In pure combinational circuits the main effort of research has been to rearrange the tree of gates in a more profitable scheme, or to insert clock gated registers which provide the desired isolation. The contribution of this paper is the evaluation of a technique similar to clock gating. To isolate parts of a circuit, transmission gates are used as low delay and area overhead bypass switches. An array multiplier with bypass transmission gates can offer power reductions of more than 50%. Similar bypass ideas with different isolating components have also been reported in the past, in. However, our contribution moves one step further and proposes a mixed architecture, to address both dynamic power dissipation and performance, by doing half of the multiplication through an array structure, with bypass transmission gates, and the other half through a Wallace tree.

II. BASIC FLIP FLOP

A. SR Flip Flop

This SR flip-flop consists of two AND gates and a basic NOR flip-flop. The outputs of the two AND gates remain at 0 as long as the clock pulse is 0, irrespective of the input values of S & R. When the clock pulse is 1, information from the inputs S & R passes through to the basic flip-flop. When S=R=1, the occurrence of a clock pulse causes both the outputs go to 0. When the clock pulse is removed, the state of the flip-flop is unstated.



(a) Logic diagram

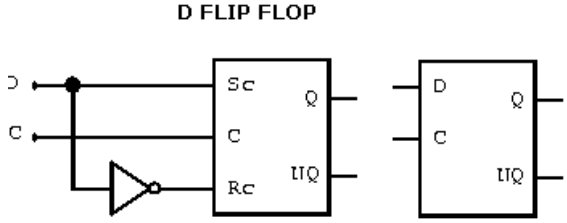
S	R	Q	Q′	
1	0	1	0	
0	0	1	0	(after $S=1, R=0$)
0	1	0	1	
0	0	0	1	(after $S=0, R=1$)
1	1	0	0	

(b) Truth table

fig(1) SR Flip SLop

B. D Flip Flop

The D flip-flop is the modification of the SR flip flop which is shown in the figure. The i/p D goes directly into the input S and the complement of the input D goes to the input R. The D input is sampled during the existence of a clock pulse. If it is 1, then the flip-flop is switched to the set state. If it is 0, then the flip-flop switches to the clear state.

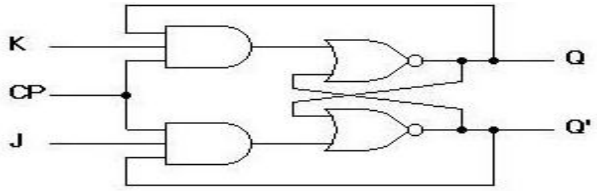


D	C	Q	$\overline{Q}$
x	0	no change	
0	p	0	1
1	p	1	0

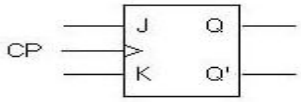
fig(2) D Flip Flop

C. JK Flip Flop

A JK flip flop is a modification of the SR flip flop. The inputs of the flip flop J, K behave like the inputs S and R. When input 1 is applied to both J & K, the flip flop switches to its complement state(if Q=1, it switches to Q=0). The JK flip flop figure is shown below.The output of the flip flop Q is ANDed with inputs k and clock pulse. The flip flop would be cleared during a clock pulse only if the output Q was previously 1. Likewise, the output Q' is ANDed with inputs CP and J. So that the flip flop is set with a clock pulse only if Q' was previously 1.



(a) Logic diagram



(b) Graphical symbol

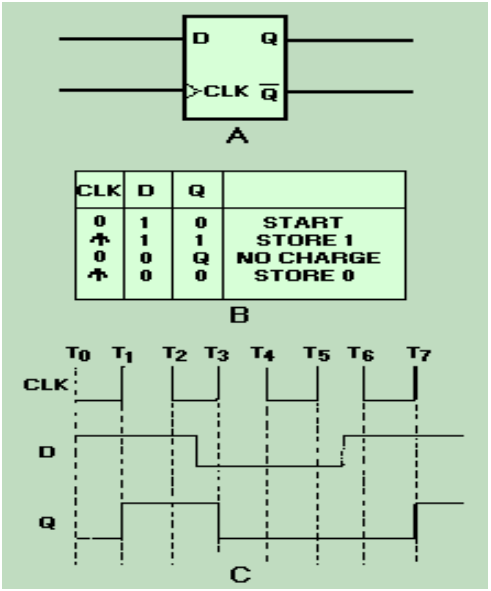
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(c) Transition table

fig(3) JK Flip Flop

D. JK Flip Flop

The T flip flop is a single input version of the JK flip flop. The operation of this T flip flop is as follows: When the input of the T is '0' such that the 'T' will make the next state the same as the present state (i.e. T = 0 then, present state = next state = 0). However, if the input of the T is '1' then the 'T' will change the next state to the inverse of the present state (i.e. T = 1 present state = 0 and next state = 1).



Fig(4). JK Flip Flop

III. POWER AND DELAY ANALYSIS OF FLIP FLOP

- D Flip-Flop: When the clock triggers, the value remembered by the flip-flop becomes the value of the D input (Data) at that instant.
- T Flip-Flop: When the clock triggers, the value remembered by the flip-flop either toggles or remains the same depending on whether the T input (Toggle) is 1 or 0.
- J-K Flip-Flop: When the clock triggers, the value remembered by the flip-flop toggles if the J and K inputs are both 1 and the value remains the same if both are 0; if they are different, then the value becomes 1 if the J (Jump) input is 1 and 0 if the K (Kill) input is 1.
- S-R Flip-Flop: When the clock triggers, the value remembered by the flip-flop remains unchanged if R and S are both 0, becomes 0 if the R input (Reset) is 1, and becomes 1 if the S input (Set) is 1. The behavior in unspecified if both inputs are 1. (In Logisim, the value in the flip-flop remains unchanged.)

These are the various types of flip-flops being used in digital electronic circuits and the applications of Flip-flops are as specified below.

- Counters
- Frequency Dividers
- Shift Registers
- Storage Registers

IV. RESULTS AND DISCUSSION

The various flip flop implemented in FPGA kit and its results are discussed below

SR Flip Flop

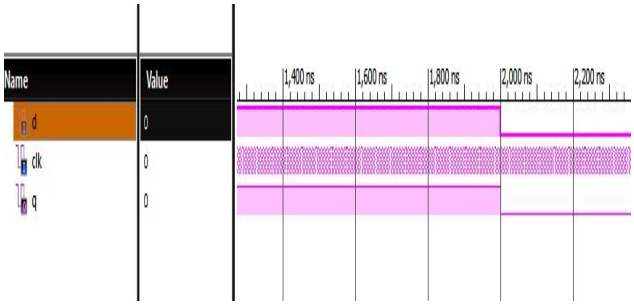
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	1	4,896	1%
Number of 4 input LUTs	1	4,896	1%
Number of occupied Slices	1	2,448	1%
Number of Slices containing only related logic	1	1	100%
Number of Slices containing unrelated logic	0	1	0%
Total Number of 4 input LUTs	1	4,896	1%
Number of bonded IOBs	5	158	3%
IOB Flip Flops	1		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	1.67		

Fig(5). Utilization for SR Flip Flop

D Flip Flop

Logic Utilization	Used	Available	Utilization
Number of Slices containing only related logic	0	0	0%
Number of Slices containing unrelated logic	0	0	0%
Number of bonded IOBs	3	158	1%
IOB Flip Flops	1		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	1.00		

Fig(6). Utilization for D Flip Flop

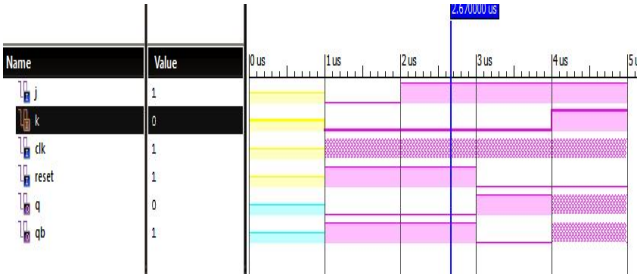


Fig(7). Simulation result for D Flip Flop

JK FF

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	2	4,896	1%
Number of 4 input LUTs	3	4,896	1%
Number of occupied Slices	2	2,448	1%
Number of Slices containing only related logic	2	2	100%
Number of Slices containing unrelated logic	0	2	0%
Total Number of 4 input LUTs	3	4,896	1%
Number of bonded IOBs	6	158	3%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.33		

Fig(8). Utilization for JK Flip Flop

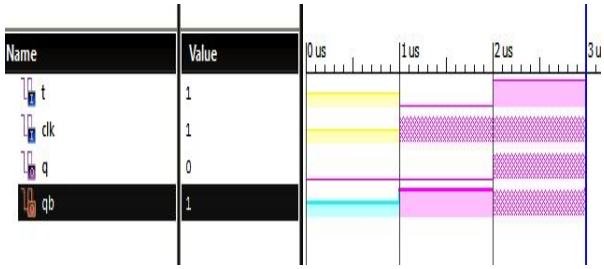


Fig(9). Simulation result for D Flip Flop

T FF

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	2	4,896	1%
Number of 4 input LUTs	1	4,896	1%
Number of occupied Slices	2	2,448	1%
Number of Slices containing only related logic	2	2	100%
Number of Slices containing unrelated logic	0	2	0%
Total Number of 4 input LUTs	1	4,896	1%
Number of bonded IOBs	4	158	2%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	1.25		

Fig(10). Utilization for T Flip Flop



Fig(11). Simulation result for T Flip Flop

Delay	SR	D	JK`	T
OFFSET IN BEFORE for Clock 'clk'	2.518ns	1.731ns	3.184ns	3.402ns
Default OFFSET OUT AFTER for Clock 'clk'	4.063ns	4.040ns	4.063ns	4.063ns

Table(1). Simulation result for T Flip Flop

V. CONCLUSION

In this work, we have implemented flip flop for Low power Applications. This topology was implemented on Spartan 3E FPGA and it was observed for the various flip flop like T, D, JK and SR. Power Measurements were performed using Xilinx "X-Power Analyzer", for a test case like random patterns. Also, this design can be implemented by using standard cell libraries designed for low power, with ASIC Development Kit, for improving the performance relatively.

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