A Novel Approach For Process Modeling of GaN Based MOS Device

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Abstract- *GaN materials are increasingly becoming popular as a replacement to the Si based devices. Due to their wide band gap they have a huge potential for high power and high frequency applications in the field of military, satellite, led's, lasers, medicine and many more. In this paper the process modeling of GaN MOS HEMT using Devedit Silvaco is discussed. Also the comparison with the conventional MOS is presented .The fabrication of various layers; their thicknesses as well as the challenges that will be faced during their fabrication are briefly discussed.*

Keywords- Gallium Nitride, MOS HEMT Device, wideband gap, 2DEG.

I. INTRODUCTION

HEMTs are heterojunctions with semiconductors having dissimilar band gaps. HEMT have several advantage over Silicon (Si) semiconductor devices, like, higher power density, high breakdown voltage and higher electron mobility (> $1000 cm^2/Vs$). Blue and Green Laser Diodes-Data storage, Displays laser TV and screens, LED, Power Electronics, PV industry RF Electronics - 3G/4G, Wi Max, Defense etc. are some of their applications. A cross section view of AlGaN MOS is shown in following fig1 [1].

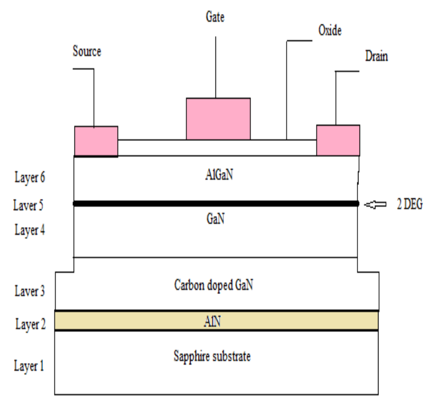

Fig 1: Cross sectional view of GaN based MOS

The structure consists of a Si substrate with GaN and AlGaN layer which results in a heterostructure. The rest structure is similar to that of a conventional MOS with source drain and gate terminals respectively. Table 2, shows comparison in between Si and GaN material.

Table 2: Properties of Si and GaN (at 300 K)[11]

Parameter	Si	GaN
a	5.43Å	4.51 Å
α ˚C	2.6x10^ (-4) ˚C	5.6 x10^(-4) ˚C
E_G (D/I)	1.1eV ,I	3.45Ev , D
E_{max}[MVcm(-1)]	0.3	2
n_i (atoms/cm^3)	9.6*10^ (9)	1.9*10^(-10)
µn [cm2 / V s]	1500	2000
Ɛr	11.9	9
v_{sat} [x 10 ^(7)	1	2.2
T_{max} (˚C)	150	800

Lattice Constant - a Å, Thermal coefficient of expansion– α ˚C, Band Gap (Direct/Indirect) - E_G (D/I), Breakdown field - Emax [MVcm (-1)], Intrinsic carrier Concentration-ni [atoms/cm^3], Electron Mobility- µn [cm^2 / V s], Relative permittivity- Ɛr, Saturation velocity [x 10^(7)]-vsat, Maximum working temperature- Tmax (˚C).

It has been shown above, that the electron and hole mobility, thermal coefficient of expansion breakdown field, maximum working temperature of GaN is higher than Si. Hence GaN is preferred for high power applications.

GaN based HEMT with depletion mode RF transistors first appeared in about 2004 using the phenomenon demonstrated in 1994 of 2DEG (two-dimensional electron gas) near the interface between an AlGaN and GaN heterostructure interface.Using SIGANTICtechnology, later in 2005 HEMT transistor made with GaN was grown on silicon wafers. The first enhancement mode GaN on Si that was designed specifically as power MOSFET replacements in 2009. Table 2 shows the difference between conventional MOS and GaN based MOS [1] [8].

Table 2: Comparison of Conventional MOS with GaN based MOS [1]

	Conventional Si based MOS	**GaN MOS**
Cross Sectional View	Source, Gate, Drain, x, L	Gate, Oxide, Source, AlGaN, Drain, GaN Channel, GaN Buffer
Symbol[1][]	Drain, Gate, Source, Gate, Source, Drain	MOS-HEMT: Source, Gate, Drain; HEMT: Source, Gate, Drain
ID-VDS CHARACTERISTICS [1]	Id: 100–600; Vds: 5, 10, 15 Lower value of Id	Id: 100–600; Vds: 1–6 Higher current value for the same value for the same value of Vds
Transfer characteristic [6]	ID(A): 20–140; VGS (V): 0–8 For gate to source voltage of 3V, there is negligible gate current.	25°C, 175°C, V_{DS} = 3V; I_D – Drain Current (A); V_{GS} – Gate-to-Source Voltage (V) Higher value of Id
Size	They have larger size	Smaller size compared to conventional MOS
Mobility	Less mobility compared to GaN mos.	High electron mobility
Threshold voltage Vs temperature		Above 25 ˚C GaN MOS has a higher value of normalized threshold voltage.

The above table shows the comparison between GaN MOS and the conventional MOS. The GaN MOS is always depletion type i.e. “normally on” and we have to use different process to make it enhancement type i.e. “normally off”. On the contrary the conventional MOS can be any of the either type. Also the GaN MOS have smaller size and higher drain current than the conventional MOS.

II. CHOICE OF MATERIALS FOR LAYERED STRUCTURED AND FABRICATION CHALLENGES

The fabrication of GaN based MOS requires various materials such as GaN, AlGaN, AlN, carbon doped GaN layer. Table 3 shows the various layers which are required for the fabrication of GaN based MOS and their function as well as challenges during fabrication [2].

TABLE 3: CHOICE OF MATERIALS WITH LAYERED STRUCTURE

Layer No.	Materials	Function	Challenges in modeling
I	Si, SiC, Sapphire(Al2O3)	Affects the performance and defect density	SiC substrates are best
II	AlN	Improved lattice match between AlN layer and GaN layer.	Due to lattice and thermal coefficient of expansion mismatch of GaN with sapphire/SiC layer causes dislocations
III	Carbon doped GaN layer	Confinement of charges at the interface	
IV	GaN	Affects 2-DEG concentration	
V	2DEG Layer	Electron mobility is high in this region	It forms due to combination of different band gap AlGaN layer and GaN layer.
Layer No.	**Material**	**Function**	**Challenges in modeling**
VI	AlN	Decreases dislocations due to lattice mismatch	

The above table 3 shows that during fabrication proper matching between the GaN and substrate is essential as it may result in defects, traps and dislocations which may affect the performance of the device. Hence proper choice of the substrate is essential. There are three choices for substrates SiC, sapphire and Si. The thermal conductivity for SiC have low lattice and thermal coefficient ofexpansion mismatch with GaN hence they are chosen for substrates. However sapphire and Si are also preferred due to low cost. AlN is used to improve the lattice match between GaN and substrate. Due to the difference in band gap of GaN and AlGaN layer, a 2DEG layer is formed. The electron density in 2-DEG layer is affected by the GaN layer.

III. PROCESS MODELLING USING SILVACO

While modeled HEMT based NMOS device, the basic design parameters are material selection, doping concentration, layer thickness and dimensions. Simulation software is Silvaco Devedit, in which the structure can be formed and impurities can be added easily compared to Athena. The only issue is that if there occurs any mistake once the structure is formed then the entire structure has to be made again.

Step 1: The GaN based MOS HEMT is first grown on the sapphire substrate [0001]
Step 2: Then GaN is deposited on the sapphire substrate by MBE.
Step 3: AlN- 20nm, Carbon doped GaN layer- 1.5um, AlGaN – 83.8NM, GaN – 0.3um, Oxide layer
thickness- 45nm, Ti/Au- 10-25 nm, Sio_2isolation-450nm.
Step 4: The formed 2DEG layer has a density of around ~$2.7\times10^{13}/cm^{2}$. [7].

IV. FABRICATON PROCESS STEPS USING DEVEDIT

Step 1. Choose the Dev Edit 2D from the deck build window of Silvaco tool, Dev Edit Window is shown as:

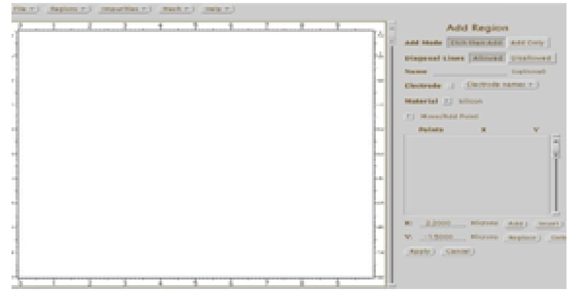

Fig 2: Dev Edit Window

Step 2.Then according to the region you have to make choose the region parameter accordingly.

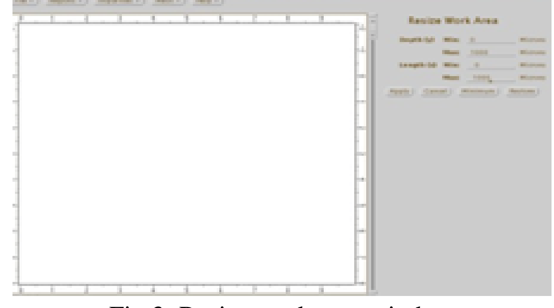

Fig 3: Resize work area window

Step 3. For sapphire (0001) wafer, add material sapphire in the region menu, the corresponding structure is as shown below:

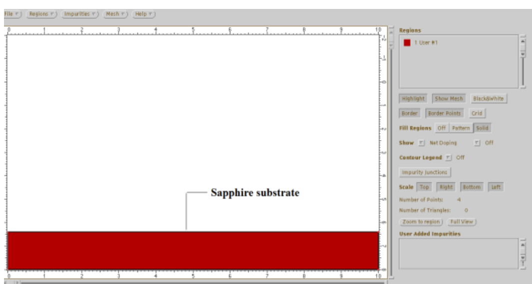

Fig 4: Sapphire substrate

Step.4 Then a thin layer of AlN of about 20nm is deposited over the sapphire substrate.

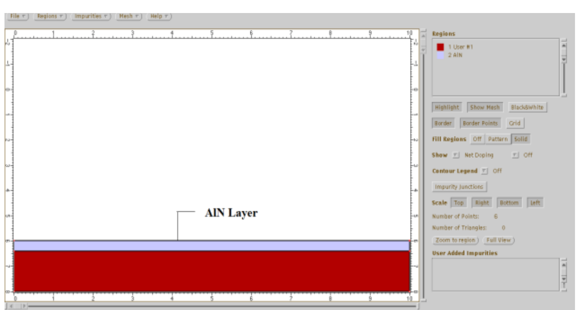

Fig 5: Deposition of AlN layer

Step 5. Then a 1.5 um highly resistive carbon doped GaN layer is deposited and etched over the side using etch region in the devedit window to obtain the following structure

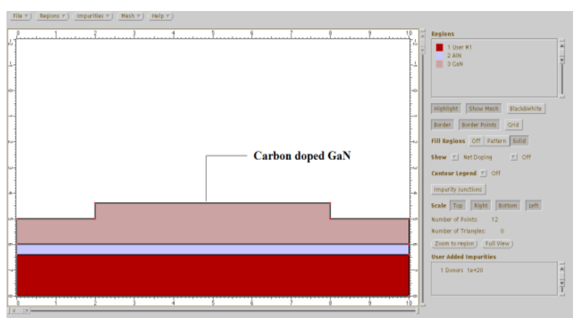

Fig 6: Deposition of carbon doped GaN

Step 6. Above the carbon doped GaN another layer of undoped GaN 10^{16} cm^{-3} is deposited with a thickness between 1.5 um.

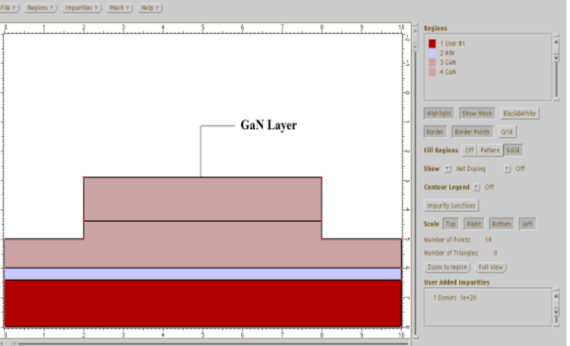

Fig 7. Formation of n- GaN layer

Step 7 Then AlGaN with a concentration of 10^{15} cm^{-3} and thickness of 83.8 nm is deposited above the GaN layer

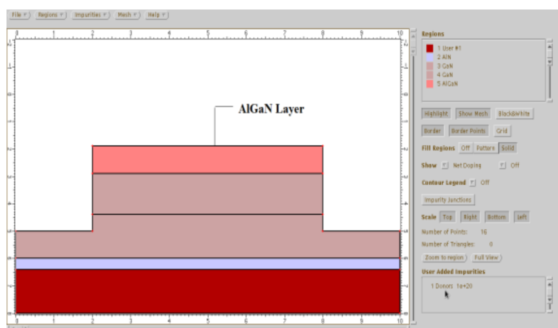

Fig 8. Deposition of AlGaN layer

Step8. Then source and drain contacts are provided of Ti/Au of 10-20nm in thickness.

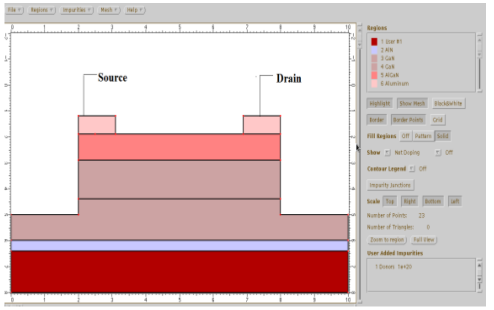

Fig 9: Formation of source and drain regions

Step 9. A layer of SiO_2 dielectric is deposited with a thickness of 45nm as shown in the corresponding.

Fig 10: Deposition of SiO_2

Step 10. Deposition of polysilicon gate over the SiO2dielectric layer as shown in fig 11.

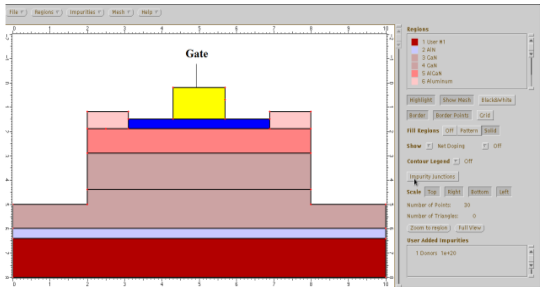

Fig 11: Deposition of polysilicon gate

Step 11. The final GaN MOS HEMT structure with the source ,drain , gate ,SiO_2 dielectric and a 2-DEG layer at the interface of AlGaN and GaN with a carrier concentration of 1 x 10^13 cm^{-2} is as follows

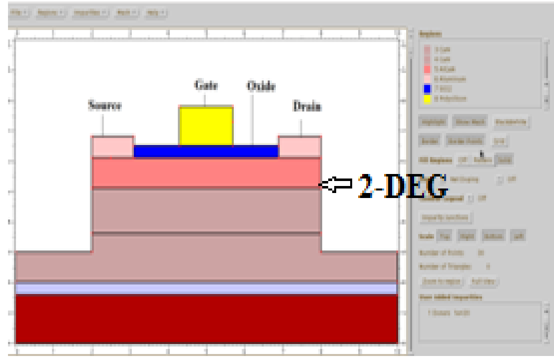

Fig 12: GaN MOS HEMT

V. FUTURE SCOPE AND CONCLUSION

The process modeling of GaN based MOS HEMT on sapphire substrate using Devedit Silvaco was performed .The higher breakdown voltage and high band gap of GaN MOS HEMT makes it an ideal candidate for high power applications.

They can be used in wide variety of applications ranging from satellites for reducing their size, for transmitting electricity at safe frequencies which is quite difficult in their silicon counterparts. Using GaN for high frequency applications also helps in increasing range of distance for wireless power transfer. By using smaller and more efficient sensing coils built of GaN FET the resolution of MRI machines is also improved. [9][10].An extensive research and some production are also being carried out for its use in power electronics, automotive applications, led's and lasers etc.

But due to the lattice mismatches of materials device performance has not reached its true limit. Thus by using proper lattice matching materials, GaN MOS HEMTS will surely prove to be the most ideal material for high voltage and high temperature

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