Optimization of Memristor based SRAM Cell using MTCMOS Technique

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Abstract- *Now a day as the technology is increasing day by day the chip size is decreasing and millions of transistors are placed on a single chip as a result the design complexity is increasing. Bottleneck is to reduce some parameters related to designing of chip like delay, average power and leakage power. In industry and research academia low power devices are very demand full, so in this paper design Multi Threshold CMOS (MTCMOS) based 6T and 7T Memristor Static Random Access Memory (SRAM) has been implemented and reduces parameters like delay, average power and leakage power. This is a nonvolatile memory because it uses Memristor. Memristor is a forth missing non-linear resistor which acts as memory and it improves the power and speed. In this paper MTCMOS technique is used, recently it is very famous in industry. It is a power reducing technique that helps in reducing leakage power in the SRAM by turning of the inactive circuit's domains. Designing and calculation of parameters of simple SRAM and MTCMOS based Memristor SRAM has been done with cadence virtuoso tool and that was done at 45 nm technology with the operating voltage of 0.7 volt.*

Keywords- Low Power, Memristor, MTCMOS, SRAM .

I. INTRODUCTION

The As the VLSI technology is increasing, the memories are also increasing. Memory is nothing but it is a collection of storage cell with proper input and output and it is widely used to design computer, mobile phones and other similar devices [1].One type of these memories is SRAM. It is volatile in nature that means data is stored, when power is plugged in, and as the power is plugged out data will get lost. The word static indicates that it does not need refreshing technique. It is type of semiconductor memory and it use numbers of transistors to store a single bit. It reduces the delay between the processor and memories. These advantages of SRAM are used to design batteries for portable system like mobile phones, laptops and other electronic devices [2]. To design these devices from SRAM, low power and leakage parameters are crucial because in recent year's technology is scaling down rapidly. So we apply some techniques to design SRAM to achieve low power for high performance of the circuits. In this paper, MTCMOS technique and Memristor have been applied to design SRAM to reduce average power in comparison to the simple SRAM. And in this paper, parameters like leakage power and delay has also been calculated in reduce form.

Memristor was invented by Leon O. Chua in 1971 and according to Chua Memristor is a fourth missing, two terminal passive elements with variable resistance also called as Memristance that give relation between flux (φm) and charge (q) [5]. This relation represented as-

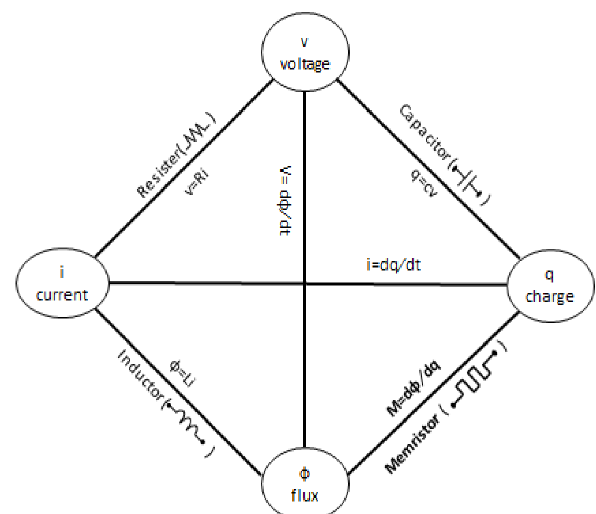

Fig. 1 Fourth missing element

Memristor is defined as a two terminal non-volatile device in which the magnetic flux (φm) between the terminals is a function of the amount of electric charge q that has passed through the device and it is denoted by M and its unit is Ω and mathematically represented as-

$$M(q) = \frac{d\varphi m}{dq} \quad (1)$$

Where M is the Memristor, φm is the magnetics flux and q is the charge. First Memristor was manufactured in HP labs by the R. Stanley Williams in 2008[6].

II. TECHNIQUE DESCRIPTION

Low power application is very needful for battery operated devices. Power dissipation in system on chip and it mainly depends on static, dynamic and short circuit components [11]. In battery operated devices power consumption is also noticeable parameter for the chip designer. To reduce the overall power consumption one method is to scale the supply voltage, but result is increase in leakage current[12].The main source of leakage current is sub-threshold leakage and it is defined as in CMOS transistor, the state of a weak inversion conduction current when Vs < Vth. And mathematically it is represented as-

$$I = I_0 .\exp\left(\frac{Vgs-Vth}{\eta kT/q}\right).[1-\exp(\frac{1-Vds}{kT/q})]$$

(2)

Where,

$$I_0 = \mu_0 C_{ox}(W/L)(kT/q)^2(1-e^{1.8})$$

(3)

μ_0 is the low field mobility, W and L are the transistor channel width and length, C_{ox} is the gate oxide capacitance, q is the electronic charge and k is the Boltzmann's constant. To reduce the leakage power number of technique are available one type of technique is MTCMOS technique.

MTCMOS technique uses two transistor one PMOS transistor known as header and one NMOS transistor known as footer, these transistors are also known as sleep transistor as shown as-

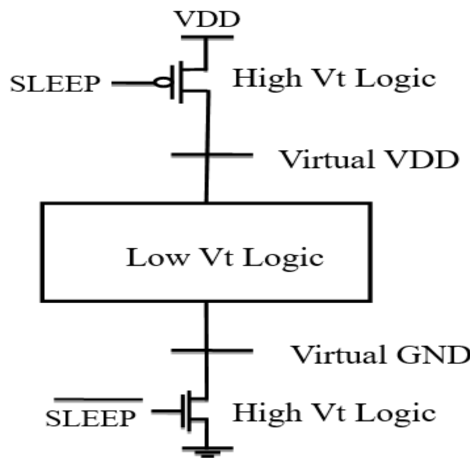

Fig.2 MTCMOS Technique

In MTCMOS header and footer transistor are high Vt transistors and between these transistors low Vt logic circuit is used. High Vt sleep transistors are used to connect or disconnect the low Vt logic from power and ground domains [13]. Header and footer transistors depends on the sleep signal, during the active mode sleep signal is disserted because both sleep transistors are turned on and provide a virtual power and ground to the low Vt logic. When the sleep device is in standby mode sleep signal is asserted forcing both sleep transistors to cut-off and disconnect from the low Vt logic. Result of this process low leakage power to ground when circuit is in standby mode.

III. SRAM

6T SRAM

In SRAM cell word 6T indicates that it uses six transistors in which there are two PMOS transistors and four NMOS transistors. Two PMOS and two NMOS transistors form two cross coupled inverter in which one PMOS and one NMOS form one inverter. Two other NMOS transistors are pass transistors and these six transistors together forms one simple 6T SRAM [15].In 6T SRAM cell two bit lines are BL and BLB and one word line WL and two outputs Q and QB in which BL & BLB and Q & QB are opposite to each other.6T SRAM is shown as-

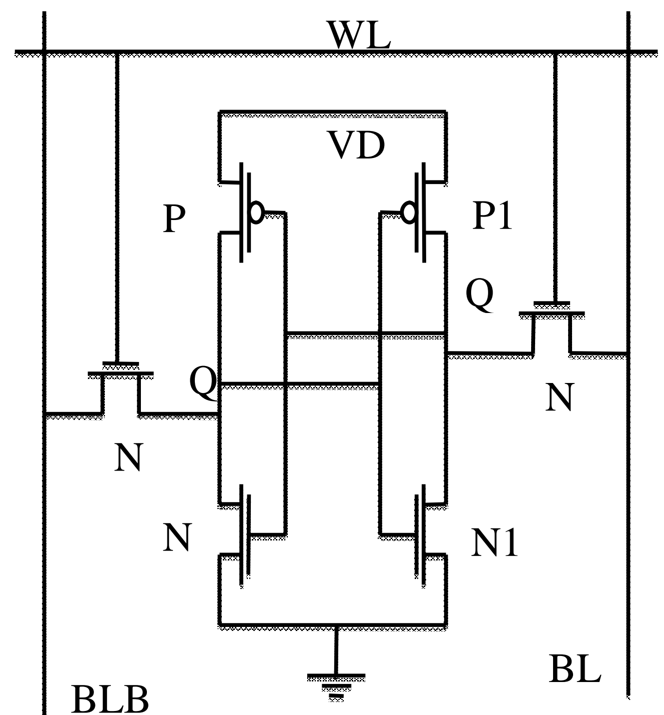

Fig. 3 Six Transistors Memory Cell

SRAM cell is used to store one bit either it will store 1 or 0 on Q and opposite values get stored at QB. SRAM performs in three different modes namely standby, write and read modes. When WL goes low (WL = 0) then SRAM work in standby mode i.e. pass transistors are off in this mode. When word line high then SRAM work either in write or read mode.

In write operation word line goes high (WL = 1) and pass transistors are on and set the value that has to be written on BL and opposite value will be set on BLB and that value will be stored in cross coupled inverters.

In read operation also word line is high (WL = 1) and BL and BLB lines are precharged. The value that is already stored in cross coupled inverters either in state 1 or 0. These values are transferred to the bit lines BL and BLB in which only one line is discharged to ground and other line is precharged this difference is sensed by the sense amplifier and value is shown at the output of the sense amplifier.

7T SRAM

7T SRAM cell made of 7-transistors in which there are two PMOS transistors and five NMOS transistors. One PMOS and one NMOS make an inverter. There are two inverters in 7T SRAM and they are cross coupled to each other and two NMOS transistors use as a pass transistors and fifth transistor N5 is connected between two cross coupled inverter. N5 connects and disconnects the feedback connection of cross coupled inverters and read and write operation is also controlled by N5 transistor [17]. Show as-

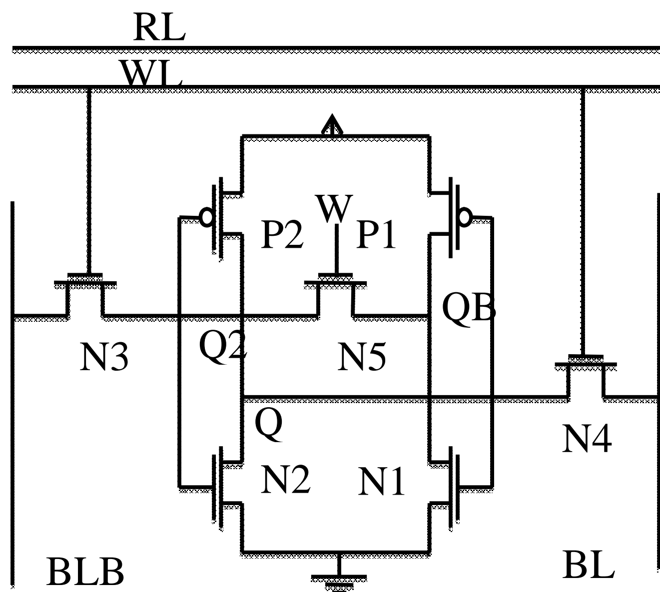

Fig. 4 Seven Transistors Memory Cell

In 7T SRAM cell two bit lines BL and BLB and two word line RL and WL. BL & BLB are precharge before and after the read/write operation. In write operation is controlled by the N5. N5 disconnects the feedback connection between the two cross coupled inverters so that write operation is performed only by the BLB line. BLB line transforms the complement of the input data that is stored in cross coupled inverter i.e. if stored value is 1 in cross coupled inverter then BLB should be 0and vice-versa.

In read operation transistor N5 kept on and it works as a simple 6T SRAM. In SRAM cell value is read by sense amplifier and these values are either 1 or 0 at the node Q. When Q is low (Q = 0) read path uses two transistors and when Q is high (Q = 1) it uses three transistors and this path is critical read path.

IV. MTCMOS BASED MEMRISTOR SRAM

Designing of memory with simple SRAM give good results but in these type of memory bottleneck is retention of data and low power. To overcome this type of problem new technique was needed for reducing the power dissipation, delay and increasing the speed of read/write in memory. In this paper, we are designing MTCMOS based Memristor SRAM which has been already discussed that Memristor was invented by Chua in 1971 and manufactured in 2008 by HP labs [22].

Memristor works as a switch like transistor except that Memristor is a two terminal device while transistor is a three terminal device [23]. Memristor is manufactured by two thin layers and these layers are sandwiched between platinum nanowires and layers are also in nanometer size. These layers are of doped TiO_{2-x} and another is undoped TiO_2 [21]. Change in resistance occurs in these layers because one TiO_2 layers receives oxygen ions and other TiO_2 layer losses the oxygen ions i.e. movement of mobile ionic charge inside the TiO_2 layer result in change in Memristor resistance. That is why it is called variable resistance and it is used in designing of memories. The voltage-current relationship of Memristor is mathematically represented as-

$$v(t) = \left[R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1-\frac{w(t)}{D}\right)\right] \times i(t)$$

(4)

Where,

$$w(t) = \mu_D \frac{R_{ON}}{D} q(t)$$

(5)

D is the TiO_2/TiO_{2-x} film thickness, R_{ON} is the resistance for doped memristor, R_{OFF} is the resistance for memristor and w (t) is the width of doped memristor and µD is the average dopant mobility and q is the charge.

Since simple SRAM is volatile in nature hence increase the booting time of a system whereas MTCMOS based Memristor SRAM is non-volatile in nature because it uses Memristor so it stores data and remember history of resistance even after the power supply is cut-off. And to retain either of the two states it does not need power, this is the factor why the MTCMOS based Memristor SRAM does not require any external circuitry to retain data when power supply is in cut-off state [22].

In this paper MTCMOS technique was used and designed MTCMOS based 6T and 7T Memristor SRAM. It is used two sleep transistors as a high Vt logic and Memristor SRAM is used as low Vt logic shown as-

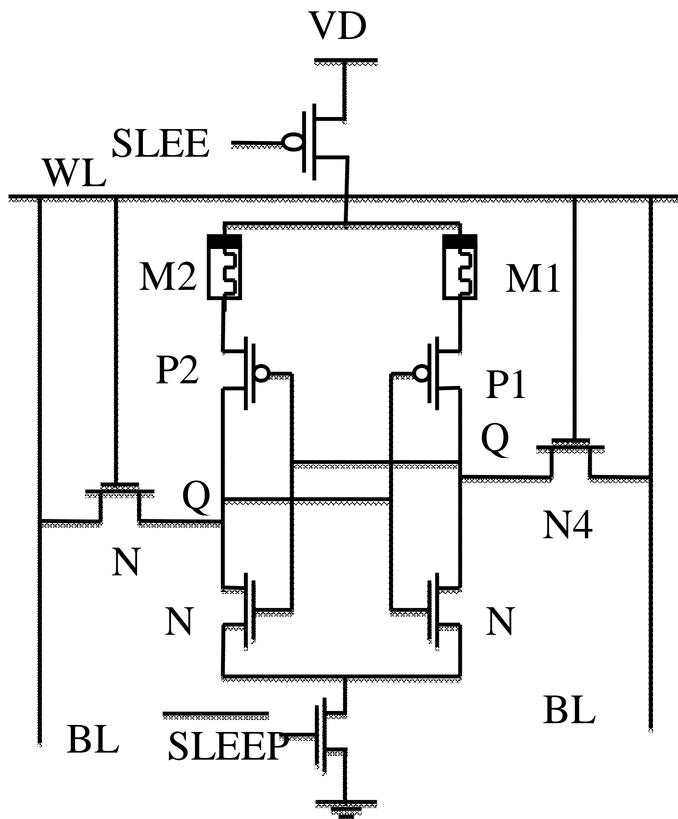

Fig.5 MTCMOS based 6T Memristor SRAM

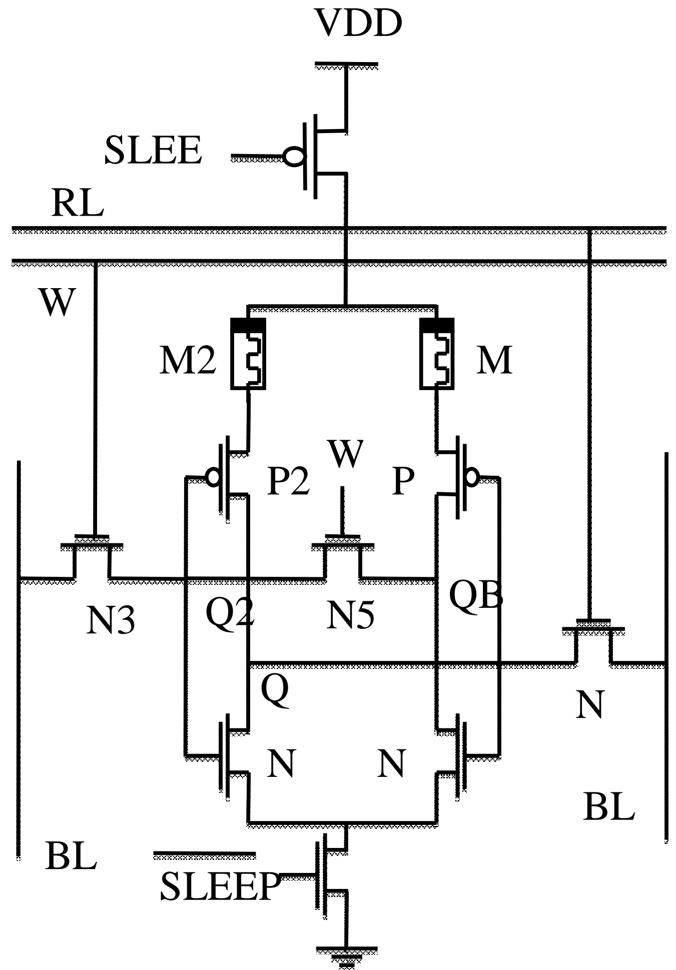

Fig. 6 MTCMOS based 7T Memristor SRAM

Shows the MTCMOS based 6T and 7T Memristor SRAM in these SRAM memories at the top PMOS transistor is used as a header transistor and it is connected to supply voltage and at the bottom, NMOS transistor is used as a footer and it is connected to the ground and Memristor SRAM was sandwiched between these two sleep transistors and Memristor M1 is connected above the PMOS-P1 transistor and Memristor M2 is connected above the PMOS-P2 transistor.

In MTCMOS based Memristor SRAM header and footer transistor operate by the sleep signal and when it is in active mode sleep signal is disserted because both sleep transistors are turn on and provide a virtual power and ground to Memristor SRAM [26]. When the MTCMOS based Memristor SRAM is in standby mode sleep signal is asserted forcing both sleep transistors to cut-off and disconnect from the Memristor SRAM.

Because of above mentioned property of MTCMOS and Memristor can help in reducing average power, leakage power and delay in the MTCMOS based Memristor SRAM.

V. SIMULATION RESULTS

Comparison of delay, average power and leakage power between 6T and 7T SRAM cell and MTCMOS based Memristor 6T and 7T SRAM cell has been done and result shown in graph and tabular form. Basic definition of these parameters are define below one by one as-

5.1 Delay

Delay in signal is the time difference in occurrence of input and output waveform and it is measure in seconds.

5.2 Average Power

The average power some time known as simply power is the average amount of energy transferred per unit time or work done and unit of average power in watt.

5.3 Leakage Power

Leakage power decreases the capacity of the devices. Further, leakage power declines the charge of any device which is continuously discharging from the device even when the device is not working and unit of leakage power in watt.

TABLE I
Parameters of 6T SRAM Cell

6T SRAM Cell		
Parameters	Simple SRAM	MTCMOS based Memristor SRAM
Delay (ps)	697.8	581.7
Average Power (nw)	47.32	15.62
Leakage Power (nw)	6.874	5.142

Shows Table-I in this table representing parameters of Simple 6T SRAM and MTCMOS based 6T Memristor SRAM and find that MTCMOS based 6T Memristor SRAM has reduced value of parameters like Delay, Average Power and Leakage Power.

TABLE II
Parameters of 7T SRAM Cell

7T SRAM Cell		
Parameters	Simple SRAM	MTCMOS based Memristor SRAM
Delay (ns)	22.01	20.93
Average Power (nw)	28.90	10.732
Leakage Power (nw)	9.59	6.8

Shows Table II in this table representing parameters of Simple 7T SRAM and MTCMOS based 7T Memristor SRAM and find that MTCMOS based 7T Memristor SRAM has reduced value of parameters like Delay, Average Power and Leakage Power.

VI. CONCLUSION

Since in this paper use Memristor SRAM it is non-volatile in nature because of Memristor and size of the Memristor is in nano scale then it increases the packing density and reduces the power in system on chip and MTCMOS technique help to reduce the leakage power in the device.

In this paper we have designed different type of simple and MTCMOS based Memristor SRAM at 45 nm technology and determined which SRAM is better based on delay, average power and leakage power. According to the these parameters and observing the above tables and graphs it is concluded that simple 7T SRAM is better than the simple 6T SRAM and MTCMOS based 7T Memristor SRAM is better than the MTCMOS based 6T Memristor SRAM. Overall MTCMOS based 7T Memristor SRAM is better than the all discussed simple SRAM and MTCMOS based Memristor SRAM due to the reduction in average power and leakage power it uses only 10.732 nw and 5.142 nw respectively.

REFERENCES

[1] ShyamAkashe, AnkitSrivastava, Sanjay Sharma, "Calculation of Power Consumption in 7 Transistor SRAM Cell Using Cadence Tool" International Journal of Advances in Engineering & Technology, vol.1, no.4, pp. 189-194, Sept 2011.

[2] ShyamAkashe, MayankShastri, Sanjay Sharma "Multi vt 7T SRAM cell for high speed application at 45nm technology," AIP conference Proceedings, vol.1476, pp.31, 2012

[3] L. O. Chua, “Memristor -the missing circuit element,” IEEE Transactions on Circuit Theory, vol.18, no.5, pp.507–519, September 1971.
[4] S. Williams “How we found the missing memristor,” IEEE SPECTRUM vol.45, PP.28-35, 2008.
[5] Nikhil Raj ,Rohit Lorenzo “An Effective Design Technique To Reduce Leakage Power” IEEE Students,” Conference on Electrical, Electronics and Computer Science, pp 1-4, March 2012 of Bhopal.
[6] Shi-Hao Chen, Youn-Long Lin, Mango C.-T. Chao “Power-Up Sequence Control for MTCMOS Designs,” IEEE Ttransactions on Very Large Scale Integration (VLSI) systems, vol.21, pp. 3, March 2012.
[7] Hailong Jiao, VolkanKursun “Ground Bouncing Noise Suppression Techniques for Data Preserving Sequential MTCMOS Circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, may 2011.
[8] ShyamAkashe, Sanjay Sharma “Low Power SRAM Cell Design based on 7T Configuration,” International Electronic Engneering Mathematical Society IEEMS, vol 4, pp. 11-18, March 2010.
[9] ShyamAkashe, Sanjay Sharma, “Design Trade-Offs for Nanoscale Process and Material Parameters on 7T SRAM Cell,” Journal ofComputational and Theoretical Nanoscience, Vol. 10, pp. 1–4, 2013.
[10] D.Vijaya Kumar, “Reduction of leakage power in 8T SRAM cell using virtual ground,” International Journal of Engineering Research and Applications (IJERA), vol. 2, no. 3, pp. 204-208, May-Jun 2012.
[11] S. K. Nanda, PayalP.Harne, “Review Paper on Memristor MOS Content Addressable Memory,” Inetrnational Journal of Innovative Research inElectrical, Electronics, Instrumentation and Control Engineering, vol. 2, no. 1, pp. 742-745, January 2014.
[12] NupurG.Nanoti, PrafullaD.Gawande “Design of High Speed Addressable Memory based on Memory-Resistance Using 45nm CMOS Technology,” International Journal of Application or Innovation in Engineering & Management(IJAIEM), vol 3, no. 3, pp. 467-477, March 2014.
[13] Shi-Hao Chen, Youn-Long Lin, Mango C.-T. Chao “Power-Up Sequence Control for MTCMOS Designs,” IEEE Ttransactions on Very Large Scale Integration (VLSI) systems, vol.2, no.3, pp. 413-423, March 2012.
[14] H. J. B. da Costa, F. de A. Brito Filho, P. I. de A. do Nascimento, “Memristor Behavioural Modeling and Simulations using Verilog-AMS,” IEEE conference, pp. 1-4, Feb-March 2012 in Playa del Carmen.
[15] S. Kvatinsky, K. Talisveyberg, D. Fliter, A. Kolodny, Uri C. Weiser, Eby G. Friedman, “ Models of Memristors for Spice Simulations,” IEEE 27th Convention of Electrical and Electronics Engineers, pp. 1-4, 2012 in Israel.