SRAM Size And Power Dissipation Reduction By Using 4 Storage Cells & 1 Access Transistor

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Abstract- *This paper gives the concept of using 5 Transistors SRAM so that it can be utilized in the place of 6 Transistors SRAM. By using DSCH2 and Microwind 2.6K I have design layout of 5T SRAM in 2.5µm and 1.5µm technology and perform read and write operation. By using Microwind 2.6K software, we can design a layout diagram and checked by using a DRC rule checker and after that simulate the layout and do the analysis. It helps to decrease the memory size.*

Keywords- DSCH2, Microwind, SRAM, DRC.

I. INTRODUCTION

Static random access memory is the basic building block of CPU in a computer. The integrated circuit is a circuit in which all contents of different circuit are integrated in a single chip. With the introduction of the integrated circuit, all the peripheral devices and microprocessor was put on a single device which is called microcontroller [1]. In microcontroller all necessary components are built together so there are no other external components are needed for its application by which we can save the time and space for construct devices. Microcontroller also store data with the help of SRAM. Microcontroller has basic registers, RAM, memory, control and timing unit. SRAM is the Static Random Access Memory in which the word static means the stored data can be retained indefinitely, without any demand for a periodic refreshes operation as long as a sufficient power supplies voltage is provided [4]. A conventional SRAM has six MOSFETs (2 PMOS and 4 NMOS) for a memory bit storing.

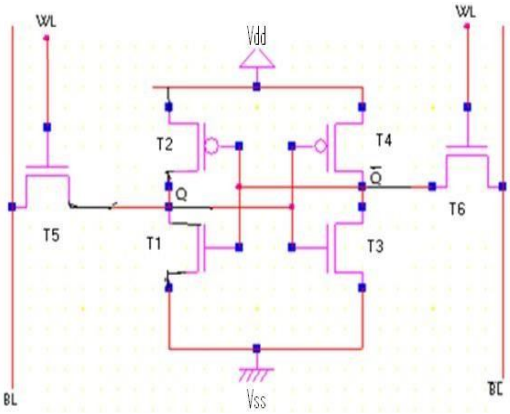

Fig.1: Stick Diagram for an SRAM [2]

This system use 2 CMOS Invertors, those are connected back to back and known as Storage Cell. 0 and 1 are the 2 stable states. T5 and T6 are controlled from word line and known as Access Transistors. They are used to access read and write the data contained in the memory cell [9]. There are 2 bit lines (BL & $\overline{BL}$). SRAM is faster than DRAM because its commercial chips accept all address bits at a time. While in DRAMs address multiplexed in two halves, i.e. the high bits is following by its lower bits to make their size and cost down [4]. There are two strong way for saving leakage and active current. First, lowering the operating voltage and secondly reduction in charging and discharging capacitance of bit and word line. Because by survey it is found that up to 70% of the total active power is dissipated in bit lines discharging/charging during read and write operations [5].

II. OPERATION OF SRAM

The access transistors perform communication with the bit lines and the inverters perform the storage element. In the SRAM cell there are three different states it is: standby when the circuit is idle, reading where the data has been requested and writing when updating the contents [6]. The three different states work as follows:

Standby-

If WL=0, T5=OFF, T6=OFF

Case I-

Let Q=0 and $\overline{Q}$=1 Then T1=ON & T4=ON
T2=OFF & T3=OFF

Case II-

Let Q=1 and $\overline{Q}$=0 Then T1=OFF & T4=OFF
T2=ON & T3=ON
It means circuit will not change the present state of Output.

Reading logic 0

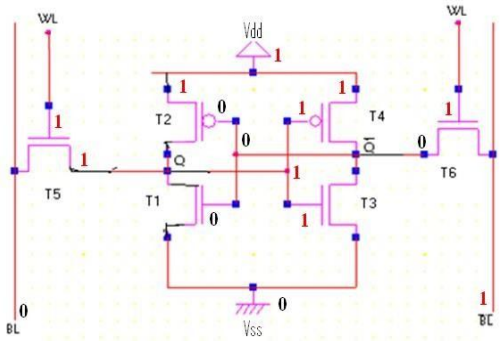

Fig.2: 6T SRAM Cell in read logic 0- operation

Let Q=1, WL=1, $\overline{Q}$=0, BL=0, $\overline{BL}$=1

This activates T5 & T6.

Q=1 is transferred to BL so that BL starts to charge. Hence BL will be 1.

$\overline{BL}$=1 is transferred to *Q* so that $\overline{BL}$ starts to discharge via T6 & T3. Hence $\overline{BL}$ will be 0.

Reading logic 1

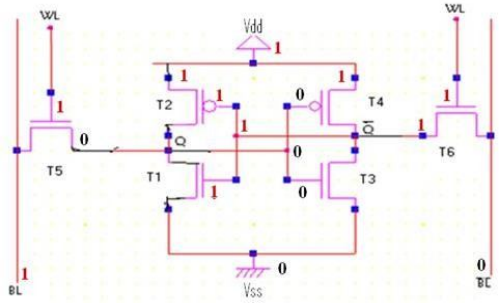

Fig.3: 6T SRAM Cell in read logic 1- operation

Let Q=0, WL=1, $\overline{Q}$=1, BL=1, $\overline{BL}$=0

This activates T5 & T6.
, $\overline{Q}$=1 is transferred to $\overline{BL}$ so that $\overline{BL}$ starts to charge. Hence $\overline{BL}$ will be 1.

BL=1 is transferred to Q so that BL starts to discharge via T5 & T1. Hence $\overline{BL}$ will be 0.

Writing Logic 0

Now Q=0, WL=1, $\overline{Q}$=1, BL=1, $\overline{BL}$=0
T1 & T4 = ON
T2 &T3 = OFF
It means writing of Q=0 has been done.

Writing Logic 1

Now Q=1, WL=1, $\overline{Q}$=0, BL=0, $\overline{BL}$=1
T1 &T4 = OFF
T2 &T3 = ON
It means writing of Q=1 has been done.

5T 1Bit SRAM

By survey it is found that up to 70% of the total active power is dissipated in bit lines discharging / charging during read and write operations [3]. So in proposed work we use only one bit line in SRAM and reduce one NMOS transistor. Due to reduction of one bit line there is saving in power by charging and discharging only one bit line capacitor instead two bit line.

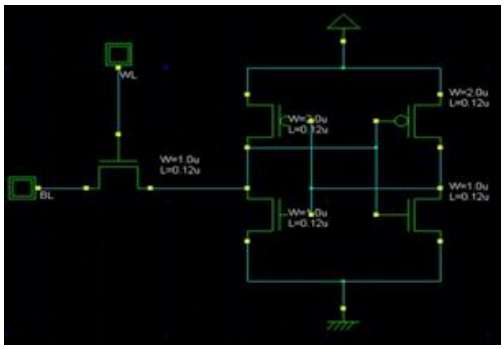

Fig.4: 5T 1Bit SRAM (proposed)

But challenge is this which Transistor should be eliminated. Since Q is the desired output and it is obtained by T5 so that T6 should be the best choice [4]. Now the SRAM is described by 5 Transistors. Now I have proposed a 64 bit 5T SRAM by using 1 bit 5T SRAM in 2.5µm technology and 1.5µm technology and compare with this by a conventional 1bit 6T SRAM and also construct a 64 bit SRAM for 6T SRAM. The access transistors perform communication with the bit lines and the inverters perform the storage element. In the SRAM cell there are three different states it is: standby when the circuit is idle, reading where the data has been requested and writing when updating the contents [6]. The three different states work as follows:

Let Q=0, WL=1, $\overline{Q}$=1, BL=1, $\overline{BL}$=0

This activates T5.

BL=1 is transferred to Q so that BL starts to discharge via T5 & T1. Hence $\overline{BL}$ will be 0.

Writing Logic 0

Now Q=0, WL=1, $\bar{Q}$=1, BL=1,
T1 & T4 = ON
T2 &T3 = OFF
It means writing of Q=0 has been done.

Writing Logic 1

Now Q=1, WL=1, $\bar{Q}$=0, BL=0, $\overline{BL}$=1
T1 &T4 = OFF
T2 &T3 = ON
It means writing of Q=1 has been done.

To design back end we can use Microwind 2.6K version for digital circuit by using Verilog files we can design the digital circuits and then compile. In the Microwind there is automatically generates an error free CMOS layout. By manual drawing Verilog syntax or custom create the layout. Now we verify the CMOS Layout by inbuilt signal simulator and further analyzed for delay, 2D view, 3D view and DRC [9].

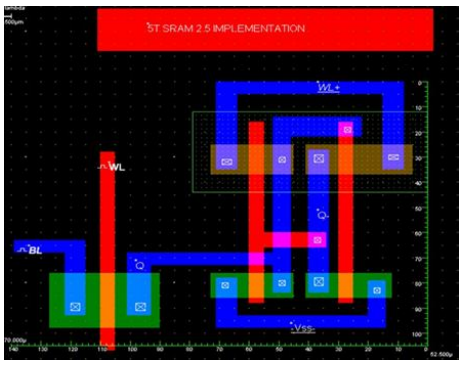

Fig.5: Layout Design of 1-Bit 5T SRAM by Using 2.5µm

Technology by Microwind software

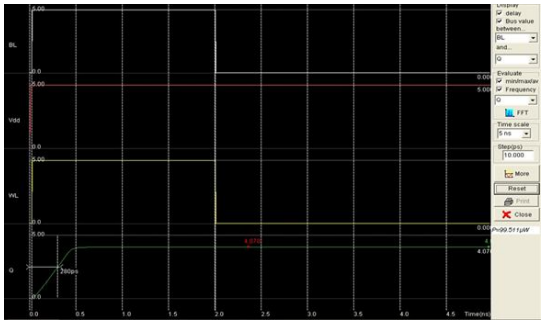

Fig.6: Voltage Vs Time Waveform of 5T 1 Bit SRAM

In the case when use 6T SRAM the parameters are-

1 Power consumption= 0.155mW
2 Layout area= 97.5µm*55µm
3 No. of transistor= 6
4 Leakage currents= $Idd\ (avr)$ = 0.031mA

Now the parameters we found in the case when using 5T SRAM are as follows:

1 Power consumption= 0.99mW
2 Layout area= 70µm*53.5µm
3 No. of transistor= 5
4 Leakage currents= $Idd\ (avr)$ = 0.020Ma

III. COMPARATIVE ANALYSIS

Here in table gives a comparison between 1 bit 5T SRAM and 1 bit 6T SRAM. From this table we can show that 5T 1 bit SRAM consume less power than 6T SRAM. Also 5T SRAM occupy less area and less leakage current than 6T SRAM in both technologies. Also it is shown that 2.5µm is better than 1.5µm because it uses less power, less area and less leakage current. Some parameters in 5T 1 bit SRAM and 6T 1bit SRAM using a 2.5µm and 1.5µm technology.

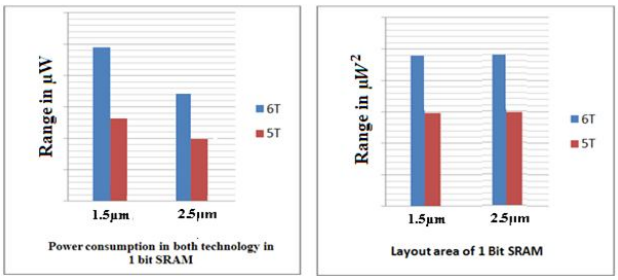

Fig.7: Comparison between 5T SRAM and 6T SRAM for 1 bit only

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