Four Switch Three Phase (FSTP) Sepic Inverter Using PIC Controller

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Abstract- *In this paper, the four-switch three-phase (FSTP) inverter is proposed depending on the topology of the single-ended primary-inductance converter (SEPIC) exclusive of output filter. The main objective of this FSTP is to minimize the cost, complexity, size, and switching losses of the dc–ac conversion system. Since the conventional FSTP inverter usually operates at half the dc input voltage, the output line voltage cannot exceed this value. Compared to conventional FSTP inverter, the proposed FSTP SEPIC inverter provides an improvement in the voltage utilization factor of the input dc supply. The proposed topology makes use of the integral sliding-mode control to optimize its dynamics and to ensure system robustness under different operating conditions. Simulation model and experimental setup are used to validate the proposed approach. Simulation and experimental results show the effectiveness of the proposed inverter.*

Keywords- four-switch three-phase (FSTP) inverter, single-ended primary-inductance converter (SEPIC), Electromagnetic Interference (EMI), common mode voltage (CMV)

I. INTRODUCTION

Researchers mainly concentrate in the development of the efficient control algorithms for high performance variable speed induction motor (IM) drives due to its easy construction, high robustness and generally satisfactory efficiency. Due to the recent development of high speed power semi conductor devices, three phase inverters take part in the key role for variable speed AC motor drives. Traditionally, Three Phase inverters with six switches (SSTP) have been commonly utilized for variable speed IM drives; this involves the losses of the six switches as well as the complexity of the control algorithms and interface circuits to generate six PWM logic signals. So researchers mainly concentrate on the development of new control algorithms to develop a cost effective, simple and efficient high performance IM drive.

During the last decades, many studies have been investigated to reduce the Common mode voltage (CMV) in conventional boost rectifier/inverter. Some of them concentrate in designing several common-mode sinusoidal output filters to reduce both differential and common mode dv/dt at the motor terminal. The others suggested a variety of PWM schemes for reducing CMV in diode as well as rectifier/inverter system. These works have been focused on eliminating zero voltage vector (ZVV) of the PWM scheme by means of using two additional active vectors instead of ZVV in that of the conventional scheme, or shifting active voltage vector of inverter to align to those of the boost rectifier for disappearing one CMV pulse in every control period. Even though CMV can be mitigated by the above methods, they also require a high extra hardware, complexity in its control, or deteriorating reliability and lifetime of system. Recently, the Z-source inverter was proposed and applied to AC machine drive applications. The main advantages of SMC are the fast dynamic response and the guarantee of stability and robustness for large variations of system parameters and against perturbations.

A new hydro energy based dc-dc PFC SEPIC based buck converter is proposed for marine lighting applications thereby achieving high power factor and low THD with higher efficiency. The proposed sepic based power converter is simulated in MATLAB/Simulink environment for verifying the performance of proposed scheme [1]. A soft-switching single-ended-primary-inductance converter (SEPIC) with multi-output sources which increases the conversion efficiency and maximum applicability is proposed. It uses a soft-switching cell with flyback-type to implement the features of ZVS and ZCS under turn-on transitions for the main switch and the auxiliary switch thereb y reducing switching losses and EMI of the switches [2]. A converter design which uses single ended Primary inductance Converter topology that will ensure high performance, low losses for higher switching frequencies, cost efficiency and low electrical stress on the components is proposed [3].

The hybrid solar and wind energy using buck boost and SEPIC converter design to eliminate the higher order harmonics is proposed and neural network control is implemented to get maximum output voltage and efficiency [4]. The SEPIC based inverter with less number of switches as an innovative inverter design to reduced cost and complexity with less switching losses of the DC-AC conversion is proposed. Therefore, the design for the FSTP produced pure sinusoidal without need of filter in output side. The Fuzzy control is adopted with proposed topology to ensure the robustness of the system [5]. A novel converter topology which employs a SEPIC converter and a coupled inductor, with low duty ratios and high turns ratios to achieve high step-up voltage conversion is proposed. It is also focused on the implementation of PI controller to control the speed of the AC motor [6]. A SEPIC type inverter with large voltage gain and high efficiency has been introduced which has the advantages like simple power circuit in less complicated control circuit, and soft switching due to soft switching auxiliary circuit and reduced losses [7]. A novel design for the FSTP inverter as an innovative inverter design based on the topology of the single-ended primary-inductance converter (SEPIC) to reduce the cost, complexity, size, and switching losses of the dc–ac conversion system is proposed [8]. A novel topology two high static gain step-up dc-dc converters based on the modified SEPIC converters which have low switch voltage and high efficiency for low input voltage and high output voltage applications are presented. In addition, the configurations with magnetic coupling and without magnetic coupling are presented and analyzed [9]. A single-phase PV system that provides grid voltage support and compensation of harmonic distortion at the point of common coupling links to a repetitive controller is presented [10]. To study the performance of the switched coupled inductor, high step up DC-DC converter with closed loop control is proposed [11].

A design method is proposed for finding the equivalent inductance and capacitance of the single-ended primary-inductor converter (SEPIC) thereby obtaining the minimum value of the output voltage ripple [12]. The analysis and design of a three-phase high power factor rectifier, based on the dc-dc single-ended primary-inductance converter (SEPIC) operating in discontinuous conduction mode, with output voltage regulation and high frequency isolation is presented [13]. A nonlinear variable-parameter DC-link voltage controller to satisfy both the dynamic characteristic of DC-link voltage control and steady-state compensation performance of a three-phase, four-wire shunt active power filter (APF) is proposed [14]. A novel configuration is proposed with a y/y step-up transformer adding to AC side of the four-switch three-phase (FSTP) active power filter (APF), so as to improve the utilization of DC voltage and further widen the voltage range of FSTP APF. Variable parameter pulse width modulation (VPPWM) approach is proposed to ameliorate the current tracking performance of the FSTP inverter [15].

II. METHODOLOGY

Fig.1 shows the block diagram of the proposed system in which the SEPIC based Three phase inverter transforms DC input to AC to supply the three phase load. This transformation takes place when the PWM signal is received from the PIC Microcontroller unit. The isolator and driver circuit is used to separate the control circuit and inverter module and to drive it. The proposed FSTP SEPIC inverter consists of two SEPIC converters, and achieves dc–ac conversion as explained by connecting two phases of the three-phase load to the output of two dc–dc SEPIC converters which are sinusoidally modulated while the third phase is directly connected to the input dc source. Both SEPIC dc–dc converters produce a dc-biased sinusoidal wave output, so that each converter produces a unipolar voltage.
To generate three-phase balanced load voltages, the sinusoidal modulation of each converter is 120° shifted and the dc-bias is exactly equal to the input dc voltage. Some advantages of the FSTP inverter over the conventional SSTP inverter such as, reduced price due to reduction in number of switches, reduced switching losses, reduced number of interface circuits to supply logic signals for the switches, simpler control algorithms to generate logic signals, less chances of destroying the switches due to lesser contact among switches and less real time computational burden.

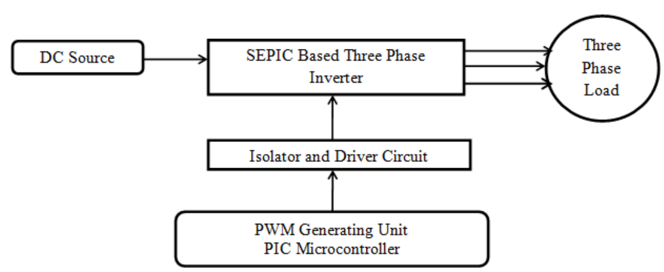

Fig. 1 Block diagram of proposed system

Fig. 2 depicts the Block Diagram of Proposed PFC SEPIC Converter for Marine Lighting Applications. It consists of the components like Hydro Turbine, Permanent Magnet Synchronous Generator (PMSG), Passive Rectifier, SEPIC Power Factor Correction (PFC) Converter and DC lighting load. Tidal wave energy is converted into mechanical energy with the help of a hydro turbine which drives a PMSG to produce three phase AC output voltage. Passive diode rectifier converts this low AC voltage into DC and then DC voltage is fed to SEPIC converter for voltage regulation as well as to improve quality of power supply such as high power factor, low Total Harmonic Distortion (THD).

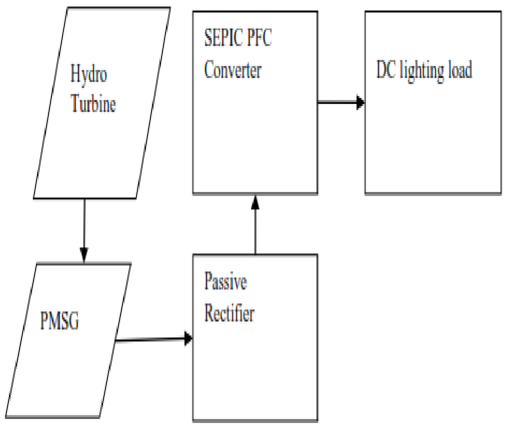

Fig. 2 Block Diagram of Proposed PFC SEPIC Converter for Marine Lighting Applications

Since the load is connected differentially across the two converters and the dc input supply, a dc bias appears at each end of the load with respect to ground. In addition, the differential dc voltage across the load is zero and the voltage generated across the load is a bipolar voltage, which necessitates the dc–dc SEPIC converters to be current bidirectional. The bidirectional SEPIC dc–dc converter is shown in fig.3 while the detailed configuration of the proposed FSTP SEPIC dc–ac inverter is shown in fig. 4.

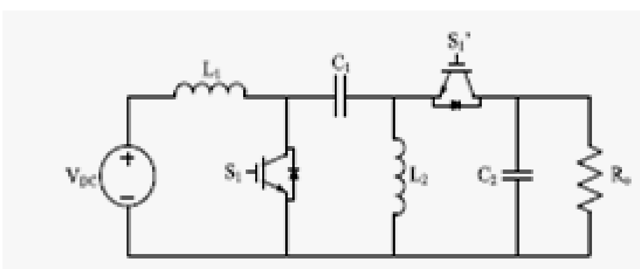

Fig.3 Bidirectional of SEPIC inverter

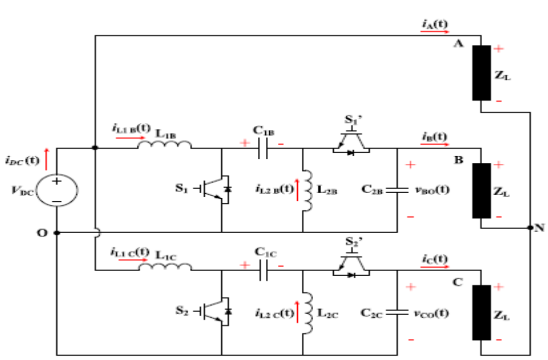

Fig.4 proposed FSTP SEPIC inverter

The bidirectional SEPIC converter includes dc input voltage V_{dc}, input inductor L_1, two complementary bidirectional power switches S_1, $S_{1'}$, coupling capacitor C_1, output inductor L_2 and output capacitor C_2 feeding a load resistance R_0. SEPIC operation core implies charging the inductors L_1 and L_2 during the ON state of the switching period taking the energy, respectively, from the input source and from the coupling capacitor C_1,and discharging them simultaneously into the load through the bidirectional switch $S_{1'}$ during the OFF state of the switching period.

The output voltage of the SEPIC dc–dc converter may be less or more than the input voltage depending on the duty cycle and is given by

$$V_0 = \frac{D}{1-D} V_{in} \qquad (2.1)$$

Where D is the duty cycle, while V_{in} and V_o are the input and output voltage of the converter, respectively. The sinusoidal modulation of each SEPIC converter implies that the reference voltage of each converter with respect to the ground is given by

$$V_{bo}(t) = V_{dc} + V_{bref} = V_{dc} - V_{ml-L}\sin(\omega t) \qquad (2.2)$$

$$V_{co}(t) = V_{dc} + V_{cref} = V_{dc} + V_{ml-L}\sin(\omega t + 2\pi/3) \qquad (2.3)$$

where V_{ml-L} is the peak of the desired line to line output voltage, while ω is the desired radian frequency.

Thus, based on Kirchhoff's voltage law in the output line voltages across the load are given by,

$$V_{ab}(t) = V_{dc} - [V_{dc} - V_{ml-L}\sin(\omega t)] = V_{ml-L}\sin(\omega t) \qquad (2.4)$$

$$V_{bc}(t) = V_{dc} - V_{ml-L}\sin(\omega t) - V_{dc} + V_{ml-L}\sin(\omega + 2\pi/3) = V_{ml-L}\sin(\omega t - 2\pi/3) \qquad (2.5)$$

$$V_{ca}(t) = V_{dc} + V_{ml-L}\sin(\omega t + 2\pi/3) - V_{dc} = V_{ml-L}\sin(\omega t + 2\pi/3) \qquad (2.6)$$

Although the FSTP SEPIC inverter can give an output line voltage upto a value equals the voltage of the input source (V_{dc}), however, it is recommended to define V_{ml-L} lower than the value of the input dc voltage to avoid operating at zero duty cycle (i.e., minimum duty cycle is selected to be slightly higher than zero).

For successful dc–ac conversion, accurate selection of passive elements of SEPIC converter is necessary and requires knowledge of the instantaneous capacitors voltages and inductors currents. The voltage across the output capacitors is given by (2.5). Based on the basics of dc–dc SEPIC converter, the average voltage across the coupling capacitor is equal to the input dc voltage, while the current through the output inductor is equal to the output load current as indicated in (2.7) and (2.8)

$$V_{c1b}(t) = V_{c1c}(t) = V_{dc} \tag{2.7}$$

$$i_{L2B}(t) = i_B(t),\ i_{L2C}(t) = i_C(t). \tag{2.8}$$

where $i_{L2B}(t)$ and $i_{L2C}(t)$ are the output inductor currents of both SEPIC converters, while $i_B(t)$ *and* $i_C(t)$ are the instantaneous load currents drawn by phase B and phase C, respectively. The load phase currents are given by

$$i_A(t) = I_m \sin(\omega t - \varnothing - \pi/6) \tag{2.9}$$

$$i_B(t) = I_m \sin(\omega t - \varnothing - 5\pi/6) \tag{2.10}$$

$$i_C(t) = I_m \sin(\omega t - \varnothing + \pi/2) \tag{2.11}$$

where I_{mis} the peak value of load current, and $\varnothing$ is the phase of the load impedance (Z_L).

The input inductor current for both SEPIC converters can be obtained by applying energy balance rule for each SEPIC converter. Assuming ideal converters, the input inductor currents for both converters are given by

$$i_{L1B}(t) = \frac{i_B(t) v_{B0}(t)}{V_{DC}} = i_B(t) \frac{V_{DC} - V_{mL-L}\sin(\omega t)}{V_{DC}} \tag{2.12}$$

$$i_{L1C}(t) = \frac{i_C(t) v_{C0}(t)}{V_{DC}} = i_C(t) \frac{V_{DC} + V_{mL-L}\sin(\omega t + 2\pi/3)}{V_{DC}} \tag{2.13}$$

where $i_{L1B}(t)$ and $i_{L1C}(t)$ are the input inductor currents of both SEPIC converters connected to phase B and phase C, respectively as shown in Fig. 2.3.

The input power drawn by each SEPIC could be obtained by calculating the average value of the input inductor current for each converter. The average values of the input inductor currents for both SEPIC converters (I_{L1C} and I_{L1B}) are given by,

$$I_{L1B} = -i_{L1B} = -V_{ml} -_{\text{Lim2}} V_{dc}\cos(\varnothing + 5\pi/6) \tag{2.14}$$

$$I_{L1C} = -i_{L1C} = V_{ml} -_{\text{Lim2}} V_{dc}\cos(\varnothing + \pi/6) \tag{2.15}$$

From (2.14), it is clear that the average value of both input inductor currents are equal only at a unity power factor ($\varnothing$ = 0, pure resistive load). In this case, both SEPIC converters will transfer the same amount of power to the load side. Otherwise, the average currents are not equal (according to (2.14)), i.e., SEPIC converters will transfer different amount of power to the load side.

Referred to Fig. 4, the dc input current of the proposed inverter topology, i_{DC}(t) is equal to the summation of the load current drawn by phase A, $i_A(t)$ and the input inductors currents of both SEPIC converters, $i_{L1B}(t)$ and $i_{L1C}(t)$ as follows:

$$i_{DC}(t) = i_A(t) + i_{L1B}(t) + i_{L1C}(t)$$
$$= i_A(t) + i_B(t)\frac{V_{DC} - V_{mL-L}\sin(\omega t)}{V_{DC}} + i_B(t)\frac{V_{DC} + V_{mL-L}\sin(\omega t + 2\pi/3)}{V_{DC}} \tag{2.16}$$

Where $i_A(t)$ is the load current of phase A as described in (2.13), which is drawn directly from the dc input source. Substituting (2.12) and (2.13) into (2.16), the dc supply current could be given in the following form:

$$i_{DC}(t) = \frac{\sqrt{3} V_{mL-L} I_m}{2 V_{DC}} \sin\left(\theta + \frac{\pi}{2}\right) \tag{2.17}$$

Equation (2.17) shows that the dc supply current drawn by the proposed inverter topology is constant.

III. HARDWARE DESCRIPTION

This Hardware is designed with a microcontroller dsPIC30F2010 followed by an opto isolator which acts as an isolation between the power circuit and the control circuit, a MOSFET driver is connected with a Optocoupler to provide the required switching voltage levels for the circuit. The working register array of dsPIC30F2010 consists of 16x16-bit registers, each of which can act as data, address or offset registers. One working register (W15) operates as a software stack pointer for interrupts and calls. The data space is 64 Kbytes (32K words) and is split into two blocks, referred to as X and Y data memory. Each block has its own independent Address Generation Unit (AGU). Most instructions operate solely through the X memory AGU, which provides the appearance of a single unified data space.

The Multiply-Accumulate (MAC) class of dual source DSP instructions operates through both the X and Y AGUs, splitting the data address space into two parts. The X and Y data space boundary is device specific and cannot be altered by the user. Each data word consists of 2 bytes, and most instructions can address data either as words or bytes. The dsPIC core has a 16-bit status register (SR), the LS Byte of which is referred to as the SR Low Byte (SRL) and the MS Byte as the SR High Byte (SRH).

3.1 PIC MICROCONTROLLER

3.1.1 dsPIC (30F2010) Microcontroller

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory. Easy Programming and Erasing are other features of dsPIC30F2010.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

Microcontroller is a general purpose device, which integrates a number of the components of a microprocessor system on to single chip. It has inbuilt CPU, memory and peripherals to make it as a mini computer. A microcontroller combines on to the same microchip:

- The CPU core
- Memory(both ROM and RAM)
- Some parallel digital I/O

3.1.2 Accessories

- A timer module is used to allow the microcontroller to perform tasks for certain time periods.
- A serial i/o port is used to allow data to flow between the controller and other devices such as a PIC or another microcontroller.
- An ADC is used to allow the microcontroller to accept analogue input data for processing.

3.2 MOSFET Driver circuit

In this work, IRF540N MOSFET is used in the converter section. A Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a recent device developed by combining the areas of Field-Effect concept and MOS technology. The MOSFETs are used as controllable device (i.e.) these devices can be turn on and turned off by the application of control signals.

3.3 OptoIsolator

It is a small device that allows the transmission of a signal between parts of circuit while keeping those two parts electrically isolated. Inside a typical optocoupler there are two things – a LED and a phototransistor. When a current runs through the LED, it switches on - at which point the phototransistor detects the light and allows another current to flow through it. And then when the LED is off, current cannot flow through the phototransistor. All the while the two currents are completely electrically isolated (when operated within their stated parameters).

3.4 Pulse-Width Modulation (PWM) Generating unit

Pulse-width modulation (PWM) is a commonly used technique for controlling power to an electrical device, made practical by modern electronic power switches. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power.

Typically switching have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies The term duty cycle describes the proportion of on time to the regular interval or period of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on the main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM works also well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.PWM has also been used in certain communication systems where its duty cycle has been used to convey information over a communications channel.

3.5 Schematic model

Fig.4 shows the Hardware Schematic model of the proposed system which comprises of dsPIC (30F2010) Microcontroller, MOSFET Driver circuit, OptoIsolator and Pulse-Width Modulation (PWM) Generating unit.

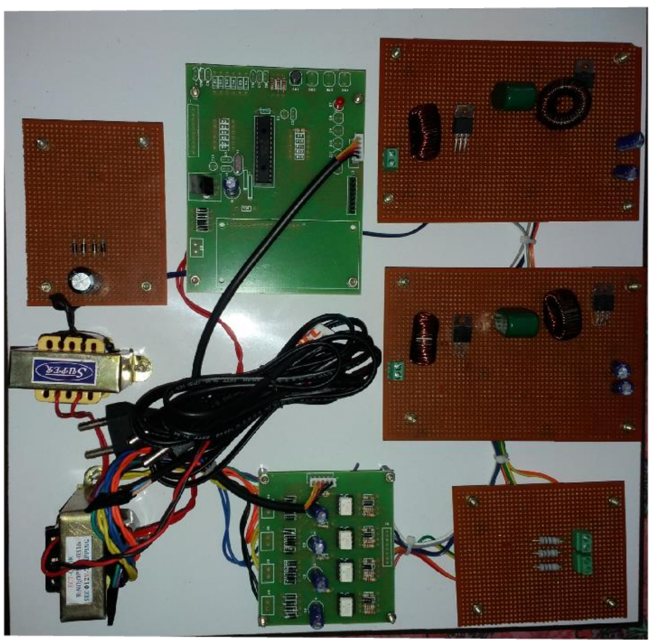

Fig.4 Hardware Schematic model of the proposed system

IV. SIMULATION DIAGRAM

Fig.5 shows the simulation diagram of the proposed system in MATLAB/SIMULINK. Simulink, developed by Math Works, is a communication tool for modeling, simulating and analyzing multi-domain dynamic systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in control theory and digital signal processing for multi-domain simulation and Model-Based Design. In this simulation diagram, the IGBT/Diode module is used to generate PWM pulses. Simulink model can be connected to hardware for rapid prototyping, hardware-in the-loop (HIL) simulation, and deployment on an embedded system.

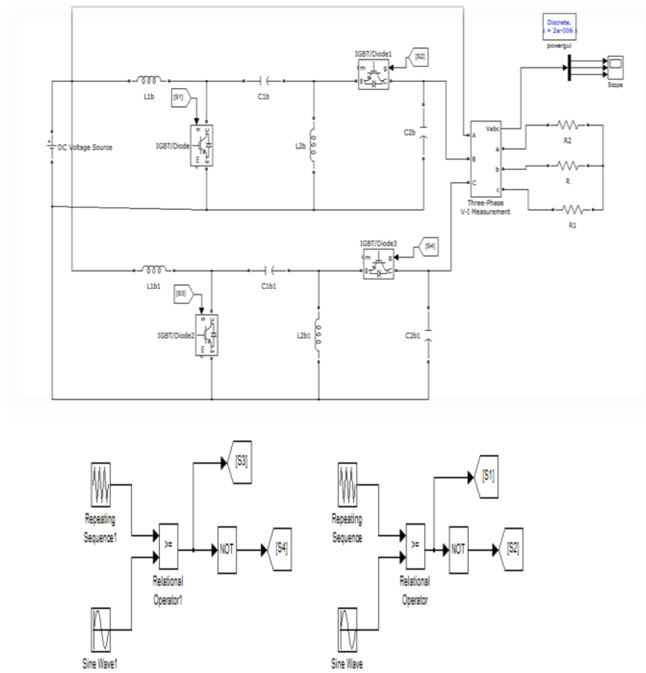

Fig.5 Simulink diagram of SEPIC input

V. RESULTS AND DISCUSSION

For line-to-line voltage peak of 86.66% of the dc input voltage, the normalized load current drawn by phase A [$i_A(t)/I_m$], normalized input inductor current for each SEPIC converter [$i_{L1B}(t)/I_m$ and $i_{L1C}(t)/I_m$], and the normalized dc input current [$i_{dc}(t)/I_m$] are shown in Fig. 6 for different load power factors. At unity power factor, the input currents of both SEPIC converters are symmetrical with the same average value as shown in Fig. 6(a). At lagging/leading power factors, the input currents of both SEPIC converters have different waveforms with unequal average values as shown in Fig. 6(b) and (c), respectively.

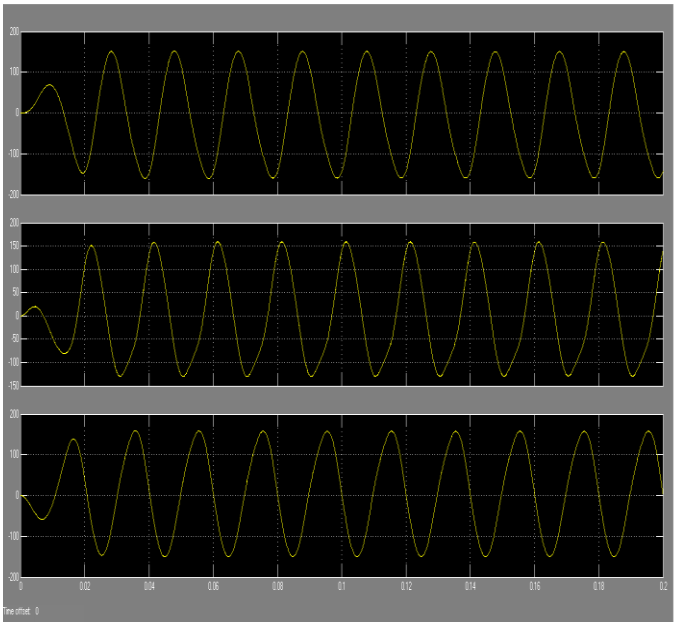

Fig.6 simulation output

VI. CONCLUSION

In this paper, a dc–ac FSTP SEPIC-based inverter is proposed which improves the utilization of the dc bus by a factor of two compared to the conventional FSTP voltage source inverter. Also, it can produce three-phase output voltages that are pure sinusoidal waves without a need for an output filter. Unlike conventional FSTP inverter, the proposed inverter does not suffer from the problems of voltage fluctuation across the dc link split-capacitors, as the third phase load current is directly drawn from the dc source without circulation in any passive component. An SMC with fixed switching frequency was designed and applied to the proposed SEPIC inverter with two different sliding surfaces called integral sliding-mode and double integral sliding-mode (DISMC). It was found that compared to ISMC, the DISMC can eliminate the steady-state error of the state variables by adding double-integral term of these errors in the sliding surface. Simulation and experimental results verified the performance of the proposed inverter with the recommended control strategy.

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