A Novel Design of RRAM Based Nonvolatile Lookup Table (nvLUT)

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Abstract- *The present work proposes a novel design of RRAM based Nonvolatile Lookup Table (nvLUT).Resistive random access memory (RRAM) is a perfect option to replace static random access memory (SRAM) in lookup table (LUT) design for its high density, non-volatility and low power consumption.The overall architecture of nvLUT consists of a RRAM slice, a tree multiplexer (TMUX), Matched reference path (MRP) and Sense Amplifier.Inputs to TMUX selects its output, based on the Truth table saved in RRAM and parallely MRP senses reference signal. This MRP and TMUX output is compared and amplified by sense amplifier and gives final output. Proposed Design reduces transistor count and power along with PDP*

Keywords- Low power, nonvolatile lookup table(nvLUT),RRAM

I. INTRODUCTION

The non-volatile field programmable gate array (FPGA) is a promising candidate for the low-power computing due to its flexibility. However, the non-volatile devices have a critical drawback of reliability due to the process variations in read operation.

SRAM-based subject-programmable gate arrays (FPGAs) have been extensively used during the last decades. but, the volatility of SRAM has constrained FPGAs in programs where excessive safety and instant power-on are required [1]. The problem may be solved by introducing nonvolatile memory (NVM) as the configuration bit. However, the conventional NVM device, which include antifuse, E2PROM, and flash, require excessive-voltage process and have terrible logic compatibility [2], [3], thus limiting the logic density and increasing the integration cost of FPGAs. Based on the logic-in-,memory concept, lookup table, which is the core building block in FPGAs, has been expected with nonvolatility. First, various nonvolatile SRAM(nvSRAM) structures with MRAM and RRAM were proposed to directly replace SRAM in the conventional lookup table to obtain nonvolatility [5]–[7]. However, the size of nvSRAM cell is extremely larger than that of SRAM, and the write annoyance is also difficult to avoid for half-select RRAM cells. For MRAM, Suzuki et al. Zhao et al. [10] proposed MRAM-based nvLUT for run-time reconfiguration.sed an another Chen et al. [13] proposed another RRAM-based nvLUT using crossbar array. However, the sneaking paths innate in crossbar array bring considerable leakage and poor sensing margin of only 10 mV. To sum up, none of the preceding work has achieved high consistency against memory and logic variations, low power, high-area efficiency, and low leakage at the same time.

This quick introduces a low-energy version-tolerant nvLUT circuit to conquer the issues inside the preceding work. RRAM era has made giant development within the beyond decade as a competitive candidate for the subsequent generation non unstable memory (NVM).because of its huge ROFF/RON, 1T1R RRAM cell is used as a configuration bit and a reference resistor to provide sufficient sense margin beside reminiscence and common sense versions. consequently, the region value is reduced because no parallel or serial memory mobile mixtures are required to assurance the feel margin. To lower the energy and location, unmarried-stage experience amplifier with voltage clamp (SSAVC) is employed without compromising the reliability. furthermore, matched reference path (MRP) is devised to minimize the parasitic RC mismatch between the chosen path inside the multiplexer and the reference path for regular sensing towards logic variations. subsequently, detailed estimation is carried out to verify the benefits.

To achieve low power, less area, High speed etc, conventional CMOS can be replaced by GDI. The GDI technique is used to reduce transistor count along with decreasing delay and power [2] [11].Simple logic gates like X-OR, X-OR, AND, OR etc can be implemented with smaller area, power and delay as compared to Static CMOS, existing PTL, DPL, HPSC etc.

The remainder of this brief is organized as follows. Section II. Proposed low-power variation-tolerant nvLUT. Section III Evaluation and analysis presents the related work. Sections IV and V provide GDI implementation and simulation results for the proposed adder. Section VI draws the conclusion.

II. PROPOSED LOW-POWER VARIATION-TOLERANT nvLUT

To illustrate the proposed design, a two-input nvLUT is offered, as proven in Fig. 1. The input count number also can be clearly extended to six, that is winning in modern-day fundamental-movement FPGA merchandise [14]. The overall architecture of nvLUT consists of an SSAVC, a tree multiplexer (TMUX), an MRP, a RRAM slice, and a footer transistor. The RRAM slice constitutes of four 1T1R RRAM cells at the left for configuration and a dummy RRAM cell at the right-maximum as a reference resistor. The truth desk is saved in the RRAM slice in the shape of resistance kingdom, ROFF or RON, which isn't the same as the logic voltage in SRAM. as an example, so as to software th e nvLUT as a NOR gate, R0 have to be programmed as RON denoting 1, while R1, R2, and R3 ought to be programmed as ROFF denoting zero. The inputs IN0 and IN1 pick out the corresponding RRAM cell via TMUX. To perform the operations of LUT, the sense amplifier is employed to convert the resistance kingdom of RRAM cell into good judgment voltage. The characteristic of footer transistor MF is to allow modern-day to go with the flow at some stage in sensing and it's miles closed all through precharge to restrain leakage.

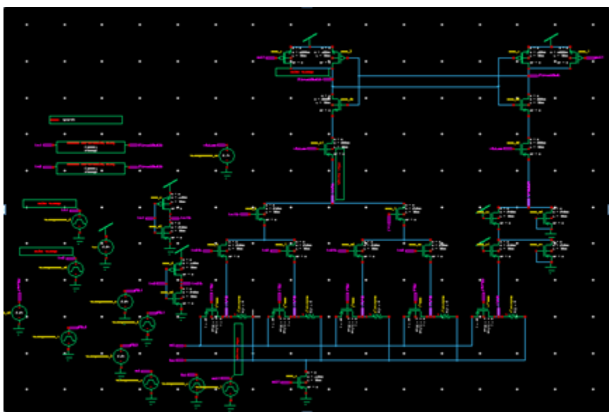

Fig.1.Overall architecture of the proposed low power variation tolerant nvLUT based on RRAM.

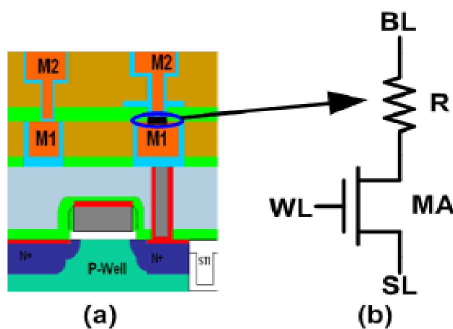

Fig.2.1T1R RRAM cell integration process and structure. (a) Cross-sectional view. (b) Schematic.

A. RRAM as a Configuration Bit and a Reference Resistor

The 1T1R RRAM cell is used as a configuration bit and a reference resistor which give sufficient sense margin, as shown in Fig.1. Different from crossbar array, a 1T1R RRAM cellular can lower the sneaking present day and the disturbances all through write and examine, as a consequence saving energy and obtaining high yield. the typical RON and ROFF of RRAM are of kilo-ohms and megaohms, respectively, and ROFF/RON is over a hundred, that's at the least forty× large than that of MRAM. Consequently, adequate feel margin is guaranteed and the configuration sources are also saved by way of half compared with the parallel or serial combination scheme. furthermore, the RRAM garage layer, i.e., R0-three and Rref , is stacked within the lower back-cease of line without occupying an extra vicinity, as shown in Fig.1 .due to the fact the characteristics of RRAM are distinct from traditional resistor, the sense margins of RON and ROFF as compared with a conventional reference resistor may undergo uneven adjustments below memory and good judgment process variation, which can also result in read failure. To resolve this trouble, dummy RRAM cellular, which is programmed to a mid-state resistance, is followed as the reference resistor. hence, the configuration bits and reference resistor range inside the equal way throughout extraordinary temperatures and approach situations, retaining the sense margins for both RON and ROFF. moreover, the dummy cellular occupies less area than traditional resistors. The peripheral decoding and writing circuits for dummy cell also can be shared with configuration bits, bringing a whole lot less place overhead. In our proposed nvLUT, considering WL, BL, and SL are all drawn out from the RRAM slice, each unipolar and bipolar RRAM can be programmed by means of using enforcing set or reset voltage on BL or SL at the equal time as activating the corresponding WL. Because of the reality the dummy RRAM cellular with a mid-nation resistance is used because the reference, the accompanied RRAMs have to help the trimming of its garage resistance to a particular charge. on this brief, that allows you to evaluate our proposed nvLUT, we use the bipolar CuxSiyO RRAM with the forming/set/reset voltage of two.five/2/−1 V. the usage of a self-adaptive-write-mode (SAWN) with well timed comments and affirm for the duration of programming , the dummy cell can be trimmed to a selected storage resistance. even though the persistence of RRAM is inside the order of 106, it however suffices because the configuration reminiscence in nvLUT as reprogramming handiest takes region while the configuration data is changed.

RRAM cell operations

The proposed RRAM cell consists of an NMOS switch transistor (cell transistor) based resistive memory

device. The RRAM device employs AlCu (top metal that connects the up-terminal of the device to the bitline), TiN (titanium-nitride electrodes), Ti (the film between the top electrode and the insulator), HfO_2 (as the insulator), and W (contact that connects the drain of MOS and the down-terminal of the RRAM device. In the initial state, the RRAM device requires a forming procedure to set the RRAM cell to a low resistive state before regular read and write operations.

There are two types of write operations for the proposed 1T1R (one transistor, one resistor). RRAM: set (write-0) and reset (write-1). The set operation changes the RRAM device from a high resistive state (HRS) to a low resistive state (LRS)by applying a set voltage (VSet) on the bitline (BL) and 0 V to the source terminal of the NMOS switch. The reset operation changes the RRAM device from LRS to HRS by applying a reset voltage (VReset) to the source terminal of the NMOS switch, and 0 V to the BL.

B. SSAVC

SSAVC converts the resistance state of RRAM right into a rail-to-rail logic voltage. As proven in Fig. 1, transistors M3–M6 represent of a latch amplifier. Transistors M1 and M2 are used to precharge the output nodes OUT and OUTB to VDD when CLK is low and transistor MF is used to initiate the conversion while CLK is excessive. compared with the previous -stage feel amplifier [8], the single-level cognizance occupies less die area. The inner voltages in TMUX and MRP are clamped to decrease voltages by using the clamp transistors to save electricity. In previous paintings, the inner nodes of the selected course in multiplexer and reference course are each precharged to VDD or (VDD-Vth) whilst CLK is low .Then, the prices are discharged to a capacitor or ground while CLK is excessive, ensuing in considerable electricity waste. to alleviate this problem, transistors M7 and M8 are inserted among the experience amplifier and the TMUX/MRP. via applying a right clamp voltage Vbias, that is lower than VDD, on the gates of M7 and M8, the inner nodes of the chosen course in TMUX and MRP can best be precharged to (Vbias-Vth). In an FPGA chip, Vbias for one of a kind nvLUTs may be generated by means of a single voltage regulator with negligible overhead and it may additionally be tuned for one-of-a-kind PVT situations. because of the quadratic courting among power and voltage, extensive common power saving may be performed by the reduction of precharge voltage. even though the voltage clamp may incur decreased currents into the sense amplifier, large ROFF/RON of RRAM nonetheless allows to maintain the feel margin without impairing the reliability.

C. MRP

Although trimming Rref with the aid of SAWM can help to disabuse the parasitic resistance mismatch between the selected route in TMUX and the reference course, their parasitic capacitance mismatch can't be effortlessly estimated and compensated. The MRP is devised to reduce the parasitic RC mismatch among the above-cited two paths. To illustrate this factor, IN0 and IN1 are assumed to take the good judgment values of 0 and 1, respectively. As proven in Fig. 1, the path marked by the inexperienced dash line in TMUX, P01, is selected to be in comparison with the reference path, Pref . For reliable sensing, the parasitic RCs of P01 and Pref need to be equivalent. consequently, the transistors MP8 and MP10 with their gate grounded are, respectively, added on the nodes B and D in MRP to mimic the parasitic effects of OFF-nation transistors MP2 and MP3 on the nodes A and C in TMUX. moreover, the transistors in MRP take the equal size with the bypass transistors in TMUX.

III. RELATED WORK

In this method, power dissipation has become a significant and very important constraint in electronic trade. Several techniques were already introduced to scale back power dissipation. Gate Diffusion Input (GDI) technique permits power dissipation to a larger extend compared to the opposite logic designs. This method additionally reduces the semiconductor device count and so the world of the circuit. so the circuit are going to be a lot of less complicated and straightforward to manage.

A) *GDI Technique*

The gdi approach makes use of easy mobile as proven in fig 3.This simple gdi cell is a conventional cmos inverter, but there are some changes made they may be:

i)The 3 inputs of gdi cellular are: p (input to the source/drain of pmos),g (commonplace gate input of nmos and pmos) and n (enter to the supply/drain of nmos).

ii) In assessment with a conventional cmos inverter bulks of both nmos and pmos are connected to n or p (respectively) and can be biased.

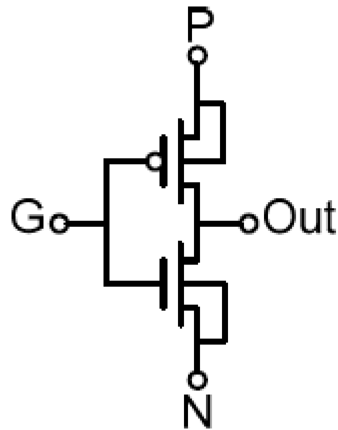

Fig. 3: Basic GDI Cell

This function cannot be implemented using standard p-well CMOS process. It can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies. Table I shows logic function of GDI cell.

TABLE I: Logic function of GDI cell

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+ B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B + AC	MUX
0	1	A	A'	NOT

III. EVALUATION AND ANALYSIS

Because of big ROFF/RON of RRAM, it is straightforward to make certain the reliability of the proposed nvLUT. consequently, our priority is to decide Rref and Vbias via the strength-delay product. For evaluation, the input remember is extended to six to comply with the mainstream FPGA products. The evaluation is carried out in 90-nm logic process and the paper.

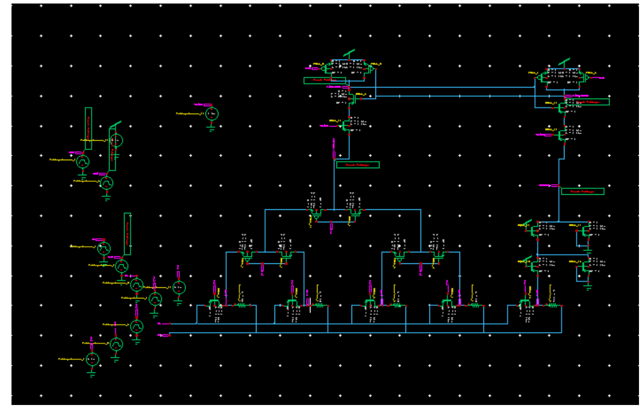

Fig.4.Low power variation tolerant nvLUT based on RRAM using GDI cell

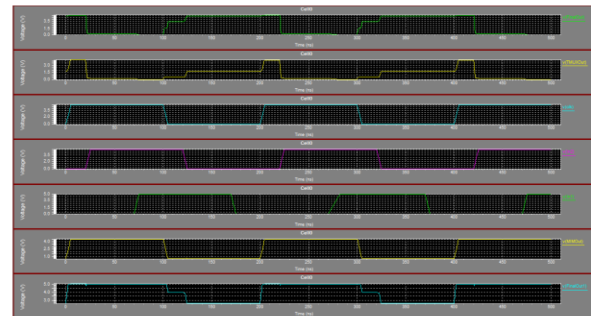

Fig. 4: Simulation result of GDI based nvLUT

SIMULATON RESULTS:

Design of RRAM based LUT is implemented as an optimized version of nvLUT and an experimental study has been performed. The performance of the proposed design is measured by four parameters: Speed or Delay, Power, Area and Power Delay Product (PDP) and compared with the conventional design. The circuit simulation of RRAM based LUT is carried out using Tanner EDA tool with 90nm technology file. Proposed RRAM based LUT is compared with existing nvLUT to prove the performance of proposed design. Schematic design of circuit is carried out in S-edit of Tanner EDA tool vs13.Simulation results are shown in fig.

Transistor count comparison of LUT with different SRAMs and LUTs is given in Table VI. It is reflected that around 28 transistors are required to design RRAM based nvLUT but only 23 transistors are required for the implementation of the proposed LUT design, showing the reduction of 4 transistors, and hence reducing 15% area than RRAM based nvLUT design.

Parameters	Conventional LUT	Proposed GDI LUT
Transistor Count	28	23
Power (µW)	5.12	4.97
Delay (ns)	1.07	9.97
PDP (*10^(-15) J)	5.47	4.95
Vdd	1.2V	1.2V

It is clear from Table that the power dissipation in proposed LUT is 4.98 µW for 5MHz as compared to 5.12 µW of RRAM based nvLUT owing to the reduction in switching power and short circuit power. Also the results show that the delay of proposed LUT at 5MHz is 9.97ns and that of RRAM based nvLUT is 1.07ns.

PDP is defined as average energy consumed per switching event. It is product of power and delay. PDP of the RRAM based nvLUT has 4.95J but that of proposed LUT is 5.47 J.

IV. CONCLUSION

The design techniques of low-power variation-tolerant nvLUT are described on this quick. RRAM is followed as the configuration bit and the reference resistor to provide massive feel margin, consequently alleviating the outcomes of reminiscence and common sense technique variations. Because of the excessive ROFF/RON of RRAM, SSAVC helps to lessen the power and place without impairing the reliability. The MRP is also devised to reduce the parasitic RC mismatch among the chosen path in the multiplexer and the reference path for dependable operation. by means of assessment, first rate upgrades in energy, delay, area, and reliability are performed.

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