Combined LMS-LMF Based Control Algorithm of DSTATCOM For Power Quality Enhancement In Distribution System

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Abstract- *This paper deals with the combined Least Mean Square-Least Mean Fourth (LMS-LMF) based control algorithm for DSTATCOM (Distribution Static Compensator) in three phase distribution system to alleviate the power quality problems caused by solid state equipments and devices. The combined LMS-LMF based algorithm is simulated using Sim Power System (SPS) toolbox in MATLAB for obtaining the corresponding active and reactive weights and supply reference currents. The proposed control algorithm has advantages of both LMF and LMS based control algorithms which helps in fast and accurate response with a robust design. Depending on the value of error signal obtained in any of the phases either of LMS or LMF based control is used to minimize the error. The developed combined LMS-LMF based algorithm is implemented on the prototype of proposed system and responses obtained are found satisfactory with harmonic spectra of the supply currents meeting the power quality standards.*

I. INTRODUCTION

COMFORT and sophisticated lifestyle has been on a exponential run since the invention of the solid state devices. The recent inventions and the new technologies in solid state equipments and devices have led to a very peaceful and smooth life but it increases the power quality problems due to these solid state devices based loads. Power quality problems are of major concern in the distribution system which leads to decrease in efficiency of the system and a serious attention is to be given to the increasing power pollution. The abundant uses of nonlinear loads such as solid state power conversion devices, medical equipment, fluorescent lighting, renewable energy systems, office and household equipment, HVDC (High

Voltage Direct Current) transmission, electric traction, arc furnaces, high frequency transformers, etc inject harmonics into the system and decline the quality of power. Moreover,due to unbalanced three phase or single phase loads, the nature of waveforms in the distribution system is disturbed which eventually affects the equipment and users nearby. Recent research on power quality focuses on mitigation of current quality problems like harmonics elimination, power factor correction, load balancing, noise cancellation and voltage quality problems like sag, swells, impulses, voltageunbalances, fluctuations and various other aspects.

Custom power devices (CPD) i.e. DVR (Dynamic Voltage Restorer), DSTATCOM (Distribution Static Compensator), and UPQC (Universal Power Quality Conditioner) are alternatives to mitigate theses current and voltage based power quality problems .

As the current based power quality issues are major concern in the distribution system due to solid state based loads, voltage source converter (VSC) based DSTATCOM is the suitable technology and/ or solution to mitigate all these problems in addition to classical or existing mitigating technology like static Var compensators, power capacitors etc. Various topologies of DSTATCOM have been discussed in the literature and a wide area of research is open to work on the power quality issues. DSTATCOM also finds applications in electric ship power systems, microgrid , distributed generation etc.

For the appropriate operation of VSC based DSTATCOM, a proper control is required. So one builds algorithm for generating the appropriate pulses for VSC to overcome the current based power quality problems. These algorithms are designed either in frequency domain or in time domain based on the type of process they choose to generate the pulses for the devices of VSC. Singh et. al. have well explained various configurations and control algorithms such as: unit template, PBT (power balance theory), I-cosΨ, CSD theory (Current Synchronous Detection), IRPT (Instantaneous Reactive Power theory), SRF (Synchronous Rotating Frame) theory, ISC (Instantaneous Symmetrical Components) theory, single PQ theory, single DQ theory, neutral network LMS (Least Mean Square) adaline based control algorithm for DSTATCOM in both PFC (power factor correction) and ZVR

(zero voltage regulation) mode. Singh et. al. have also designed new control for the DSTATCOM with improved performance with conventional algorithm such as leaky LMS algorithm, composite observer algorithm , adaptive theory based improved linear sinusoidal tracer algorithm, SPD (simple peak detection) theory algorithm, back-propagation algorithm, Learning-based anti-hebbian algorithm , hyperbolic tangent function based LMS algorithm , kernel incremental metaconvergence algorithm , and variable forgetting factor recursive least square algorithm. All these algorithms are designed for ZVR and PFC for the particular system. This is achieved by extracting the reference supply currents from the sensed signals of the system and then comparing them with the observed supply currents to produce the required pulses for the VSC. Luo et. al. have designed improved DPC (direct power control) algorithm based on deadbeat current controller and double deadbeat current controller. Kumar et. al. have also designed the controller for DSTATCOM with improved power quality such as voltage controlled DSTATCOM, multifunctional DSTATCOM with new control algorithm , improved hybrid DSTATCOM topology, interactive DSTATCOM operating in CCM (current control mode) and VCM (voltage control mode) . The last few decades have seen a major surge in the number of researchers working on power quality issues and they have come up with numerous advanced control techniques for the harmonics suppression, PFC, ZVR, load balancing problems and many other power quality issues

In this paper, a combined LMS-LMF (Least Mean Square-Least Mean Fourth) based control algorithm of DSTATCOM is proposed for the power quality improvement in the proposed system. The error of the algorithm is minimized by the appropriately selecting either LMS or LMF for the pulse generation, thus the algorithm helps in extracting accurate pulses for the operation of DSTATCOM. Depending on the value of error signal obtained in any of the phases either of LMS or LMF based control algorithm is used to minimize the error thereby taking the advantage of both algorithms . The step size is selected on the basis of power rating of the system. The combined LMS-LMF control algorithm has better performance as compared with LMF and LMS control algorithm based on steady state performance and mean square error. The proposed control algorithm has fast convergence speed when compared with LMS and LMF control algorithms. This control algorithm is designed for harmonics elimination, ZVR, PFC and load balancing of nonlinear loads. This algorithm is robust for application, easy to implement and the response is fast.

II. PROPOSED SYSTEM CONFIGURATION

The power quality in the distribution system can be improved by using the proposed configuration as shown in Fig.1. This system includes a three phase nonlinear load which is supplied from a 415 V, 50 Hz, 3-phase AC supply with supply resistance (*Rs*) and supply inductance (*Ls*), VSC with a DC bus capacitor (*Cdc*) and ripple filters (*Rf*, *Cf*) to eliminate the high switching frequency noise during the operation of VSC. The VSC is linked to the Point of Common Coupling (PCC) through the interfacing inductors (*Li*) which are tuned such that they reduce the ripples in the compensating currents. A 3-phase diode bridge rectifier (DBR) is used as a nonlinear load with a RL branch on the DC side. For the simulation

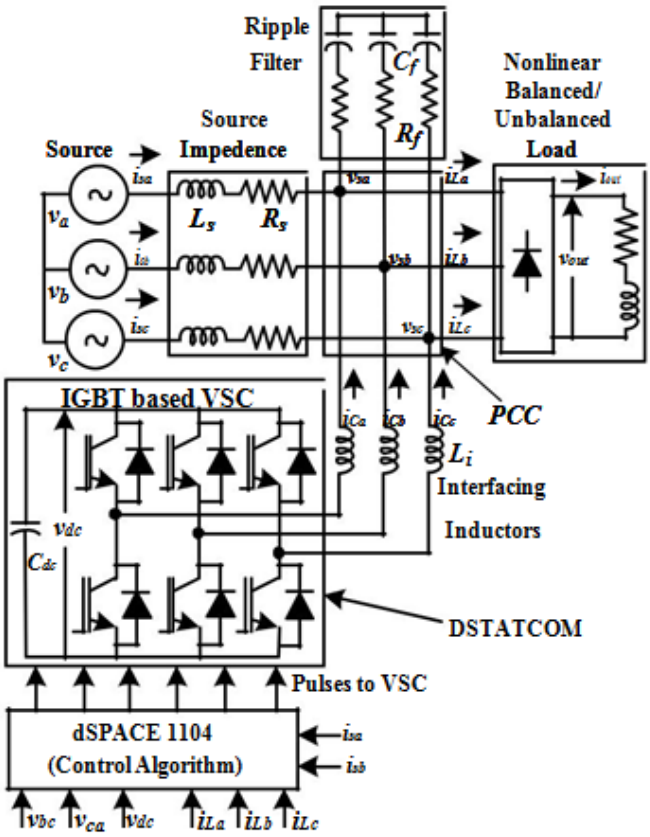

Fig.1 Schematic diagram of distribution system with DSTATCOM

using MATLAB software, the passive elements such as ripple filters (*Rf* and *Lf*) and interfacing inductors (*Li*) are designed considering the specifications of three phase PCC voltage at 415 V and the load to operate at 20 kW power rating [33]. The corresponding values required for simulation are as specified in Appendix A. Similarly the design for the hardware implementation with a three phase PCC voltage of 105 V and load operating at 1.1 kW power rating are realized and the corresponding values are as specified in Appendix B.

III. CONTROL ALGORITHM

The schematic of the combined LMS-LMF based control algorithm of DSTATCOM is shown in Fig. 2. This combined LMS-LMF based algorithm is used to derive the required reference supply currents from the observed load currents (*iLa, iLb, iLc*), unit templates (*uaa, uab, uac*) derived from the sensed supply voltages (*vsa, vsb* and *vsc*), the DC link voltage across the compensator (*vdc*), and the magnitude of supply voltages (*Vt*). The reference supply currents which are generated from the algorithm are correlated with the supply currents sensed from the system and the resulting error difference is used to generate the appropriate pulses for the DSTATCOM by passing these error signals through hysteresis based current controller.

Initially one derives the active unit template components (*uaa, uab, uac*) for the three phases which are in-phase to the supply voltages (*vsa, vsb* and *vsc*) are expressed as [2],

$$u_{aa} = \frac{v_{sa}}{V_t}\ ; u_{ab} = \frac{v_{sb}}{V_t}\ ;\ u_{ac} = \frac{v_{sc}}{V_t} \qquad (1)$$

where *Vt* is the amplitude of sensed supply voltages (*vsa, vsb* and *vsc*) or PCC voltage and is expressed as [2],

$$V_t = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)} \qquad (2)$$

These unit templates are used to synchronize the obtained active weights (*waa, wab, wac*) with the phase of supply voltage to obtain the appropriate errors (*eaa, eab* and *eac*).

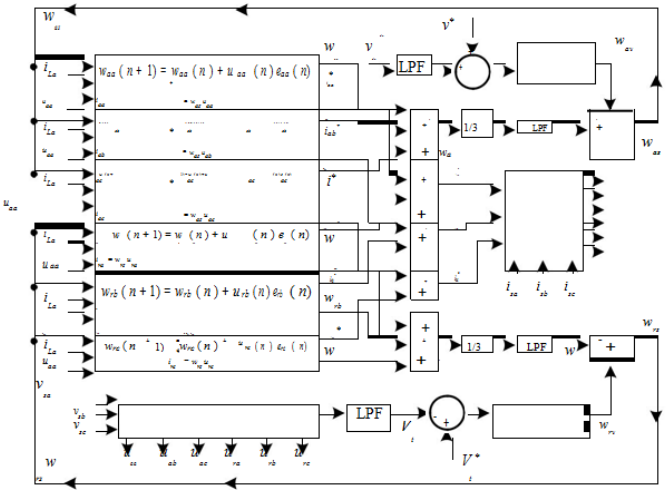

Fig. 2 Block diagram of combined LMS-LMF based control algorithm

The active weight component of the phase 'a' at sampling instant $(n+1)^{th}$ is estimated as,

$$w_{aa}(n+1) = w_{aa}(n) + u_{aa}(n)e_{aa}(n) \qquad (3)$$

where, $e_{aa}(n)$ is the actual active error vector of phase 'a' for the proposed combined LMS-LMF [31-32] based control algorithm and this error component is expressed as,

$$e_{aa}(n) = er_{aa}(n) \text{ if } er_{aa}(n) \geq 1$$
$$= er^3_{aa}(n) \text{ if } er_{aa}(n) < 1 \qquad (4)$$

where $er_{aa}(n)$ is the error in active load component of phase 'a', at sampling instant $(n)^{th}$ and is estimated as,

$$er_{aa}(n) = k\{i_{La}(n) - u_{aa}(n)w_{aa}(n)\} \qquad (5)$$

The factor used in the formation of these equations is k which is a step size and the suitable value for this applications is 0.1.

Similarly, the active weight component for phase 'b' and 'c' are expressed as,

$$w_{ab}(n+1) = w_{ab}(n) + u_{ab}(n)e_{ab}(n) \qquad (6)$$

$$w_{ac}(n+1) = w_{ac}(n) + u_{ac}(n)e_{ac}(n) \qquad (7)$$

By adding (3), (6) and (7), the mean value of the fundamental active weight components is obtained as,

$$w_a = (w_{aa} + w_{ab} + w_{ac})/3 \qquad (8)$$

The set DC voltage reference value is correlated with sensed DC link voltage (v_{dc}) of VSC and the error is given to the PI controller of DC bus voltage. The output of this controller is taken to be the DC loss weight component and is expressed as,

$$w_{av}(n+1) = w_{av}(n) + K_{pd}\{v_{dd}(n+1) - v_{dd}(n)\} + K_{id}\, v_{dd}(n+1) \qquad (9)$$

where, $w_{av}(n+1)$, $v_{dd}(n+1)$ are the DC bus loss component and error between of sensed DC link voltage of VSC and reference DC value at $(n+1)^{th}$ sampling time. K_{id} and K_{pd} are the integral and proportional gains of the DC bus voltage controller.

By adding the DC loss component to the average fundamental active weight component, one gets the total active weight component (w_{at}) of the supply reference currents as,

$$w_{at} = w_a + w_{av} \qquad (10)$$

The active in-phase reference supply current components for the three phases are expressed as,

$$i^*_{sa} = w_{at}u_{aa}\ ;\ i^*_{sb} = w_{at}u_{ab}\ ;\ i^*_{sc} = w_{at}u_{ac} \qquad (11)$$

The reactive unit template components (u_{ra}, u_{rb}, u_{rc}) for the three phases which are quadrature to the supply voltages (v_{sa}, v_{sb} and v_{sc}) are expressed as [2],

$$u_{ra} = -\frac{u_{sa}}{\sqrt{3}} \cdot \frac{u_{ac}}{\sqrt{3}}\ ;\ u_{rb} = \frac{\sqrt{3}u_{aa}}{2} + \frac{(u_{ab} - u_{ac})}{2\sqrt{3}}\ ;$$
$$u_{rc} = -\frac{\sqrt{3}u_{aa}}{2} + \frac{(u_{ab} - u_{ac})}{2\sqrt{3}} \qquad (12)$$

The reactive weight components for three phases a, b and c are estimated by using the following equations,

$$w_{ra}(n+1) = w_{ra}(n) + u_{ra}(n)e_{ra}(n) \qquad (13)$$

$$w_{rb}(n+1) = w_{rb}(n) + u_{rb}(n)e_{rb}(n) \qquad (14)$$

$$w_{rc}(n+1) = w_{rc}(n) + u_{rc}(n)e_{rc}(n) \qquad (15)$$

By adding (13), (14) and (15), the mean value of the fundamental reactive weight components is obtained as,

$$w_r = (w_{ra} + w_{rb} + w_{rc})/3 \qquad (16)$$

The average magnitude of the supply voltage is sensed and is correlated with set reference magnitude value and the error difference is given to the AC voltage PI (Proportional Integral) controller. The AC voltage controller output is weighted to be the AC loss weight component and is expressed as,

$$w_{rv}(n+1) = w_{rv}(n) + K_{pt}\{v_{dt}(n+1) - v_{dt}(n)\} + K_{it}\, v_{dt}(n+1) \qquad (17)$$

where $w_{rv}(n+1)$, $v_{dt}(n+1)$ are the reactive power component

and error between sensed AC link voltage and reference magnitude value at $(n+1)^{th}$ sampling time. K_{iv} and K_{pv} are the integral and proportional gains of AC voltage controller.

By subtracting the average fundamental reactive weight component from the reactive power component, one gets the total reactive weight component (w_{rs}) of the supply reference currents and it is estimated as,

$$w_{rs} = w_{rs} - w_r \quad (18)$$

The reference reactive supply current components which are in quadrature with the three phase voltages are expressed as,

$$i^* = w\,u \quad ; i^* = w\,u \quad ; i^* = w\,u \quad (19)$$

Finally adding the active and reactive reference components of the supply currents of each of the three phases, reference supply currents are expressed as,

$$i^* = i^* + i^* \; ; i^* = i^* + i^* \; ; i^* = i^* + i^* \quad (20)$$

These reference supply currents (i_{sa}^*, i_{sb}^*, i_{sc}^*) and sensed supply currents (i_{sa}, i_{sb}, i_{sc}) are given to hysteresis current controller which generates the gating pulses to VSC.

IV. SIMULATION RESULTS AND DISCUSSION

The simulation model of distribution system with DSTATCOM using the combined LMS-LMF based control algorithm is developed by using MATLAB software. The model is run in both PFC and ZVR modes under nonlinear load. The steady state and dynamic performances for the proposed combined LMS-LMF based control algorithm are studied in detail. The design parameters for the proposed system are as specified in Appendix A.

A. Characteristics of Intermediate Signals for Combined LMS-LMF Based Algorithm of DSTATCOM

The characteristics of intermediate signals for the combined LMS-LMF based DSTATCOM under nonlinear load are shown in Fig. 3. In this figure, waveforms of PCC voltages (*vpcc*), phase 'a' current of supply (*isa*), phase 'a' current of load (*iLa*), average value of the active weight component in-phase to supply voltages (*wa*), total active weight component (*was*), average value of reactive weight components in-quadrature to supply voltages (*wr*), total reactive weight component (*wrs*), supply currents (*is*) and reference supply currents (*is**) are shown. These waveforms from 0.52 s to 0.54 s are during unbalanced load by switching off the phase 'a' of load. At 0.54 s, the phase 'a' of load is reconnected. Since the overall load is reduced between 0.52 s and 0.54 s, the value of weights is less but as the load is reconnected at 0.54 s, the weights built back to their higher value while the actual and reference supply currents are sinusoidal and balanced.

B. Dynamic Response of System in PFC Mode

The dynamic response of the system in the PFC mode for a varying nonlinear load is shown in Fig. 4. In this figure, waveforms of PCC voltages (*vpcc*), supply currents (*is*), load currents (*iLa*, *iLb*, and *iLc*), compensator currents (*ica*, *icb* and *icc*) and DC voltage across the VSC (*vdc*) are shown. One may see that when the phase 'a' load is cut off, the supply currents are sinusoidal and balanced. Moreover, the DC link voltage is regulated at 700 V during load unbalanced condition.

The harmonic FFT (Fast Fourier Transform) analysis of phase 'a' PCC voltage (*vsa*), phase 'a' current of supply (*isa*) and phase 'a' current of load (*iLa*) in PFC mode at nonlinear load is shown in Fig. 5 and their total harmonic distortions (THDs) are 2.01 %, 2.48 % and 25.06 % respectively. It is

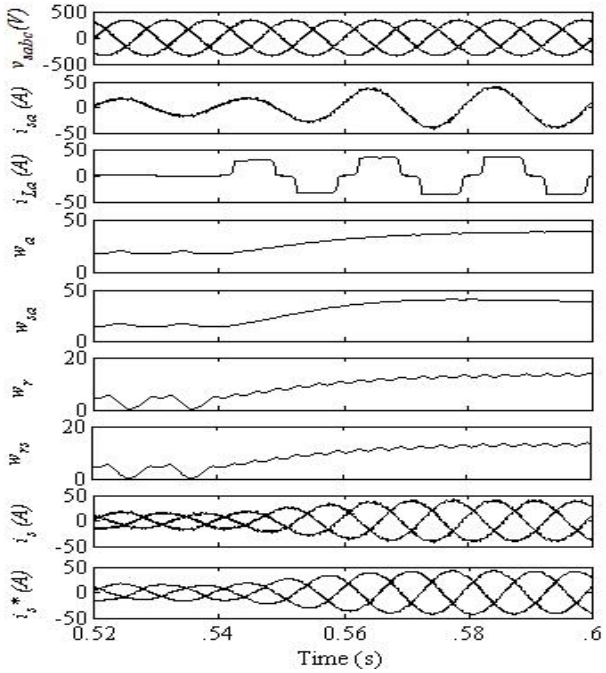

Fig. 3 Characteristics of intermediate signals using combined LMS-LMF based control algorithm

observed that the PCC voltage and supply current THDs are well below the limit as specified in IEEE-519 standard [34] compared to the load current THD of 25.06 %.

C. Dynamic Response of System in ZVR Mode

The dynamic response of the system in the ZVR mode for a varying load is shown in Fig.6. In the figure, waveforms of PCC voltages (*vpcc*), supply currents (*is*), load currents (*iLa*, *iLb*, and *iLc*), compensator currents (*ica*, *icb* and *icc*), DC voltage across the VSC (*vdc*) and voltage amplitude at PCC (*Vt*) are shown. One may see that when the phase 'a' load is cut off, the supply currents are sinusoidal and balanced. Moreover, the DC link voltage is regulated at 700 V and the AC PI controller regulates the PCC voltage amplitude at a

nominal value of 338.8 V even during load unbalanced condition.

V. HARDWARE RESULTS AND DISCUSSION

The response of the proposed system with combined LMS-LMF based algorithm is implemented on the DSTATCOM prototype developed in the laboratory as shown in Fig. 7. The prototype is fed from a 3-phase supply with a DBR nonlinear load and uses a three-leg VSC linked at PCC along with the Hall effect voltage and current sensors. The voltages and currents are sensed and used in the algorithm through the real time controller (dSPACE 1104) via digital to analog converter (DAC) channels. Test results, both steady-state and dynamic conditions are recorded with the help of PQ analyzer (Fluke 43B) and digital signal oscilloscope (Agilent DSO6014A).

A. Response of Power Quality Improvement

Fig. 8 shows the steady-state response waveforms under nonlinear load. Fig. 8 (a) shows the waveforms of PCC voltage (*vbc*) and supply current of phase 'a' (*isa*); while Fig. 8 (b)shows the power at the supply side (*Ps*) and Fig. 8 (c) shows the THD of the supply current (*isa*) which is 4.1% and is in accordance to IEEE-519 standard [34]. Fig. 8 (d) shows the waveforms of PCC voltage (*vbc*) and load current of phase 'a'(*iLa*); while Fig. 8 (e) shows the power at the load side (*PL*) and Fig. 8 (f) shows the THD of the load current (*iLa*) which is 24.7%. Fig. 8 (g) shows the PCC voltage (*vbc*) and compensator current of phase 'a'(*ica*) while Fig. 8 (h) shows the compensator power (*Pcomp*) and Fig. 8 (i) shows the THD

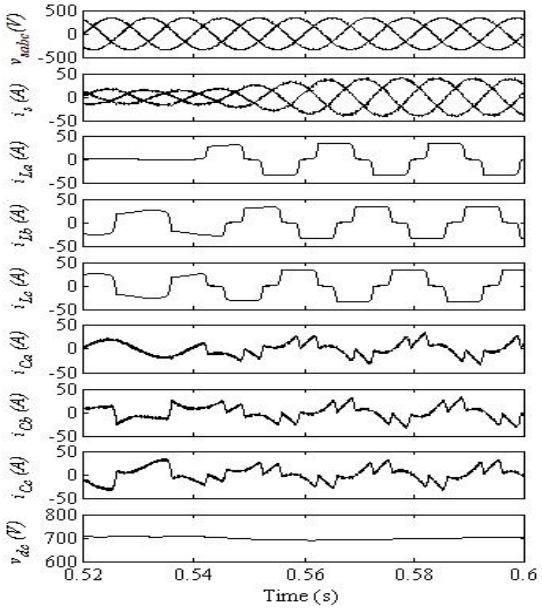

Fig. 4 Dynamic response of the system in PFC mode of the PCC voltage (*vsa*) which is 3.1% and is in accordance to IEEE standard .

B. Steady-State Response of System under Nonlinear Loads

The steady state response of the system is shown in Figs. 9 (a)-(d) with the PCC voltage (*vbc*) along with the three phase supply, load and compensator currents. Fig. 9 (a)

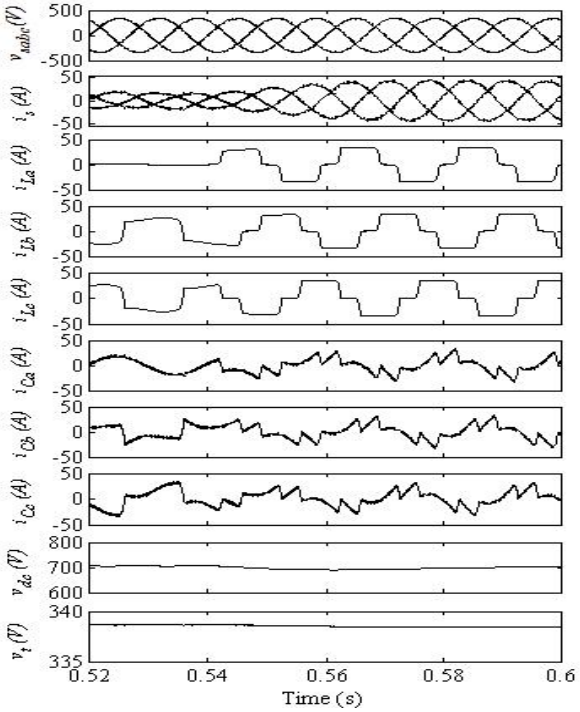

Fig. 6 Dynamic response of the system in ZVR mode

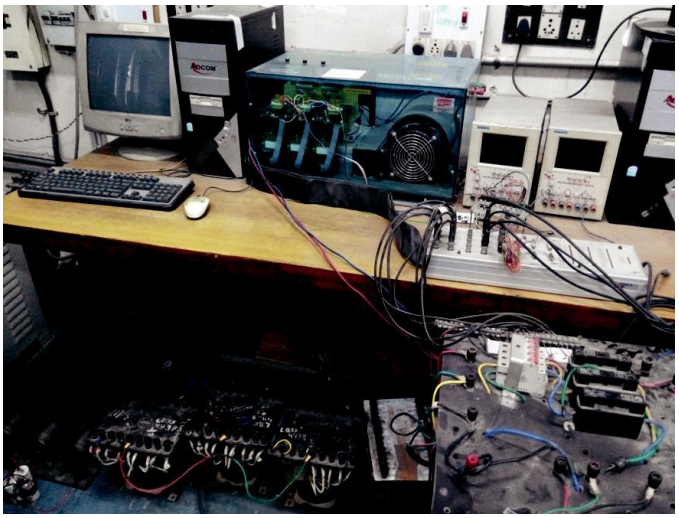

Fig. 7 Hardware prototype of proposed DSTATCOM system

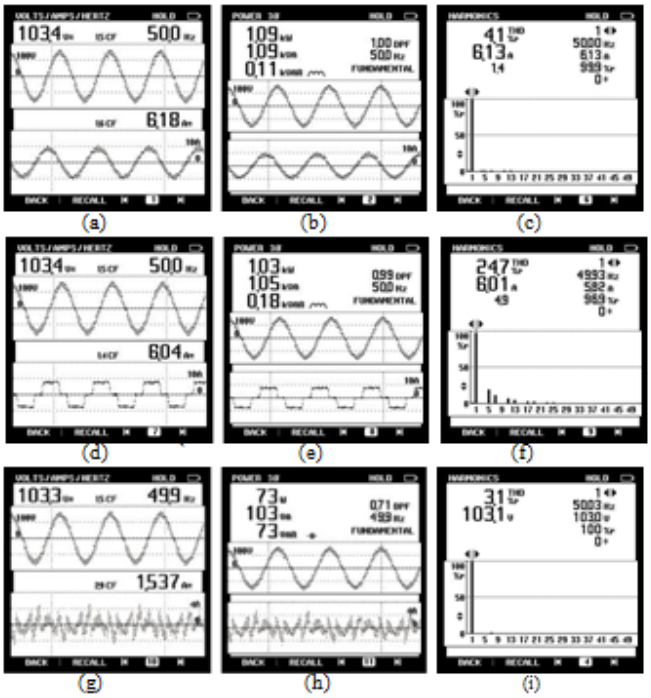

Fig. 8 Steady-state responses of the system (a) v_{bc} and i_{sa} (b) P_s (c) harmonic FFT analysis of i_{sa} (d) v_{bc} and i_{La} (e) P_L (f) harmonic FFT analysis of i_{La} (g) v_{bc} and i_{ca} (h) P_{comp} (i) harmonic FFT analysis of v_{sa}

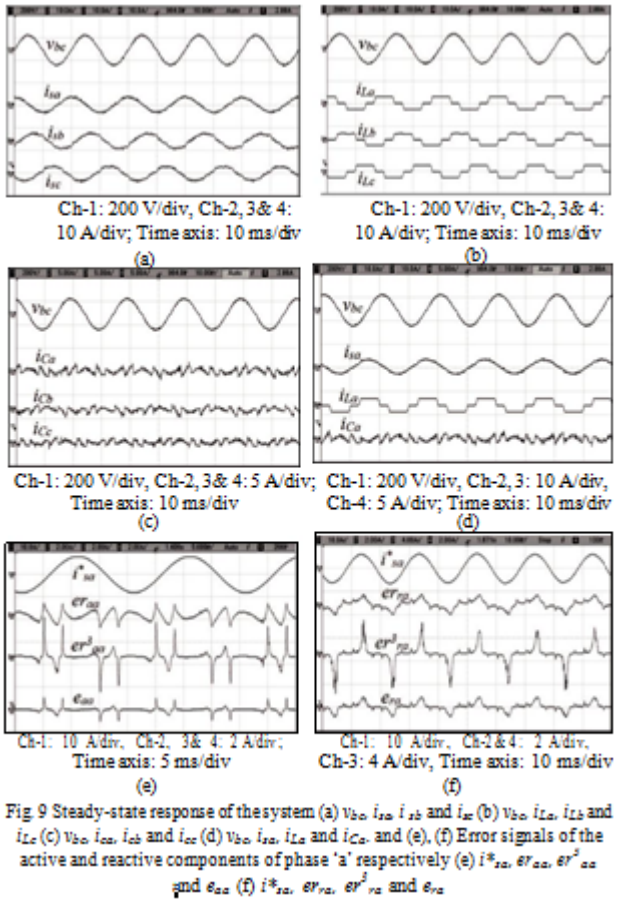

Fig. 9 Steady-state response of the system (a) v_{bc}, i_{sa}, i_{sb} and i_{sc} (b) v_{bc}, i_{La}, i_{Lb} and i_{Lc} (c) v_{bc}, i_{ca}, i_{cb} and i_{cc} (d) v_{bc}, i_{sa}, i_{La} and i_{Ca}, and (e), (f) Error signals of the active and reactive components of phase 'a' respectively (e) i^*_{sa}, er_{aa}, er^3_{aa} and e_{aa} (f) i^*_{sa}, er_{ra}, er^3_{ra} and e_{ra}

shows the PCC voltage (*vbc*) and three phase supply currents (*isa*, *isb* and *isc*). Fig. 9 (b) shows the PCC voltage (*vbc*) and three phase load currents (*iLa*, *iLb* and *iLc*). Fig. 9 (c) shows the PCC voltage (*vbc*) and three phase compensator currents (*iCa*, *iCb* and *iCc*) and Fig. 9 (d) shows the PCC voltage (*vbc*), supply current phase 'a' (*isa*), load current (*iLa*), compensator current (*iCa*) of phase 'a'.

C. Error Signals of Active and Reactive Components

The steady-state response of error signals along with the reference currents for active and reactive components of phase 'a' is shown in Figs. 9 (e)- (f). Fig. 9 (e) shows the reference supply current of phase 'a' (i^*sa), active error output of LMS algorithm of phase 'a' (*eraa*), active error output of LMF algorithm of phase 'a' (er^3aa) and active error output of the combined LMS-LMF based control algorithm of phase 'a' (*eaa*) while Fig. 9 (f) shows the reference supply current of phase 'a' (i^*sa), reactive error output of LMS algorithm of phase 'a' (*erra*), reactive error cube output of LMF algorithm of phase 'a' (er^3ra) and reactive error output of combined LMS-LMF based control algorithm of phase 'a' (*era*). One sees that the combined LMS-LMF waveform resembles the minimum of both the waveforms of LMS and LMF. This reduces the error thus driving the algorithm to generate accurate pulses compared to any of LMS or LMF algorithms.

D. Dynamic Response of DSTATCOM under Nonlinear Loads

The dynamic response of the system is shown in Figs. 10 (a)-(b). The responses are observed when the phase 'a' of load is switched ON. Fig. 10 (a) shows the PCC voltage (*vbc*), supply current (*isa*), load current (*iLa*), compensator current (*iCa*) of phase 'a'. These waveforms show that initially the phase 'a' of load is switched off; so the load current (*iLa*) is zero but the compensator current (*ica*) is maintaining the supply current (*isa*) to be sinusoidal in phase a. Here one may see that the magnitude of supply current reduces since the overall load has reduced which denotes the load balancing. Moreover, the PCC voltage (*vbc*) waveform is well regulated even in case of an unbalance from the load side. Fig. 10 (b) shows the DC link voltage across VSC (*vdc*), supply current of phase 'a' (*isa*), load current (*iLa*), compensator current (*iCa*) of phase 'a'. Here one may see that the even under unbalance in phase 'a' load, the DC link voltage is well regulated at 200 V DC and the supply current is sinusoidal.

E. Dynamic Response of Internal Signals of Proposed Algorithm

The dynamic response of internal signals namely average value of the active weight components in-phase to the PCC voltages (*wa*), DC link PI controller weight output (*wav*), total active weight component (*was*) along with the reference supply current of phase 'a'(i^*sa) are shown in Fig. 10 (c). Similarly, the dynamic response of the internal signals namely average value of the reactive weight components in-phase to the PCC voltages (*wr*), weight output of the PCC voltage controller (*wrv*), total reactive weight component (*wrs*) along with the reference supply current of phase 'a'(i^*sa) are shown in Fig. 10 (d). One can see that initially there is a load removal situation but when the phase 'a' load is put back, balancing the load, the weights built up while the reference supply currents are sinusoidal.

VI. CONCLUSION

The proposed combined LMS-LMF based control algorithm of DSTATCOM has been implemented and simulated for both ZVR and PFC modes under nonlinear balanced and unbalanced loads. Moreover, this algorithm has also been verified on the hardware prototype of the DSTATCOM developed in the laboratory. The proposed algorithm has been used for obtaining the reference supply currents from the active and reactive weight components with distortions of the PCC voltages and supply currents well below 5% which is well within the specified standard. The load balancing has also been achieved keeping the waveforms of PCC voltages and currents as sinusoidal and in phase.

VII. APPENDICES

APPENDIX-A

AC mains: 3 phase, 415 V at 50 Hz; Ripple Filter: *Rf* = 5 Ω and *Cf* = 10 µF; Diode-bridge rectifier based nonlinear load

with *Rout* = 15.6 Ω and *L out* =200 mH; Rating of VSC = 20 kVA; *Cdc* = 6800 µF; *vdc*= 700 V; *Li* = 3.1 mH; step size (*k*) = 0.1; DC PI controller gain value: *Kpd* = 0.8 and *Kid* = 0.5; AC PI controller gain value: *Kpt* = 1.2 and *Kit* = 0.5.

APPENDIX-B

AC mains: 3 phase, 103.4 V at 50Hz; Ripple Filter: *Rf* = 5 Ω and *Cf* = 10 µF; Diode-bridge rectifier based nonlinear load with *Rout*= 21.5 Ω and *Lout*=130 mH; Rating of VSC = 5 kVA; *Cdc*= 3100 µF; *vdc* = 200 V; Interfacing Inductors (*Li*) = 2.4 mH; step size (*k*) = 0.2; DC PI controller gain value: *Kpd* = 0.6 and *Kid* = 0.15.

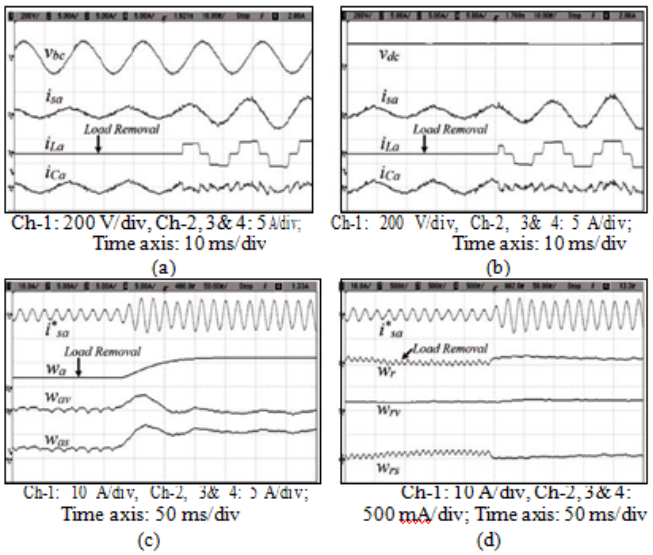

Fig.10 Dynamic response of the system (a) v_{bc}, i_{sa}, i_{La} and i_{ca} (b) v_{dc}, i_{sa}, i_{La} and i_{ca}. and (c),(d) Internal signals of active and reactive weight components respectively (c) i^*_{sa}, w_a, w_{av} and w_{as} (d) i^*_{sa}, w_r, w_{rv} and w_{rs}.

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