Design Of Three Level Integrated Ac-Dc Converter With Pulse Width Modulation

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Abstract- *In a new integrated three-level ac–dc converteris presented. The proposed converter integrates the operation of the boost power factor correction and the three-level dc–dc converter. The converter is made to operate with two independent controllers—an input controller that performs power factor correctionand regulates the dc bus and an output controller that regulates the output voltage. The input controller prevents the dc-bus voltage from becoming excessive while still allowing a single-stage converter topology to be used. The project explains the operation of the new converter in detail and discusses its features and a procedure for its proper design. Experimental results obtained from a prototype are presented to confirm the feasibility of the new converter.*

I. INTRODUCTION

Higher power ac–dc converters are required to have some kind of power element rectification (PFC) ability to consent to symphonious principles, for example, IEC61000-3-2. PFC techniques can for the most part be isolated into the accompanying three classifications:

1) Passive PFC converters: They utilize aloof components, for example, inductors and capacitors to channel low recurrence information current sounds and make the data current more sinusoidal. In spite of the fact that these converters are straightforward and reasonable, they are additionally overwhelming and massive and are accordingly utilized as a part of a predetermined number of uses.

2) Two-stage converters: They comprise of an ac–dc help pre controller converter that shapes the data current and a secluded dc–dc full-connect converter that changes over the pre controller yield into the required dc voltage. Two-stage converters, be that as it may, require two separate switch-mode converters (each with its own controller), and along these lines, can be costly. In addition, they have poor effectiveness when working under light-stack conditions as there are two converter stages that are working—each with its own particular arrangement of settled misfortunes—while a little measure of influence is really exchanged to the heap. These settled misfortunes are predominant under light-stack working conditions.

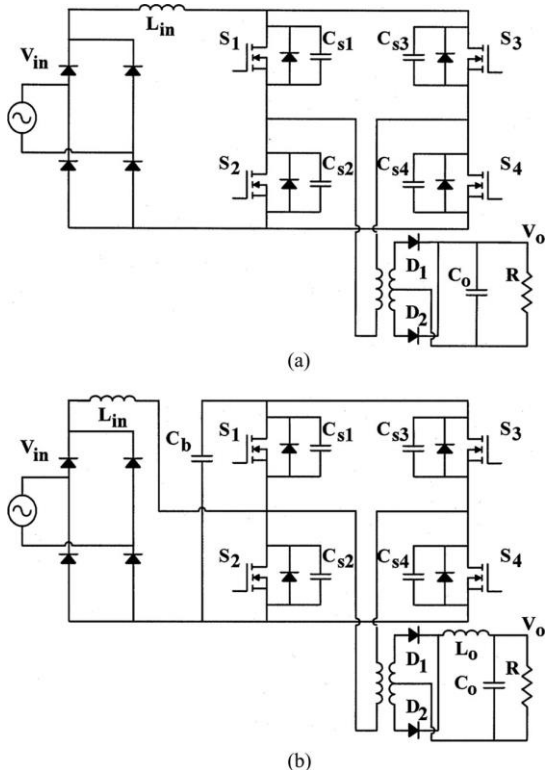


Fig.. Various single-stage power factor correction converters.
(a) Boostbased
current-fed ac–dc PWM integrated full-bridge converter [3].
(b) SSPFC
PWM full-bridge converter

II. PULSE WIDTH MODULATION

The proposed converter is made to work with the PWM procedure. PWM signs are heartbeat trains which are connected to the door of changes to perform the operation of converter. The beat trains are altered recurrence and size and variable heartbeat width. There is one beat of altered greatness in each PWM period. Be that as it may, the width of the beats changes from period to period as indicated by a tweaking signal. At the point when a PWM sign is connected to the entryway of a powertransistor, it causes the turn on and kills interims of the transistor to change starting with one PWM

period then onto the next PWM period as indicated by the same regulating signal& thus working of converter begins. The recurrence of a PWM signal must be much higher than that of the adjusting signal, the crucial recurrence, such that the vitality conveyed to the heap depends for the most part on the tweaking signal. The control of yield voltage is done utilizing beat width tweak.

III. AC–DC RECTIFIER

The circuit diagram of the full-bridge, three-phase, AC–DC rectifier is shown in next page. The power switch generally used in the rectifier is the SCR. The average DC output voltage is given by:

$$Vdc = \frac{3\sqrt{2}}{\pi} V_L \cos\alpha \quad \text{.....(1)}$$

Where

V_L = line-to-line voltage on the three-phase AC side of the rectifier

α = angle of firing delay in the switching

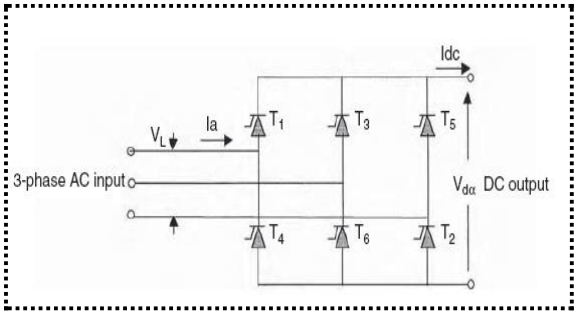


Fig: Three-phase, full-bridge, AC–DC controlled rectifier circuit

The delay angle is measured from the zero intersection in the positive portion of the AC voltage wave. Mathematical statement 11.1 demonstrates that the yield DC voltage can be controlled by changing the postponement point α, which thusly controls the conduction (on-time) of the switch. Superimposed on the DC voltage at the rectifier yield are high-recurrence AC harmonics (swells). A consonant channel is, in this manner, expected to diminish the AC segment of the yield voltage and expansion the DC segment. A L–C channel does this with an inductor associated in arrangement and a capacitor in parallel with the redressed yield voltage.The load determines the DC-side current as:

$$I_{dc} = \frac{\text{DC load Power}}{Vdc} \quad \text{.....(2)}$$

In steady-state operation, the balance of power must be maintained on both AC and DC sides. That is, the power on the AC side must be equal to the sum of the DC load power and the losses in the rectifier circuit. The AC-side power is therefore:

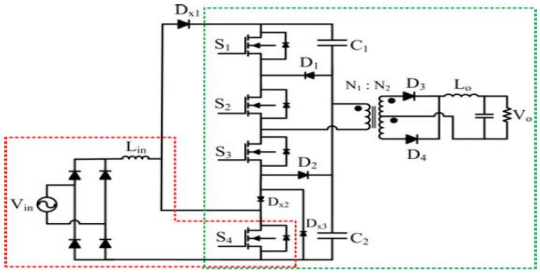
$$Idc = \frac{\text{DC load Power}}{\text{Rectifier Efficiency}} \quad \text{.....(3)}$$

the three-phase AC power is given by:

$$P_{AC} = \sqrt{3} V_L I_L \cos\emptyset \quad \text{..... (4)}$$

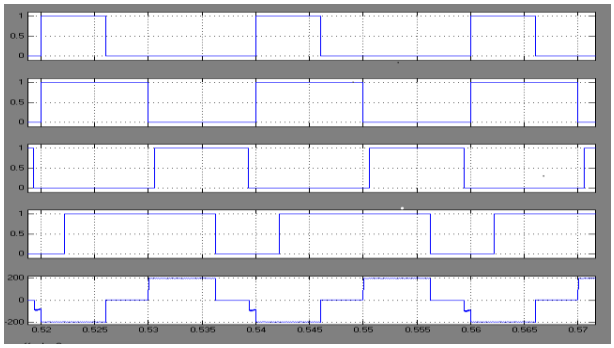
where $\cos^{\emptyset}$ is the power factor on the AC side. With a well-designed power electronic converter, the power factor on the AC side is approximately equal to that of the load.

IV. PROPOSED SYSTEM



The proposed converter, which is appeared in above figure, coordinates an ac–dc help PFC converter into a three-level dc–dc converter. The ac–dc help segment comprises of an info diode span, support inductor Lin , help diode Dx1 , and switch S4 , which is shared by the multilevel dc–dc segment. At the point when S4 is off, it implies that no more vitality can be caught by the help inductor. For this situation, diode Dx2 keeps info current from streaming to the midpoint of capacitors C1 and C2 and diode Dx1 directs and exchanges the vitality put away in the support inductor Lin to the dc transport capacitor. Diode Dx3 sidesteps Dx2 and makes a way to circulate current. In spite of the fact that there is just a solitary converter, it is worked with two free controllers. One controller is utilized to perform PFC and direct the voltage over the essential side dc-transport capacitors by sending proper gating signs to S4 . The other controller is utilized to manage the yield voltage by sending fitting gating signs to S1 to S4 . It ought to be noticed that the control of the info area is decoupled from the control of the dc–dc segment and in this way can be outlined independently. The gating sign of S1 , notwithstanding, is subject to that of S4 , which is the yield of the info controller; how this sign is produced is talked about in point of interest later in this project. The gating signals for S2

and S3 are simpler to create as both switches are each ON for a large portion of an exchanging cycle, yet are never ON in the meantime. Commonplace converter waveforms are appeared in Fig. 3, and proportional circuit outlines that demonstrate the converter's methods of operation are appeared in Fig. 4 with the diode rectifier span yield supplanted by an amended sinusoidal source. As the data line recurrence is much lower than the exchanging recurrence, it is expected that the supply voltage is consistent inside of an exchanging cycle. It is additionally expected that the info current is spasmodic, despite the fact that there is no motivation behind why the data current can't be made to be ceaseless if this is what is fancied.



V. CONCLUSION

Another multilevel single-stage ac–dc converter is proposed in the project. This converter is worked with two controllers one controller that performs data PFC and a second controller that manages the yield voltage. The remarkable element of this converter is that it joins the execution of two-stage converters with the diminishment of expense of single-stage converters. The project presents the proposed converter, clarifies its fundamental working standards and methods of operation, and talks about its outline as for various dc-transport voltages. Exploratory results that affirm the achievability of the converter are likewise displayed in the project.

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