A Capacitor Less Ldo Regulator Using Push–Pull Amplifiying Regulator Power Transistor With A Sub-1 V Transient An Enhanced Output

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Abstract- *An output-capacitor much less low-dropout (OCL-LDO) regulator with a push–pull composite power transistor is provided on this paper. Using the proposed composite transistor, the non dominant parasitic poles may be pushed to better frequencies, main to good balance. In addition, the slew price drawback on the gate of the energy transistor is advanced significantly by using the proposed push–pull structure. Implemented and fabricated in UMC 65-nm CMOS technology, the LDO regulator occupies best an lively place of 0.0096 mm2. The experimental results have shown that the regulator is capable of perform at VIN = 0.Seventy five V and supply a most load contemporary of 50 mA with a dropout voltage of less than 250 mV. It consumes a quiescent current of 16.2 μA and is able to settle within 1.2 μs.*

Keywords- HSPICE Synopsis Tool, Composite electricity transistor, low-dropout (LDO)Voltage regulator, low-voltage regulator. Output-capacitor less (OCL) LDO regulator, push–pull.

I. INTRODUCTION

LOW-DROPOUT (LDO) regulator is an important building block in modern VLSI circuit designs. Compared with switching type of regulators, LDO regulator is often employed to provide a regulated and stable supply voltage to those noise sensitive analog/RF blocks, especially under on-chip applications environment. Conventional LDO regulator requires a large off-chip capacitor in the scope of μF to guarantee security. Hence, yield capacitor less LDO controller (OCL-LDO) is favored for on-chip applications. Low-control utilization is a standout amongst the most discriminating parameters, particularly for versatile electronic gadgets. To lessen the force utilization, the working supply voltage must be lessened while tending to tranquil mindful outline. It is on account of this is one of the most effective ways to prolong the battery life of a portable device. Therefore, it possesses a demand of an ultralow voltage LDO regulator which can provide a 0.5 V supply line to those integrated circuits. Ultralow voltage design imposes several challenges for LDO regulators in terms of stability, headroom, and slew-rate problems.

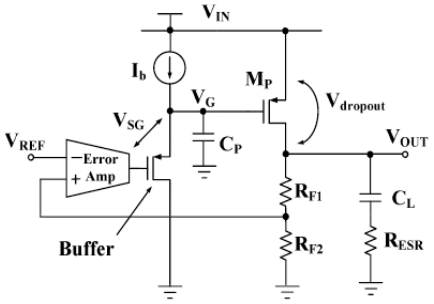


Fig: Structure of the buffer based LDO regulator

As shown in Fig. 1, the buffer based LDO regulators require an additional *V*SG to ensure the operation. Under sub-1 V environment, the buffer based LDO regulator is difficult to fulfill the headroom budget. In addition, the parasitic capacitor *CP* associated at the gate of power transistor *MP* is greatly affected by the input supply *V*IN and the dropout voltage *V* dropout*(*max*)* = *(V*IN–*V*OUT*)* of regulator design. Consider a PMOS power transistor operates in saturation region, the required aspect ratio is given as

$$\frac{W}{L} = \frac{2I_{LOAD(\max)}}{\mu C_{OX} V_{dropout}\left(V_{IN} - V_G - V_{THP} - \frac{V_{dropout}}{2}\right)} \quad \text{.....(1)}$$

Where *μ*, *C*ox, and VTHP are the mobility, gate capacitance per unit, and threshold voltage of power transistor, respectively. *VG* is defined as the power transistor's driver output voltage. *I*LOAD*(*max*)* is the maximum load current. To save silicon area the power transistor working in linear region can be adopted but at the expense of loop gain of the LDO regulator as the design tradeoff. The required aspect ratio becomes

$$\frac{W}{L} = \frac{I_{LOAD(\max)}}{\mu C_{OX} V_{dropout}\left(V_{IN} - V_G - V_{THP} - \frac{V_{dropout}}{2}\right)}$$

……..(2)

As can be observed in (1) and (2), the size of power transistor depends on multiple parameters. They are operating region, *I*LOAD *(*max*), V* dropout, and *V*IN. In either approach, when both low voltage and/or low dropout are required, the size of the power transistor needs to be increased to compensate the reduction in the headroom, thus leading to the increase of *CP*. As a result, the parasitic capacitances increase significantly, causing the stability, and slew-rate problems.

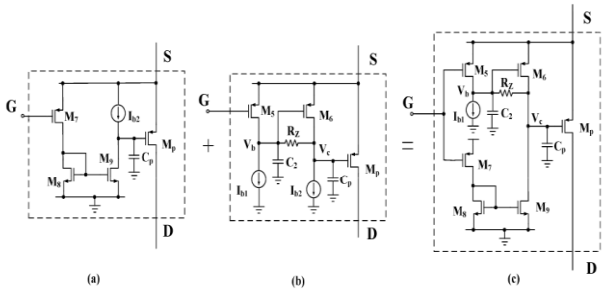


Fig.: (a) Conventional non inverting stage + power transistor. (b) Class-A composite power transistor. (c) Proposed push–pull composite power LDO regulators that can operate at sub-1 V supply voltage have been demonstrated.

The body-bias technique is employed to reduce the threshold voltage *V*TH of the transistors. However nanometer CMOS technology devices, the body-bias threshold reduction for low-voltage operation is not effective due to small value of body factor. In addition, the design only supports a very limited output capacitor value. No output capacitor *CL* is reported. It may have difficulty for use in higher on-chip capacitive load *CL* that lies in the range of few tens of pF. The *Q*-reduction technique is introduced to permit the low-voltage stable LDO operation. Due to the fact that the output nodes of each stage are loaded with the compensation capacitors, the slew-rate of the LDO regulator is greatly affected. Although a LDO regulator with ultralow-quiescent current of 103nA is reported by employing a digital error amplifier (EA), the large voltage dip of 300 mV and setting time of 400μs might not meet the speed requirements in the ultralow-voltage applications.

Demonstrates a gain-enhanced flipped voltage follower-based LDO regulator that consumes only 8μA. However, it draws a minimum *I*LOAD of 3mA to ensure stability for *CL* of 50pF. Hence, it is not suitable for low load current applications. Push–pull technique is demonstrated to improve the slew-rate problem. However, they need the minimum *I*LOAD requirement to maintain stability. n assisted push–pull output stage is proposed to enhance the transient response without requiring any compensation capacitor. However, the transient enhancement circuit is a complicated structure which also requires additional biasing voltage. In addition, it suffers from stability problem when *I*LOAD is less than 100μA. A sub-1 V OCL-LDO regulator with a push–pull composite power transistor is presented. By using the proposed push– pull composite power transistor, without any minimum *I*LOAD requirement, the stability is enhanced because the non dominant parasitic poles can be pushed to higher frequencies. In addition, the slew-rate limitation at the door of the power transistor is enhanced significantly by the proposed push–pull structure without expanding the static biasing current. It allows the utilization of straightforward recurrence pay plan with little pay capacitor.

II. LITERATURE SURVEY

A multiplexer-based concept for reconfigurable multiplier arrays:

this work, a multiplexer-based idea for making a run-time configurable exhibit of multipliers equipped for obliging diverse info information word lengths is exhibited. In our methodology, every component of m 1× m 2 multiplier exhibit is a parallel-parallel multiplier itself, each again embodying various essential math primitive cells and including multiplexers as controllable interconnects. Likewise, we recognize multiplier components for unsigned and marked numbers which vary in calculation and configuration. Assorted architectures are being inspected and an evaluation of equipment unpredictability and zone utilization is given.

Razor: A low-power pipeline based on circuit-level timing speculation:

With expanding clock frequencies and silicon coordination, power mindful processing has turn into a discriminating concern in the configuration of installed processors and frameworks on-chip. One of the more compelling and generally utilized strategies for force mindful processing is dynamic voltage scaling (DVS). To get the greatest force funds from DVS, it is fundamental to scale the supply voltage as low as could reasonably be expected while guaranteeing right operation of the processor. The basic voltage is picked such that under a most dire outcome imaginable of procedure and ecological varieties, the processor dependably works effectively.

On the other hand, this methodology prompts an extremely traditionalist supply voltage since such a most

pessimistic scenario blend of diverse variability's is exceptionally uncommon. In this paper, we propose another way to deal with DVS, called Razor, in view of element recognition and rectification of circuit timing lapses. The key thought of Razor is to tune the supply voltage by checking the lapse rate amid circuit operation, consequently taking out the requirement for voltage edges and abusing the information reliance of circuit deferral. A Razor flip-flop is presented those twofold examples pipeline stage values, once with a quick clock and again with a period obtaining deferred clock. A met soundness tolerant comparator then approves lock qualities tested with the quick clock. In the occasion of timing slip, a changed pipeline recuperation component restores right program state. A model Razor pipeline was outlined in a 0.18 µm innovation and was examined. Razor vitality overhead amid ordinary operation is restricted to 3.1%. Investigations of a full-custom multiplier and a SPICE-level Kogge-Stone viper model uncover that considerable vitality investment funds are feasible for these gadgets (up to 64.2%) with little effect on execution because of lapse recuperation (under 3%).

The N-P-N Composite Transistor:

A p-n-p transistor in the common-collector configuration when driven by a current source behaves very much like an n-p-n transistor in the common-emitter configuration when driven by-a current source. Thus the two transistors shown in Figure 3.3

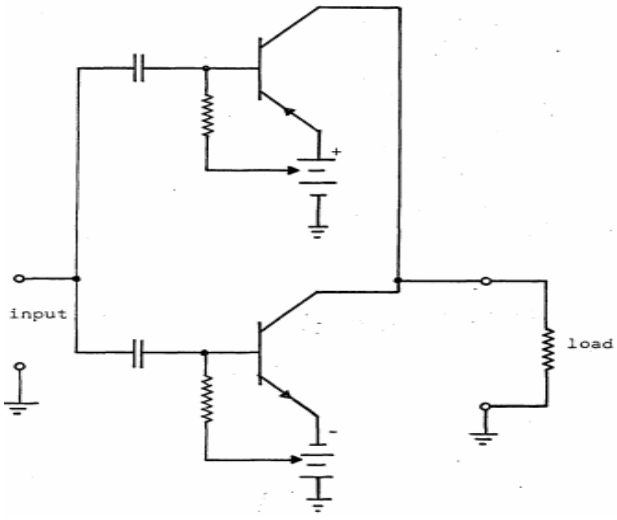


Fig: The basic complementary-symmetry circuit

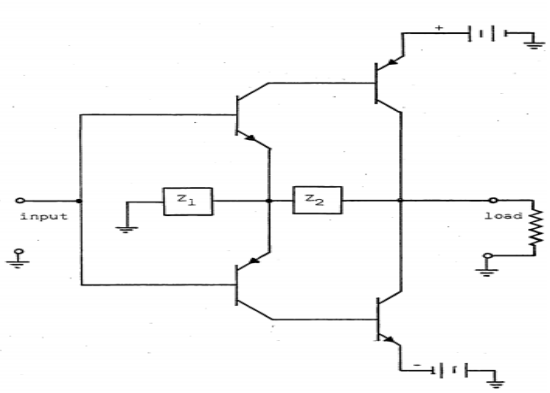


Fig: A modified form of complementary-symmetry circuit

Behave somewhat like a single n-p-n power transistor. This composite transistor has the advantage that the power is largely dissipated by the p-n-p power transistor and a much smaller and readily-available n-p-n unit can be used in the driver stage. It has the disadvantage that the current gain and cutoff frequency are first order functions of the current gains and cutoff frequencies of the individual transistors. Any attempt to match such a composite transistor to an enantiomorphism counterpart would at best be a very tedious process and as a practical matter would probably be impossible. The addition of two impedances as shown in Figure 3b provides local series feedback and results in a composite n-p-n transistor whose characteristics are almost independent of the characteristics of the individual transistors as will be shown by the following analysis. If the bias levels are ignored for the present, the composite transistor of Figure 3b may be represented for small-signal purposes by the set of two-port networks shown in Figure 4a. Note: 'The addition of a current-source input and a load to complete the circuit as it will appear in the final form'. In the analysis, a two-port network will be represented by a matrix using the standard notation as given by Shea (16). The subscript will indicate the particular element of a matrix and the superscript will indicate the matrix to which it belongs. i\z Thus b^2 will be the first-row, second-column element of the B matrix for the fourth two-port network. The hybrid-tt model of the transistor will be used as the standard model for all of the following analysis (15). This model represents the transistor quite satisfactorily for small-signal analysis below the a-cutoff frequency and its parameters are readily interpreted as physical quantities.

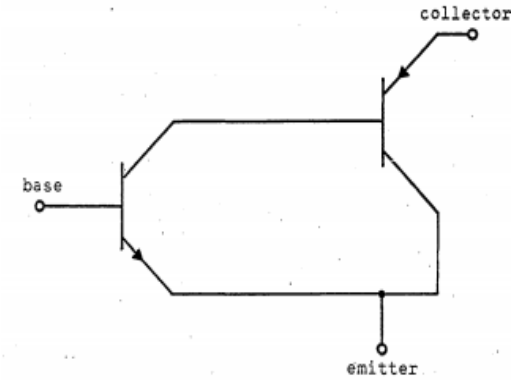


Fig: One possible composite n-p-n transistor

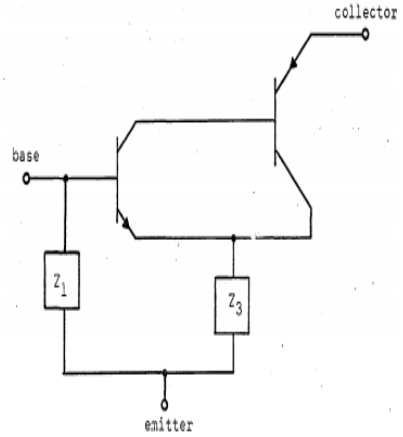
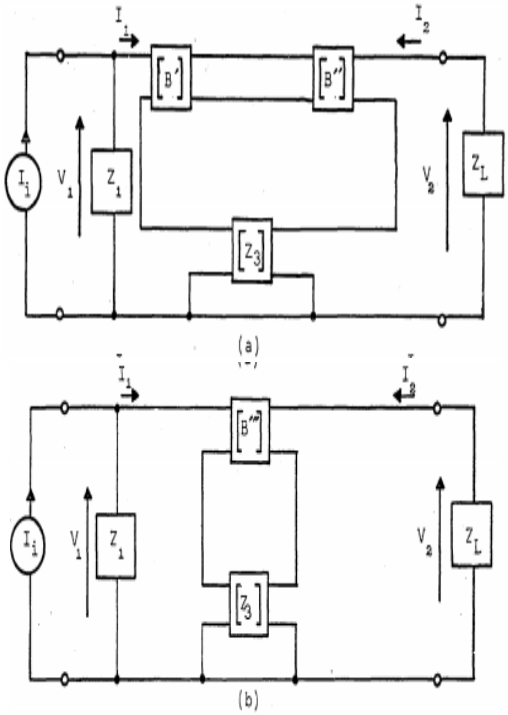


Fig: The final form of the composite n-p-n transistor



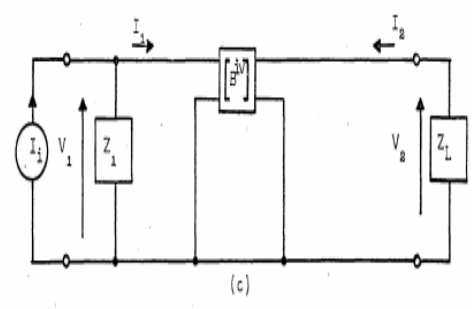


Fig: Sequence of two-port networks used in the analysis of the n-p-n composite transistor.

III. PROPOSED PUSH–PULL COMPOSITE POWER TRANSISTOR

A. Class-A Composite Power Transistor:

Under ultralow-voltage operating environment, to have enough loop gain, LDO regulators with multistage structure are often adopted. To improve the voltage swing, o/p stage with only 2 transistors [Fig. 2(a)] is allowed to serve as a power transistor driver. By adopting this structure, the LDO regulator is potentially unstable because of the multiple high-impedance nodes in the control loop. To solve this problem, a complex frequency compensation technique is required. To eliminate the need of complex frequency compensation, a Class-A composite power transistor is proposed in and

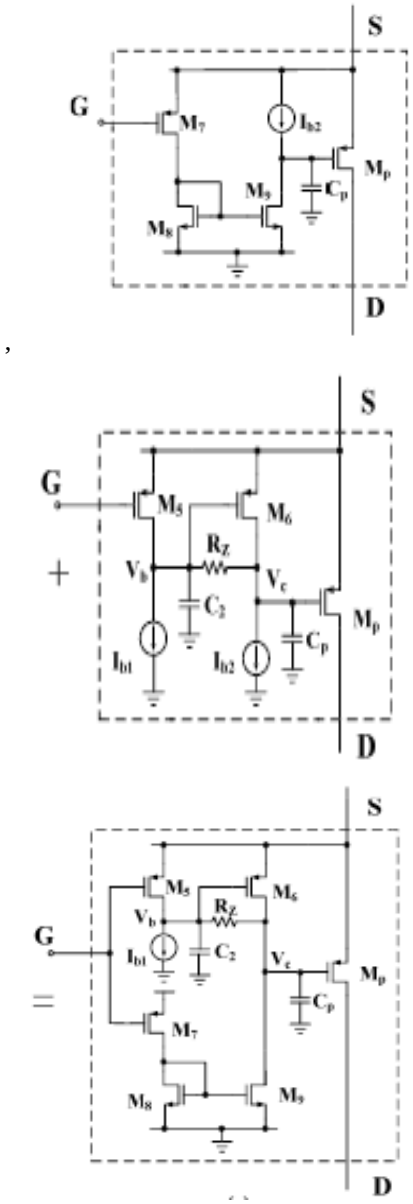


Fig: (a) Conventional non inverting stage + power transistor. (b) Class-A
composite power transistor. (c) Proposed push–pull composite power.

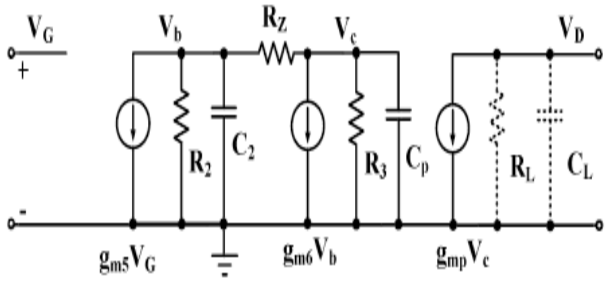


Fig: Small-signal model of the Class-A composite power transistor

This has an open-loop structure, is shown in Fig.4.2. The small signal model of the composite power transistor is given in Fig.3,with *RL* and *CL* representing the effective resistive and capacitive load, respectively. This loading effect will be included in the analysis when the composite transistor forms the circuit in the subsequent LDO circuit topology.

By applying the nodal analysis to the small-signal model that excludes the loading effect, the frequency-dependent transconductance *G*mp*(*Class-A*)* of the composite power transistor which is defined as the ratio of output current *g*mp *Vc* to input voltage *VG* can be approximated as

$$G_{mp(class-A)} = \frac{g_{m5}R_Z}{\left(1+\frac{C_p(R_2+R_Z)}{g_{m6}R_2}S\right)\left(1+\frac{C_2R_ZR_2}{R_2+R_Z}S\right)} g_{mp} \quad \ldots\ldots (4)$$

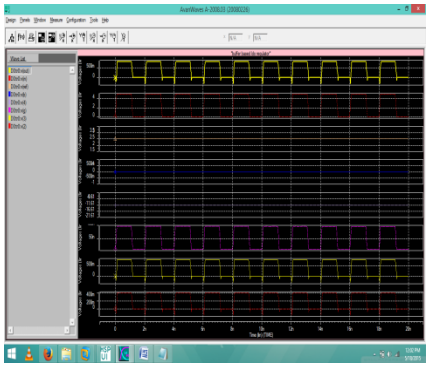
Where *g*mp is the transconductance for the respective devices, *Ci* and *Ri* are the respective lumped parasitic capacitance and resistance at the output of each stage. As can be seen from (3), the transconductance consists of two poles. In general, the parasitic capacitor *C*2 is small. Therefore, the second pole can be ignored. Due to the shunt feedback resistor *RZ*, the output impedance of the Class-A driver approximately equals to (*R*2 + *RZ*)/*R*2*gm*6. If *R*2 _ *RZ* , the output impedance ≈1/*gm*6. This low impedance will be helpful in the context of stability of the LDO regulator. In advanced nanometer CMOS technology, the value of *RZ* could be close to *R*2 such that the output impedance is ∼2/*gm*6. In short, the Class-A driver can be viewed as a buffer stage with gain of *gm*5 *RZ* . Therefore, it offers the advantage of higher stability over other designs.

Push–Pull Composite Power Transistor

The operation of the push–pull composite power transistor in Fig. 2(c) is explained in the following. The static bias current source *Ib*2 is replaced by a signal-dependent current source formed by transistors *M*7 −*M*9. Consequently, the bias current of transistor *M*6 and *M*9 depends on the voltage level at the gate of the composite power transistor. With the signal dependent current source, the sinking capability at node *Vc* is no longer limited by the static current source *Ib*2. The proposed low-voltage push–pull structure will provide extra transient current which is much larger than the static bias current at node *Vc* during transient event.

$$G_{mp(push-pull)} = \frac{\left(g_{m5}R_Z+\frac{g_{m7}}{g_{m6}}\right)\left(1+\frac{g_{m7}C_2}{g_{m5}g_{m6}}S\right)}{\left(1+\frac{C_p(R_2+R_Z)}{g_{m6}R_2}S\right)\left(1+\frac{C_2R_ZR_2}{R_2+R_Z}S\right)} \times g_{mp} \quad \text{…..(5)}$$

From (4), it can be seen that the transconductance of the push–pull composite power transistor is larger than that of the Class-A counterpart due to the signal-dependent current source. In addition, the signal-dependent current source also introduces a left-hand-plane zero. However, it is a function of parasitic capacitance and can be located at high-frequency easily. Furthermore, the parasitic pole is also located at high frequency. Similar to the Class-A version, the transconductance and bandwidth are independent of each other.



IV. CONCLUSSION

A transient-enhanced OCL-LDO regulator with push–pull composite power transistor implemented in 65-nm CMOS technology has been introduced. With the proposed low voltage circuit architecture, the LDO regulator can operate at sub-1 V supply. Furthermore, the proposed push–pull structure improves the load transient response. Both undershoot and overshoot are improved greatly when compared with the counterparts. Finally, with the composite power transistor, the no dominant poles are located at higher frequencies. Thus, the compensation capacitor can be made small. In view of silicon area, the smaller compensation capacitor leads to a small-area LDO regulator. This is very suitable for VLSI implementation in which the silicon overhead of the proposed regulator for fully on-chip applications is small.

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