# A Fast Approach Towards Test Program Generation For Mixed Signal IC

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***Abstract-*** *In VLSI industries the cost of the product depends on the several factors like silicon cost, packaging cost and testing cost. Testing cost can be reduced by the simplification of the test program development for the Automatic Tester Equipment(ATE). The existing flow includes generation of the test patterns(vectors) for testing the particular Analog Mixed Signal IP/design, which later on will be given to the test engineer for the generation of the test program utilizing these vectors, at post silicon phase. In case of any silicon issues, it involves multiple iterations between the DFT and Test engineers to debug, develop and to simulate the test cases, leading to increase in Time to Market (TTM). The new flow proposes the generation of test program itself along with the testbench in pre-silicon phase. Hence reducing product cost as well as the time to market.*

***Keywords***- Mixed Signal IC, ATE, Test program, Time to Market

## I. INTRODUCTION

DFT contributes to achieve high quality metrics and to reduce the time involved in the test vector generation and the cost involved with the test vector application. The "Virtual Test" concept can help for the simplification of the program development. It is highly valuable to any organization, as the hardware testers are much costlier. The emergence of Virtual Test had been delayed until now due to the complex mixed-signal design space, the lack of standardized HDLs for behavioral level design and inadequate design tools. A major bottleneck in the time-to-market (TTM) for integrated circuits is the time taken to develop test programs. The digital IC test development is reasonably automated, but for the analog and mixed-signal ICs' test programs for a tester are still hand written. The test program is developed by the test engineer at the post silicon phase. This article proposes the development of test methodology for analog mixed signal designs(modules) with generation of test program at the pre-silicon phase with the information regarding the DIB and the resources to be used by the Automatic Tester Equipment (ATE) for the testing the circuit.

## II. MIXED SIGNAL CIRCUIT TESTING

Mixed signals circuits are the one which includes both the analog circuitry (e.g. filters, amplifiers) and digital circuitry (e.g. control logic and data paths), as well as analog to digital converters (ADCs) and digital to analog converters (DACs). As different types of circuitries are involved, several different techniques, to test a mixed signal circuit, are usually needed. During the testing of a digital block of a mixed signal circuit the analog blocks are isolated by the isolation cells i.e., the analog blocks are considered as the black boxes and are bypassed. The explicit functional testing is done on the analog blocks by configuring the isolation blocks/cells using the control blocks and the response is observed through one of the IC level pins. [1]

## III. PROBLEM STATEMENT

The traditional flow that many industries follow to generate test program for Mixed Signal designs includes the generation of the test vectors for the mixed signal modules which are nothing but the control signal for the isolation blocks. The generated patterns will be verified for the correctness considering the timing as well, via the simulation and if the pattern passes then those patterns will be handed off to the test engineer who utilizes these vectors and generates the test program (either hand written or automatically generated in post-silicon phase) compatible to the tester format (in C, C++, Python, etc.).

Different industries have different in-house tool for the test pattern generation for the mixed signal designs. But the idea for the pattern generation remains the same i.e., isolate the analog blocks and define the control bits controlling the mode in which the isolation cell works while testing the analog blocks. It involves multiple iterations between test engineering and DFT to debug, develop and simulate the test cases. To overcome the above scenario, it is necessary to arrive at the new test methodology for analog mixed signal designs which proposes required test structures for the AMS design and the test program development parallel to the test vector generation i.e., at pre-silicon phase. This enables Design, DFT, Verification and Test engineering to work collaboratively in a uniform platform for the early detection of problems, not only in test program but also in test architecture, design and load board.

## IV. PROPOSED APPROACH

The proposed approach of mixed signal test generation is as shown below. The testbench generator is provided with all the information like the design netlist, IC pining information, the resources (instruments) required for each test case, customized programing language which helps instructing the utility for the generation of testbench or the test program for defined tester.This approach requires the DIB information as per the test architecture, the timing information of the digital pins as we can't expect the ideal timing for the virtual test i.e., imitating the ATE in simulation environment. With the above inputs the testbench is generated including the testcase where the IC pins are driven via the load board.

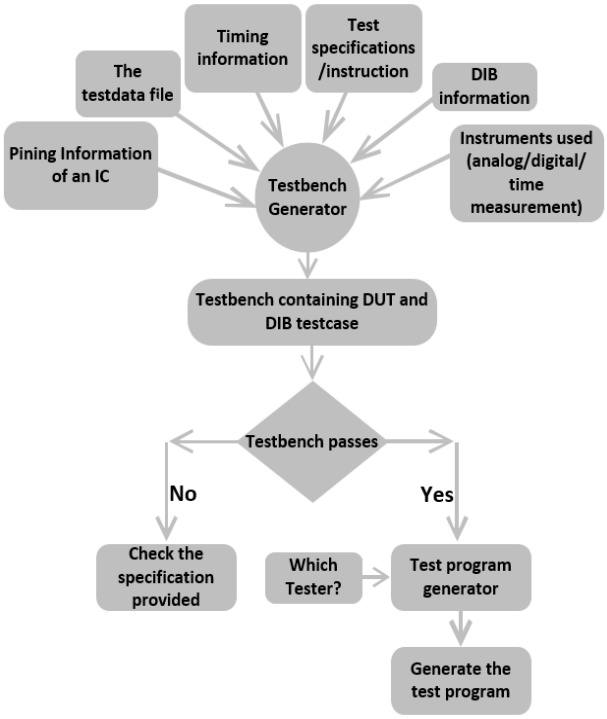


Figure 1: Proposed approach for Test program generation.

The testbench generated is verified for its correctness by simulating it on the top of design and DIB netlist. If the testcase passes then the test program is generated for the specified tester. All this is performed in the pre-silicon phase hence the test program generated will be optimized all the required debugs even before the arrival of first silicon hence reducing the time to market.

## V. ANALYSIS OF THE PROPOSED APPROACH

This approach proposes the generation of test program instead of test vectors in the pre-silicon phase itself applying the test cases through the load board. Hence mimicking the Automatic Test Equipment making sure the minor and time-consuming bugs like the tester instrument connection and the testing method are debugged before the silicon release.

## VI. CONCLUSION

The test development for the mixed signal designs is done using the proposed approach, can detect the bugs in the design as well as in the load board configuration even before the release of silicon, in the pre-silicon phase. Once the silicon release occurs it involves the iterative process between the DFT and test engineer to debug, develop and to simulate the test case. The test program developed will be accurate, helping us to reduce the product cycle, the Time to Market (TTM) and hence the cost of the product.

## REFERENCES

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